

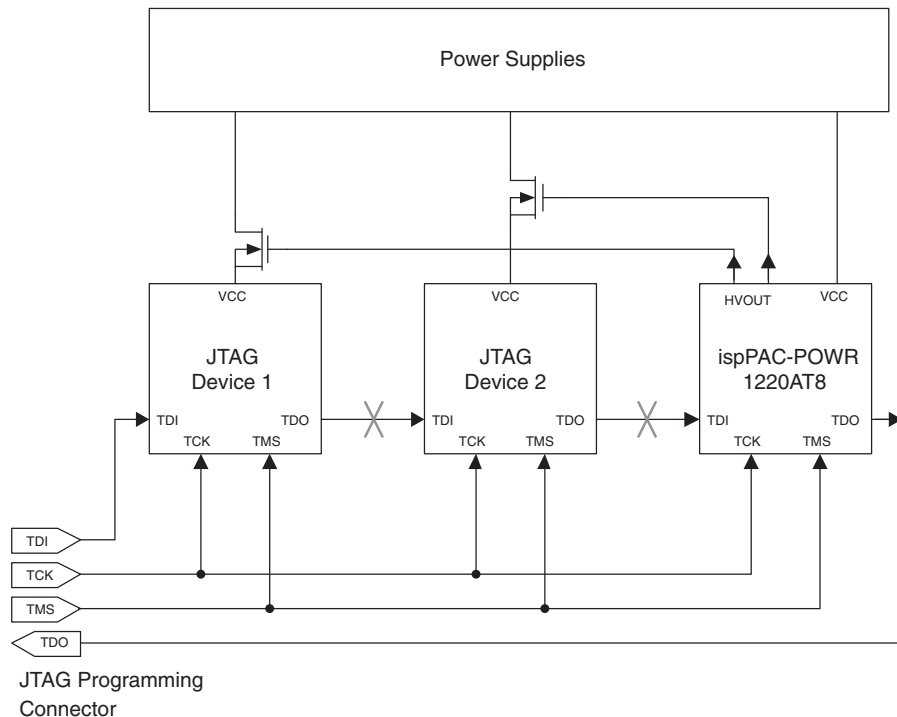
Introduction

The primary function of the ispPAC[®]-POWR1220AT8 is to monitor, measure, trim/margin and to sequence the application of power to electronic devices in complex, multi-supply environments. As with other members of the Power Manager II family from Lattice, the ispPAC-POWR1220AT8 is also a non-volatile E²C^{MOS}[®] device and can be programmed through its JTAG port. As such the configuration programming of the ispPAC-POWR1220AT8 can be done “in-system” during manufacturing. There are numerous manufacturing advantages associated with In-System Programmability (ISP[™]) such as simplified inventory management, reduced parts handling requirements and less complex assembly and test flows. Likewise, ISP designs support design changes and system upgrades throughout the life of a project with reduced design effort.

Configuration development for the ispPAC-POWR1220AT8 is accomplished using the Lattice-provided PAC-Designer[®] software design tool. PAC-Designer is a Windows[®]-based tool that provides engineers with an intuitive user-friendly graphical interface. This tool simplifies the task of learning, simulating, and designing power management solutions to a series of point-and-click operations.

Special design considerations arise when programming an ispPAC-POWR1220AT8 that is placed in a serial chain with other JTAG compliant devices. The first and most obvious challenge is when the power to other JTAG devices in the chain is controlled or sequenced by the ispPAC-POWR1220AT8. This is illustrated in the block diagram of Figure 9-1. In this diagram the devices in the chain that precede the ispPAC-POWR1220AT8 are not powered until the ispPAC-POWR1220AAT8 enables the supplies to them. However, the un-programmed ispPAC-POWR1220AT8 cannot enable the supplies until it is programmed through the JTAG chain. But, the JTAG chain remains broken by the powered down devices and the crossed out nets in Figure 9-1 highlight the broken links. Thus, another method of connecting devices for programming is suggested.

Figure 9-1. ispPAC-POWR1220AT8 in a “Broken” JTAG Chain



There are several alternative solutions that will address the issue of initially programming the Power Manager II.

- Avoid it altogether by using a preprogrammed ispPAC-POWR1220AT8 device.
- Put the ispPAC-POWR1220AT8 into a separate JTAG chain and use multiple JTAG connections.
- Use the ispPAC-POWR1220AT8’s proprietary, alternate TDI mode.

The first option sacrifices the flexibility of in-system programming and limits future re-programming options.

The second option adds both the cost and complexity of multiple JTAG interface connections. Many boards have physical restrictions and do not have the space required for a second connector.

The third option combines the flexibility of in-system programming with access to all the JTAG devices through a single serial connection. By using its alternative TDI input pin (ATDI), it is possible to send commands and data to program an ispPAC-POWR1220AT8 by physically bypassing the other devices in the same serial chain. Figure 9-2 illustrates the ATDI connection to the ispPAC-POWR1220AT8 at the end of the chain that provides a bypass path. Notice that while the other devices may be powered down, they are still connected to TMS and TCK. Therefore, for this circuit to function properly, they should be “hot socket” compatible so they do not load-down or clamp the TMS or TCK signals.

Figure 9-2. The ATDI Pin is Used to Physically Bypass Powered Down Devices

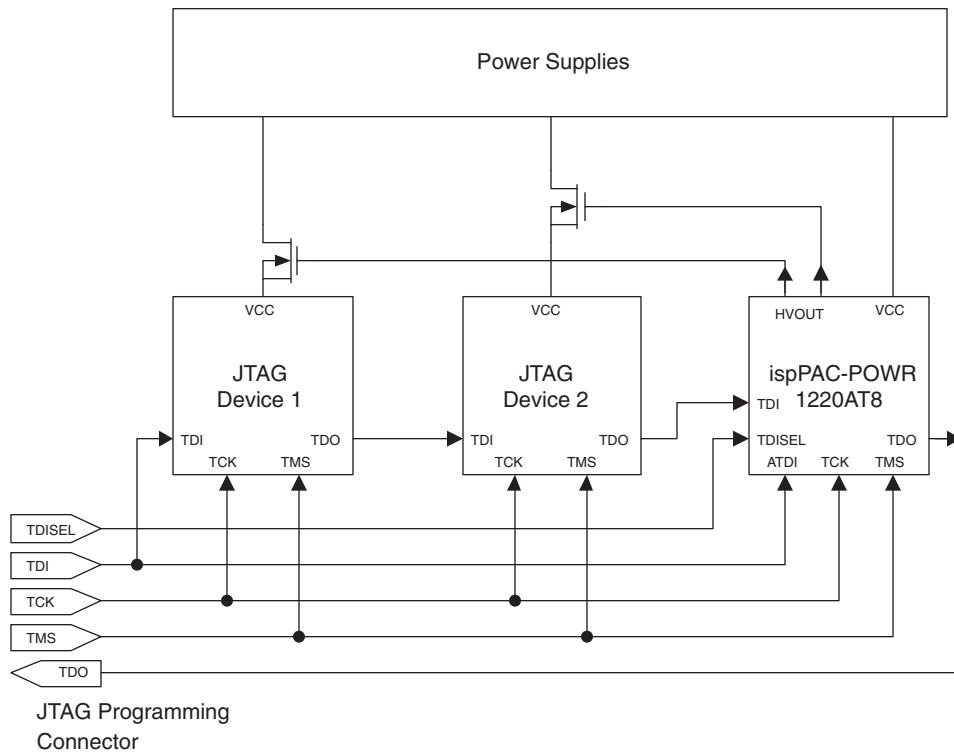


Figure 9-2 also shows the optional connection to the ispPAC-POWR1220AT8 TDISEL pin. This pin can be used to directly control the selection of either the TDI or ATDI pin for JTAG programming. The TDISEL pin connection is optional because there is also a software method of selecting between the TDI and ATDI pins. The software solution is realized by modifying the programming routine and makes use of the existing JTAG pins.

Enabling ATDI Through TDISEL Pin

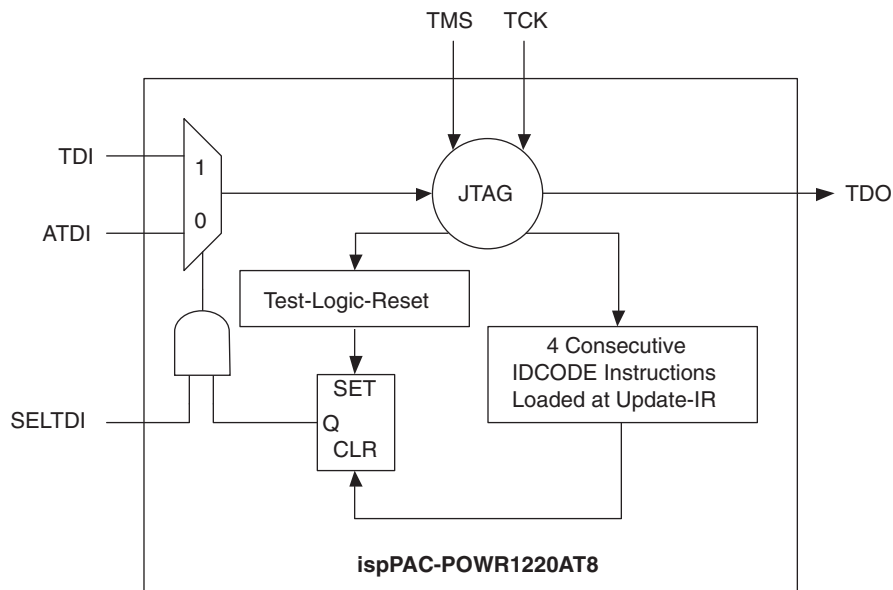
The TDISEL pin has an internal pull up so that when it is left unconnected the ispPAC-POWR1220AT8 will default to the standard TDI pin for JTAG input. When the TDISEL pin is driven low the ispPAC-POWR1220AT8 will uncon-

ditionally select the ATDI pin to be the active JTAG input instead of the TDI pin. Figure 9-3 illustrates the relationship between the TDISEL pin and the selection between the TDI pin and ATDI pin. When the input to the MUX is high the TDI pin is routed to the JTAG engine. Conversely, when the MUX input is low the ATDI pin is routed to the JTAG engine.

One key advantage of using the TDISEL pin is that changes to the data file or the fundamental programming algorithm do not have to be made. The control of the TDISEL pin can be realized by using a jumper or by driving the pin from a tester or programmer. When using the TDISEL pin the following programming flow is suggested:

1. Apply programming power and pull the TDISEL pin low with a jumper or by program control.
2. Erase, program, and verify the ispPAC-POWR1220AT8 with the desired configuration using standard programming routines that support either SVF or JEDEC formats.
3. Remove programming power and jumper (if used).
4. Apply system power and allow ispPAC-POWR1220AT8 to power up the other devices in the JTAG chain.

Figure 9-3. TDI and ATDI are Selected with the TDISEL Pin or JTAG Commands



Enabling ATDI Through JTAG Commands

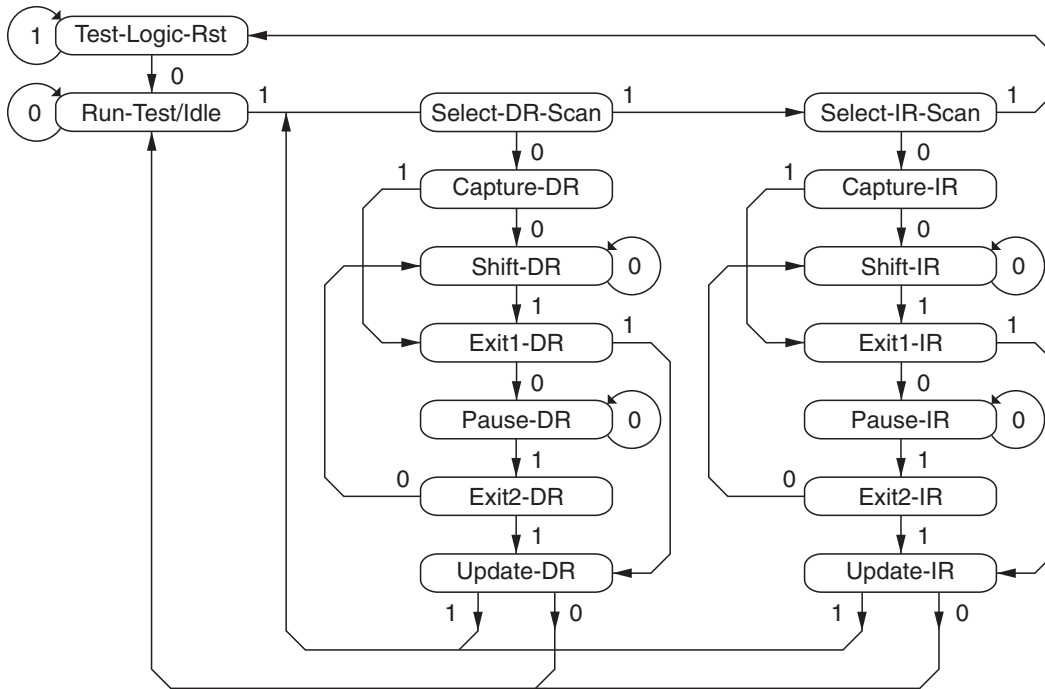
Figure 9-3 also contains the logic to support the ATDI pin selection from the JTAG circuitry. This method relies on the standard JTAG interface signals so the TDISEL pin can be left unconnected (the internal pull-up resistor will keep the pin high) or externally set high with a pull-up resistor or jumper. When the TDISEL pin is held high and four consecutive IDCODE instructions are decoded by the ispPAC-POWR1220AT8, it responds by making the ATDI pin its active JTAG data input. When ATDI is selected, data on its TDI pin is ignored until the JTAG state machine returns to the Test-Logic-Reset state.

This method of selecting ATDI takes advantage of the fact that a JTAG device with an IDCODE register will automatically load its unique IDCODE instruction into the instruction register (IR) after a Test-Logic-Reset (TLR) to support blind interrogation. Blind interrogation is a method by which a test program or programming routine can determine which devices are present without any foreknowledge. This is accomplished by clocking all the devices in the chain from TLR to the CAPTURE-DR state and then to the SHIFT-DR state. Now each device in the chain is positioned to shift out its own 32-bit ID code so the tester or programmer can figure out which device is where in the chain.

Blind interrogation is accomplished without presenting any data on the TDI pin and therefore synchronizing a switchover from TDI to ATDI is not needed. Taking advantage of this JTAG feature, the ispPAC-POWR1220AT8 selects the ATDI pin to be the active JTAG data input after it detects that four consecutive IDCODE instructions have been latched into UPDATE-IR. Data on the unselected TDI input is ignored after that.

By examining the state machine in Figure 9-4, one can visualize how the IDCODE instruction can be latched in UPDATE-IR four consecutive times without using the TDI pin. Note that state transitions are accomplished using only TMS and TCK signals. From Test-Logic-Reset (TSR), where the IDCODE is loaded into the IR, TMS and TCK are toggled to move the machine to the Capture-IR state. By setting TMS high and applying two TCK edges the machine skips over the Shift-IR state and goes right to Update-IR. By skipping the Shift-IR state, the IR preserves the IDCODE instruction and retracing the capture-exit-update path three more times provides the trigger required to clear the latch in Figure 9-3 that engages the ATDI pin.

Figure 9-4. JTAG Test Access Port (TAP) State Machine Diagram



Note: The value shown adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK.

The SVF code in Listing 1 is an example of how to select the ATDI pin when using an SVF programming tool (ispVM for example). The bold text is the code that has been added to an existing SVF file to drive the state machine and enable the ATDI pin.

Listing 1. SVF Code Modification to Enable ATDI

```

TRST ON;
TRST OFF;
ENDIR IRPAUSE;
ENDDR DRPAUSE;

! enable the ATDI pin on the ispPAC-POWR1220AT8
STATE IRPAUSE;
STATE IDLE;
STATE IRPAUSE;
    
```

```

STATE IDLE;
STATE IRPAUSE;
STATE IDLE;
STATE IRPAUSE;
STATE IDLE;
! repeat the above code after every TRST ON/OFF or STATE RESET

```

At first glance this code may appear to be insufficient to specify the required path that was described above. However, according to the SVF specification, when a “state” keyword has only one “statepath” parameter and that parameter is a stable state, then the path taken is implied based upon the current state. Therefore, the terse code in Listing 1 is sufficient to drive the state machine through the UPDATE-IR state four times and enable the ATDI pin. As we examine each of the implied paths below, notice that every path skips the Shift-IR state and the IDCODE remains unchanged in the IR from reset. From the SVF specification, the path from Reset to Pause-IR is as follows:

- RESET
- IDLE
- DRSELECT
- IRSELECT
- IRCAPTURE
- IREXIT1
- IRPAUSE

Likewise, the SVF specification says the path from Pause-IR to Idle is as follows:

- IRPAUSE
- IREXIT2
- IRUPDATE
- IDLE

Finally, the SVF specification says the path from Idle to Pause-IR is as follows:

- IDLE
- DRSELECT
- IRSELECT
- IRCAPTURE
- IREXIT1
- IRPAUSE

When using the software method to activate the ATDI pin, the following programming flow is suggested;

1. Apply programming power only to the ispPAC-POWR1220AT8 using the VCCPROG and VCCJ pins.
2. Erase, program, and verify the ispPAC-POWR1220AT8 with the desired configuration using a modified programming routine or modified data file (.SVF).
3. Remove programming power.
4. Apply system power and allow ispPAC-POWR1220AT8 to power up the other devices in the JTAG chain.

Power Supply Considerations when Programming

Regardless of which method is used to activate the ATDI pin (hardware or software), the application of power during and after programming is essentially the same. In addition to having a flexible JTAG input pin the ispPAC-POWR1220AT8 also supports multiple power supply pins to facilitate various programming schemes. A separate power supply pin is provided, VCCPROG, making it easy to isolate and program ispPAC-POWR1220AT8 before other devices in the same circuit are powered on. This can be done without using external circuitry or jumpers. Figure 9-6 shows how a single power supply can power both the VCCPROG and VCCJ to initially program the isp-

PAC-POWR1220AT8. If the other devices in the JTAG chain have VCCJ pins, then they should be powered along with the Power Manager's VCCJ to prevent the TMS and TCK pins from being clamped. Figure 9-5 shows how the ispPAC-POWR1220AT8 can be programmed without using VCCPROG.

Figure 9-5. Power Supply Connections for Initial Programming of the Power Manager Without VCCPROG

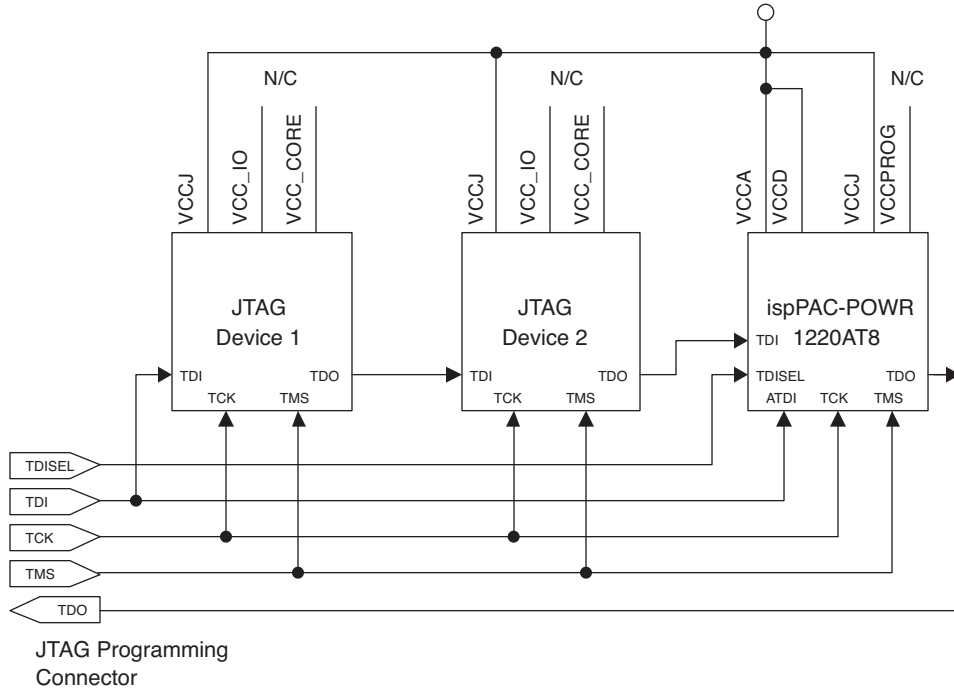
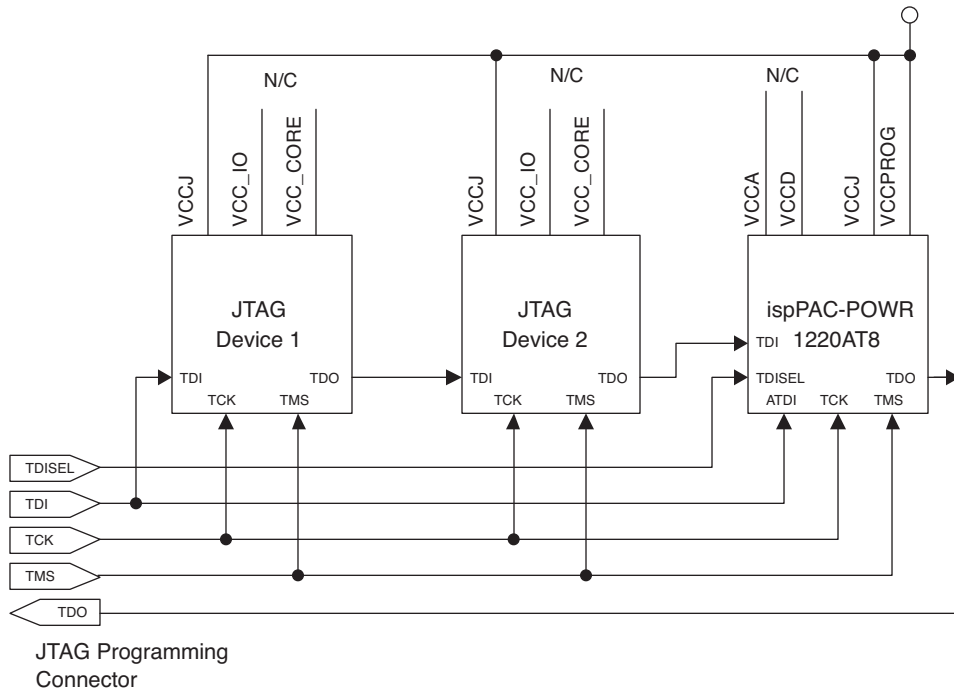


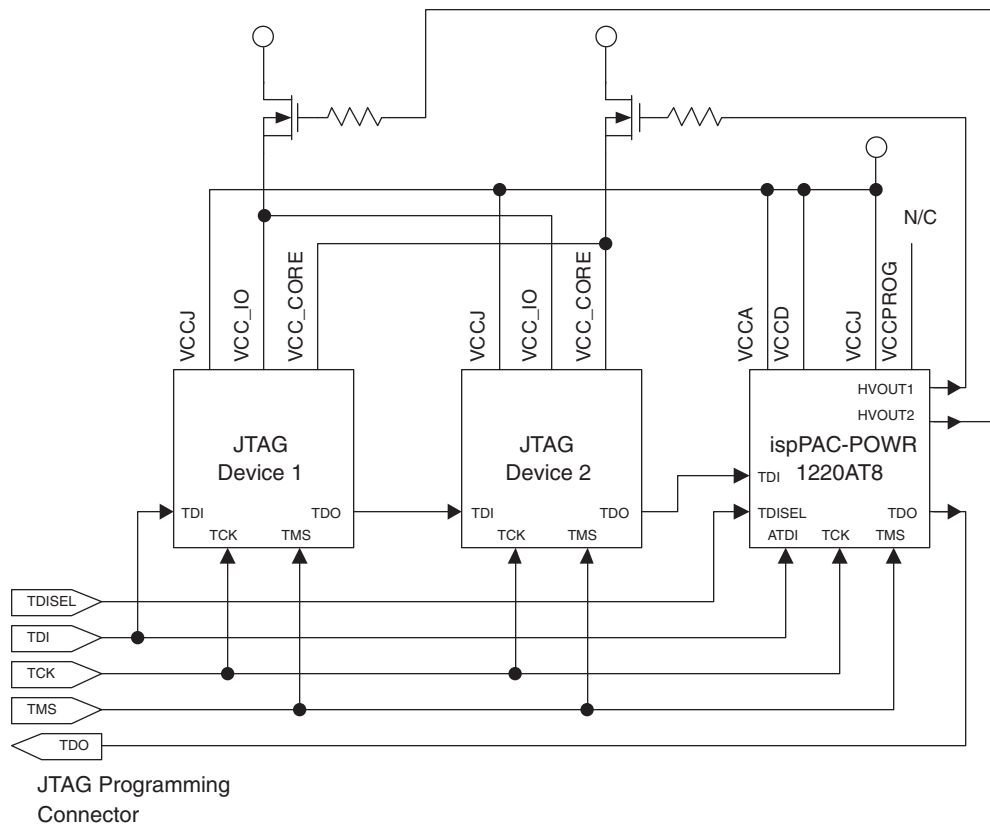
Figure 9-6. Power Supply Connections for Initial Programming of the Power Manager Using VCCPROG



After the ispPAC-POWR1220AT8 has been programmed, power must be removed from the VCCPROG pin before applying power to both the VCCA and VCCD pins. This is shown in Figure 9-7. Now the ispPAC-POWR1220AT8 will execute the sequence that it has been programmed with and power up the other devices in the chain so they can be programmed.

Using VCCPROG pin of the ispPAC-POWR1220AT8 for programming instead of the VCCD pin will insure power is only applied to its programming circuitry. Whether using VCCPROG or VCCD for programming, VCCJ is always required to bias the JTAG I/O to the correct logic levels. When the ispPAC-POWR1220AT8 is using VCCPROG and its VCCD pin is open, or pulled low, all inputs to the device except for the JTAG pins are ignored and digital output pins other than TDO are in a Hi-Z state. Output pins that are configured as HVOUT charge pumps will be pulled low to prevent turning on any MOSFETs. VCCD and VCCA should be applied after VCCPROG has been removed to insure that the internal power-on-reset circuitry is activated. Likewise, VCCJ should be removed after programming the ispPAC-POWR1220AT8 and re-applied before programming the rest of the JTAG chain.

Figure 9-7. Power Supply Connections for Sequencing and Programming the Rest of the Chain



Summary

In this application note we have explored two methods of taking advantage of the ispPAC-POWR1220AT8's alternative TDI pin (ATDI) to program in-system while other devices in the JTAG chain remain powered down. One solution is to use the TDISEL pin to enable the ATDI pin and the other solution makes use of a unique JTAG sequence to enable the ATDI pin. Table 9-1 summarizes the means by which the ATDI pin can be activated.

Table 9-1. ATDI Selection Methods

TDISEL Pin	JTAG State Machine Test-Logic-Reset	Four Consecutive IDCODE Commands Loaded at Update-IR	Active JTAG Data Input Pin
H	No	Yes	ATDI
H	Yes	No	TDI
L	X	X	ATDI

In addition to the flexible JTAG input structure, we have also examined the power supply features of the ispPAC-POWR1220AT8 device. The VCCPROG pin provides a way to isolate programming power to only the ispPAC-POWR1220AT8 thus eliminating the need for external circuitry or jumpers. The VCCJ pin provides compatibility with many different I/O voltage standards. The ispPAC-POWR1220AT8 from Lattice provides designers with numerous options for in-system programming.

Related Literature

- DS1015, [ispPAC-POWR1220AT8 Data Sheet](#)
- AN6062, [Using ispVM System to Program ispPAC Devices](#)
- Serial Vector Format Specification Revision E, March 1999 ASSET InterTech

Technical Support Assistance

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Revision History

Date	Version	Change Summary
November 2005	01.0	Initial release.
February 2011	01.1	Clarified usage of VCCPROG pin.