L-ASC10 and Platform Manager 2 Hardware Checklist

March 2015 Technical Note TN1225

Introduction

When designing complex hardware using L-ASC10 and Platform Manager 2, designers must pay special attention to critical hardware configuration requirements. This technical note steps through these critical hardware requirements related to the L-ASC10 and Platform Manager 2 devices. This document does not provide detailed step-by-step instructions but gives a high-level summary and checklist to assist in the design process.

This technical note assumes that the reader is familiar with the L-ASC10 and Platform Manager 2 device features as described in DS1042, L-ASC10 Data Sheet and DS1043, Platform Manager 2 Data Sheet.

The critical hardware areas covered in this technical note include:

- Power supplies as they relate to the Platform Manager 2 supply rails and how to connect them to the PCB and the associated system
- Configuration and how to connect the configuration mode selection for proper power up configuration
- System connections required for proper operation of the Platform Manager 2 system
- Device I/O interface and critical signals.

Important: Users should refer to the following documents for detailed recommendations.

- TN1068, Power Decoupling and Bypass Filtering for Programmable Devices
- TN1198, Power Estimation and Management for MachXO2 Devices
- TN1202, MachXO2 sysIO Usage Guide
- TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices

Power Supplies

There are several different types of power rails required to operate the Platform Manager 2 devices. Each type will be discussed to assist the user in setting up the board correctly.

VCC

The core power for the FPGA section of the Platform Manager 2 is the VCC rail. VCC is nominally 3.3 V, with a minimum of 2.8 V and a maximum of 3.465 V. VCC must have 0.1 uF decoupling capacitors located as close to the VCC pins as possible. In addition to the 0.1 uF capacitors, a 1-10 uF tantalum capacitor should be added to the rail on the board.

VCCA

The VCCA is an analog supply for the ASC section of Platform Manager 2. This supply should have a 0.1 uF capacitor close to the VCCA pin and a ferrite bead to isolate the supply from the VCC rail. The nominal value is 3.3 V, with a minimum of 2.8 V and a maximum of 3.465 V. The values listed here are practical limits taking into account the interface to the FPGA section of Platform Manager 2 or to a MachXO2.

VCCIO0, VCCIO1, VCCIO2, and VCCIO3

These are the FPGA PIO bank supplies. In general, the VCCIO supply must be in the range from 1.14 V minimum to 3.465 V maximum except where noted below. It is recommended to include a 0.1 uF decoupling capacitor located close to the VCCIO pins. When a PIO bank is hooked up as 3.3 V, for example, all of the PIOs in that bank share a common 3.3 V I/O voltage. If a PIO bank is not used, the VCCIO pins for that bank should be connected to the VCC rail on the board.

VCCIO0

This is the supply for FPGA Bank 0 as well as the supply for the JTAG and I^2C ports. This rail is required for programming and has a minimum of 2.8 V and a maximum of 3.465 V. It is recommended to include a 0.1 uF capacitor located close to the VCCIO0 pin.

VCCIO1

This is the supply for FPGA Bank 1. For Platform Manager 2 devices, bank 1 is used to interface to the internal ASC section. Therefore the VCCIO1 supply has a minimum of 2.8 V and a maximum of 3.465 V. For Platform Manager 2 or MachXO2 designs which include external ASCs, the PIO banks that are used to interface to the ASC must have a VCCIO supply between 2.8 V and 3.465 V. It is recommended to include a 0.1 uF capacitor located close to the VCCIO1 pin.

Table 1. Power Supply Description and Voltage Levels

Supply	Voltage (Nominal Value)	Description
VCC	3.3 V	Core power supply for FPGA section of Platform Manager 2.
VCCA	3.3 V	Core power supply for Analog section (or ASC) of Platform Manager 2.
VCCIO0	3.3 V	Power Supply for PIO Bank 0, JTAG, and I^2C pins.
VCCIO1	3.3 V	Power Supply for PIO Bank 1 and ASC interface section of LPTM21.
VCCIO2	1.2 V to 3.3 V	Power Supply for PIO Bank 2.
VCCIO3	1.2 V to 3.3 V	Power Supply for PIO Bank 3.

Power Good Condition

The VCC, VCCA, and VCCIO0 power supplies determine the internal “power good” condition for the Platform Manager 2 device. All three of these supplies need to be at a valid and stable level before the device can become operational. In addition, when using external ASC devices which are “Mandatory”, these are required to be powered up fully before the Platform Manager 2 can become operational. If the system is using “Optional” external ASC devices, these do not have to be powered up fully before the Platform Manager 2 can become operational.

For most applications all supplies can be tied to a common VCC rail of 3.3 V, with added ferrite isolation on VCCA. When they are all common, the rails will all come up at the same time and the device would be set up for VCC, VCCIO, inputs/outputs, JTAG, etc. at the nominal range for 3.3 V logic interfaces.

Ground Pins

The Platform Manager 2 device uses both GND and GNDIO pins. The GNDIO0, GNDIO1, GNDIO2, and GNDIO3 pins are the ground pins for each of the PIO Banks of the device. All ground pins are required to be connected to a common ground plane.

External ASC Considerations

When using an external ASC device insure that the power supply for the external ASC has a common ground reference level with the Platform Manager 2 or MachXO2 device. This can be challenging if the external ASC is mounted on a separate card but is important. In addition, the power supplies for the ASC must have levels which are similar to the Platform Manager 2 VCCIO rails. Different voltage levels may adversely affect the signals between the Platform Manager 2 or MachXO2 and the external ASC devices.

If programming external ASC devices in-system, insure that the VCC source to the external ASC devices will not be turned off when the Platform Manager 2 enters a programming sequence and its outputs return to their safe state condition.

Power Estimation

Once the Platform Manager 2 device density, package and logic implementation is decided, power estimation can be performed using the Power Calculator tool which is provided as part of the Lattice Diamond® design software. While performing power estimation the user should keep two specific goals in mind.

1. Power supply budgeting should be considered based on the maximum of the power-up in- rush current, configuration current or maximum DC and AC current for a given system environmental condition.
2. The ability of the system environment and Platform Manager 2 device packaging to support the specified maximum operating junction temperature.

By determining these two criteria, system design planning can take the Platform Manager 2 power requirements into consideration early in the design phase.

This is explained in TN1198, Power Estimation and Management for MachXO2 Devices.

Configuration Considerations

Platform Manager 2 devices contain two types of memory, SRAM and non-volatile. SRAM is volatile memory and contains the active configuration. The non-volatile memory provides on-chip storage for the SRAM configuration data. The FPGA section uses flash memory for non-volatile storage while the ASC uses EEPROM for non-volatile storage.

The Platform Manager 2 is configured using the JTAG port but can also be configured from the primary I^2C port. The ASC devices are configured from the I^2C port. The Diamond Programmer software will automatically send the configuration data to the appropriate ports.

When using the Dual Boot mode (enabled in software) the "Golden Image" of the system configuration can be stored in an external SPI flash and the master SPI port will be used.

For ease of prototype debugging it is recommended that every PCB should have easy access to the programming and configuration pins.

The use of external resistors is always needed if the configuration signals are being used to handshake with other devices. Pull-up and pull-down resistor (4.7K) recommendations on different configuration pins are listed below. External pull-up or pull-down resistors should be added to the pins shown in Table 2 if the configuration port is used in the design. If the optional pins are left as general purpose I/O then the external resistors are not needed.

When using JTAG programming, place a 4.7K pull-up on the TMS signal and a 4.7K pull-down on the TCK signal. For noisy environments, an optional R/C filter can be placed on the JTAG clock line, TCK. Use a 100 Ohm series resistor located close to the TCK pin and a 50 pF capacitor to ground.

Table 2. Default State of the sysCONFIG Pins

Pin Name	Pin Function (Configuration Mode)	Pin Direction (Configuration Mode)	Default Function (User Mode)
PROGRAMN	PROGRAMN	Input with weak pull-up, Add external pull-up	PROGRAMN
INITN	I/O	I/O with weak pull-up	User-defined I/O
DONE	I/O	I/O with weak pull-up	User-defined I/O
MCLK/CCLK	SSPI	Input with weak pull-up, Add external pull-up	User-defined I/O
SN	SSPI	Input with weak pull-up, Add external pull-up	User-defined I/O
SI/SPISI	SSPI	Input	User-defined I/O
SO/SOSPI	SSPI	Output	User-defined I/O
CSSPIN	I/O	I/O with weak pull-up, Add external pull-up 10K	User-defined I/O
SCL	I^2C	Bi-Directional open drain, Add external pull-up	SCL
SDA	I^2C	Bi-Directional open drain, Add external pull-up	SDA
TDI	TDI	Input with weak pull-up	TDI
TDO	TDO	Output with weak pull-up	TDO
TCK	TCK	Input, Add external pull-down	TCK
TMS	TMS	Input with weak pull-up, Add external pull-up	TMS
JTAGENB	I/O	Input with weak pull-down, Add external pull-up	I/O

PROGRAMN Initial Power Considerations

The Platform Manager 2 PROGRAMN pin is permitted to become a general purpose I/O. The PROGRAMN only becomes a general purpose I/O after the configuration bitstream is loaded. When power is applied to the Platform Manager 2, the PROGRAMN input performs the PROGRAMN function. It is critical that any signal input to the PROGRAMN have a high-to-low transition period that is longer than the VCC (min) to INITN rising edge time period. Transitions faster than this time period prevent the Platform Manager 2 from becoming operational. It is recommended that the PROGRAMN pin be used for configuration only to avoid startup problems of the Platform Manager 2 device.

System Connections

When using a Platform Manager 2 design, there are a number of connections that must be made on the customer's board. Some are made between pins of the LPTM21 device. Others are made between the LPTM21 or MachXO2 and the external ASC devices. The required connections are listed below along with the conditions for each.

RESETb Connections

User MUST connect the RESETb pin from the LPTM21 to a PIO pin of the FPGA section. This must be done external to the device package on the customer's board. If using external ASC devices the user must also connect the RESETb pin from the ASC to a PIO of the FPGA.

If using a MachXO2 FPGA with external ASC devices the user MUST connect the RESETB from the ASC to a PIO of the MachXO2.

The RESETb pins from all Mandatory ASC devices must be connected to the same PIO pin on the FPGA section. ASC0 is always Mandatory by design. The RESETb pins from all Optional ASC devices must be connected to individual PIO pins of the FPGA section. For examples of the required connections see Figure 1 through Figure 2 in the Appendix. For more information see DS1042, L-ASC10 Data Sheet and DS1043, Platform Manager 2 Data Sheet.

The RESETb pin must not be used for the sequencer control logic reset. Instead, an FPGA PIO pin should be used along with equations or logic steps that reset the sequencer control logic. Any FPGA PIO pin can be used for this function though it must not be the same PIO pin that is connected to a RESETb pin.

ASC CLOCK Connections

If using an LPTM21 device, the ASCCLK pin is a NO CONNECT pin for all external ASCs and for the LPTM21 device. For an example of the required connections see Figure 1 in the appendix. For more information see DS1042, L-ASC10 Data Sheet and DS1043, Platform Manager 2 Data Sheet.

If using a MachXO2 FPGA with external ASC devices the user MUST connect the ASCCLK pin from ASC0 to a PCLK pin (True) on the MachXO2. For any other external ASCs the ASCCLK pin is a NO CONNECT pin. For examples of the required connections see Figure 2 in the Appendix. For more information see DS1042, L-ASC10 Data Sheet and DS1043, Platform Manager 2 Data Sheet.

ASC Interface Connections

For all external ASC devices the user MUST connect the WRCLK, WDAT, and RDAT pins of the ASC to PIO pins on the FPGA section or MachXO2 FPGA. Each ASC in the system MUST have its own three I/O pins assigned for these signals; the ASC devices CANNOT share these I/O pins on the MachXO2. For examples of the required connections see Figure 1 through Figure 2 in the Appendix. For more information see DS1042, L-ASC10 Data Sheet and DS1043, Platform Manager 2 Data Sheet.

Please note that the NC_FT1, NC_FT2, and NC_FT3 pins are NO CONNECT pins on the LPTM21 device. It is recommended to bring these pins out to test points close to the device for diagnostic purposes but these pins MUST NOT be connected to VCC, GND, or to any other devices in the system.

I^2C Connections

For an LPTM21 project the user MUST connect the SDA_S and SCL_S pins on the package to the SDA_M and SCL_M pins of the FPGA section. This must be done external to the device package on the customer's board. For an example of the required connections see Figure 1 in the Appendix. For more information see DS1042, L-ASC10 Data Sheet and DS1043, Platform Manager 2 Data Sheet.

For LPTM21 projects the user MUST connect the SDA and SCL pins on all external ASC devices to the SDA_M and SCL_M pins on the LPTM21 device. For MachXO2 projects the user MUST connect the SDA and SCL pins on all external ASC devices to the SDA/PCLKC0_0 and SCL/PCLKT0_0 pins on the MachXO2 device. For examples of the required connections see Figure 1 through Figure 2 in the Appendix. For more information see DS1042, L-ASC10 Data Sheet and DS1043, Platform Manager 2 Data Sheet.

Make sure there are external pull-up resistors (typically 2.2K to 3.3K) on the SDA and SCL lines from the LPTM21 device.

It is recommended to add a 50 ns filter to the I^2C lines which connect to the SDA/PCLKC0_0 and SCL/PCLKT0_0 pins on the MachXO2 or the SDA_M and SCL_M pins of the LPTM21 device to insure compliance with the I^2C specification.

I^2C Write Protect

If using the I^2C write protect feature in your design, the user MUST connect the ASC GPIO1 pin to a PIO pin on the FPGA section. For examples of the required connections see Figure 2 in the appendix. For more information see DS1042, L-ASC10 Data Sheet and DS1043, Platform Manager 2 Data Sheet.

I²C Address Pin

When using external ASC devices the user MUST connect the appropriate size resistor to the I2C_ADDR pin on the ASC. See Table 3 for a listing of the required resistor sizes for each ASC in the system.

Table 3. Resistor Sizes for External ASC I2C_ADDR Pin

ASC Device Number	Raddr Value
0[2]	Tie to GND
1	2.2 kΩ
2	4.4 kΩ
3	7 kΩ
4	10 kΩ
5	14 kΩ
6	18 kΩ
7	Tie to +3.3 V[1]

1. Tie to same supply used for VCCA of the ASC device.
2. For LPTM21 projects the External ASCs start with ASC1. The Internal ASC of the LPTM21 has the I2C_ADDR pin connected On-Chip and is always designated as ASC0.

External ASC Die Pad

The die pad of the external ASC package (48 pin QFN) is the ground connection for this package and MUST BE connected to the ground of the PCB by the user. This pin is listed as pin 49 in DS1042, L-ASC10 Data Sheet.

I/O Pins

There are several types of I/O pins on the Platform Manager 2 device. These range from special function pins to standard inputs and outputs. Designers need to pay attention to the different types of pins to understand their functions and how they interface to other analog or digital circuits on the board. Listed below is a summary of the different pin types and their typical configuration requirements. Refer to DS1043, Platform Manager 2 Data Sheet for detailed information.

GPIO Pins

The GPIO1 through GPIO10 pins can be configured either as input or output pins (but not as true bi-directional pins). When configured as outputs these are open-drain type outputs. These pins are controlled by the logic equations defined in the Platform Designer tool or in HDL. In addition, GPIO2 and GPIO3 can be controlled though the ASC Output control block if desired. The GPIO1 pin can be used as the I²C write protect pin if this feature is selected. In this mode it becomes a dedicated input pin.

The GPIO pins require an external pull-up resistor tied to a power rail when used as outputs. The outputs can be pulled as high as 5.5 V. Unused output pins can be left floating.

HVOUT Pins

The HVOUT pins are N-Channel MOSFET drivers for generating a controlled power supply ramp. These pins can also be programmed as open-drain logic outputs. When used as a MOSFET driver, place a 10-100 Ohm series resistor in the gate path. Place the resistor as close to the MOSFET gate lead as possible. This will help prevent high-speed parasitic oscillations. When used as open-drain outputs, the output requires an external pull-up resistor. HVOUTs in open-drain mode can be pulled up to a max of 13 V. Unused HVOUTs can be left floating or connected to ground.

GPIO and HVOUT Safe State

Be sure to review the Safe-State of the GPIO and HVOUT pins to insure the connected device has the correct behavior. The safe-state of the GPIO and HVOUT pins is shown in Table 4. See the data sheet for more details.

Table 4. GPIO and HVOUT Safe-State Definitions

I/O	Safe-State
HVOUT1	Low
HVOUT2	Low
HVOUT3	Low
HVOUT4	Low
GPIO1	Low
GPIO2	Low
GPIO3	Low
GPIO4	Low
GPIO5	Low
GPIO6	Low
GPIO7[1]	Hi-Z
GPIO8	Hi-Z
GPIO9	Hi-Z
GPIO10	Low

1. GPIO7 is not bonded out on the QFN48 package ASC device.

Please note that if the Safe-state of a GPIO or HVOUT pin is "Low" then any external pull-up resistor will be overridden by the Safe-state during the power-up process of the Platform Manager 2 system. Please see DS1043, Platform Manager 2 Data Sheet for more information about the Platform Manager 2 system power-up process.

VMON Pins

VMON pins are used for voltage monitoring. The VMON1 through VMON4 signals are differential and the remaining VMON signals (including HVMON) are single-ended. Connect the VMONx pins to the voltage being monitored, near the load side. For the differential signals the VMONGSx pins are required to be connected to ground. Tie the VMONGS lines close to the low side of the load being measured for accurate differential measurement. Unused VMON pins can be left floating or grounded. There is an internal impedance of 55-75 kOhm to ground on the VMON pins.

When monitoring a voltage or current from a higher voltage source, only the HVIMONN_HVMON and HVIMONP pins can be connected directly to a voltage source which is greater than 5.9 Volts. A voltage divider circuit or other means of isolation is required if using VMON1-9 to monitor a voltage source greater than 5.734 Volts (this is the maximum trip point setting).

TRIM Pins

Trim pins are special function pins from the TRIM DACs. These pins are used in conjunction with the internal TRIM blocks and use a set of external resistors to bias the reference or feedback node of power supplies. Care should be taken in layout to minimize the parasitic board trace capacitance. TRIM resistors should be located near the DC-DC power supply that is under TRIM control. TRIM pins are associated with a specific VMON input. TRIM1 is associated with VMON1; TRIM2 is associated with VMON2, and so on. Unused TRIM pins can be left floating.

FPGA PIO Pins

The PIO pins of the FPGA section support various logic standards, both single-ended and differential. There are four PIO banks and each bank has an associated set of VCCIO power supply and ground pins. All PIOs in a given bank are referenced to the VCCIO for that bank. When configured as outputs the PIO output standard must match the VCCIO for that bank (i.e. LVCMOS25 outputs must reside in a bank which has VCCIO of 2.5 V). If a PIO is not programmed for use in the software, that pin defaults to an input pin with an internal pull-down resistor. Unused pins can be left floating or tied to GND. The voltage level at the FPGA PIO pin must not exceed 3.6 V. The average DC current drawn by FPGA PIO pins should not exceed 8 mA per pin.

Checklist

	Platform Manager 2 Hardware Checklist Item	OK	N/A
1.1	Core Supply VCC and VCCA are at 3.3 V		
1.2	Ferrite bead isolating VCCA from the VCC supply		
1.3	I/O power supply VCCIO0 and VCCIO1 at 3.3 V		
1.4	I/O Power supply VCCIO2 and VCCIO3 at 1.2 V to 3.3 V		
1.5	All Ground pins connected to ground plane.		
1.6	External ASC has a common ground reference level.		
1.7	External ASC has similar voltage levels.		
1.8	Power Estimation		
2.1	Configuration options		
2.2	Pull-up on PROGRAMN		
2.3	Pull-up on SPI mode pins		
2.4	Pull-up on I^2C mode pins		
2.5	JTAG logic levels at 3.3 V and proper pull-up or pull-down resistors used.		
2.6	PROGRAMN high-to-low transition time period is larger than the VCC (min) to INITN rising edge time period.		
3.1	RESETb connection from all ASCs to FPGA section or MachXO2.		
3.2	ASCCLK connection only from ASC0 for MachXO2 design. No ASCCLK connections on LPTM21 designs.		
3.3	Connect external ASC pins WDAT, RDAT, and WRCLK to Platform Manager 2 FPGA section or MachXO2 PIO pins.		
3.4	SDA_M and SCL_M connected to SDA_S and SCL_S pins on an LPTM21 project.		
3.5	Connect ASC SDA and SCL pins to LPTM21 SDA_M and SCL_M pins or to MachXO2 SDA/PCLKC0_0 and SCL/PCLKT0_0 pins.		
3.6	Connect ASC GPIO1 to FPGA PIO pin if using I^2C write protect feature.		
3.7	Correct resistor size installed on ASC I2C_ADDR pin for external ASC devices.		
3.8	The die pad of all external ASC devices connected to ground.		
4.1	Pull up resistors on GPIO pins configured as outputs. Pull-up to 5.5 V or less.		
4.2	Series resistor installed near gate for HVOUT pin used in MOSFET driver mode.		
4.3	Pull up resistors on HVOUT pins configured as Open-Drain outputs. Pull-up to 13 V or less.		
4.4	Safe-state of GPIO and HVOUT pins is correct for design.		
4.5	VMONGS pins connected to ground for VMON1-VMON4.		
4.6	Only HVIMONN_HVMON and HVIMONP pins connected directly to voltages over 5.9 V.		
4.7	Trim output 1 matched up to VMON input 1, TRIM2 to VMON2, and others.		
4.8	Maximum voltage at FPGA PIO pins is 3.6 V or less.		
4.9	Average current drawn by FPGA PIO pins should not exceed 8 mA per pin.		

Technical Support Assistance

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Revision History

Date	Version	Change Summary
March 2015	1.1	General updates: — Changed document title to L-ASC10 and Platform Manager 2 Hardware Checklist. — Added references to L-ASC10. — Removed references to LPTM20. — Updated links to DS1042 and DS1043.
		Updated I^2C Address Pin section. Clarified I2C_ADDR pin usage in Table 3, Resistor Sizes for External ASC I2C_ADDR Pin.
		Updated Appendix: System Connections Examples section. Clarified I2C_ADDR pin usage in the following figures: — Figure 1, LPTM21 System Connections Example — Figure 2, MachXO2 and ASC System Connections Example Removed the LPTM20 System Connections Example figure.
November 2013	01.0	Initial release.

Appendix: System Connections Examples

Figure 1. LPTM21 System Connections Example

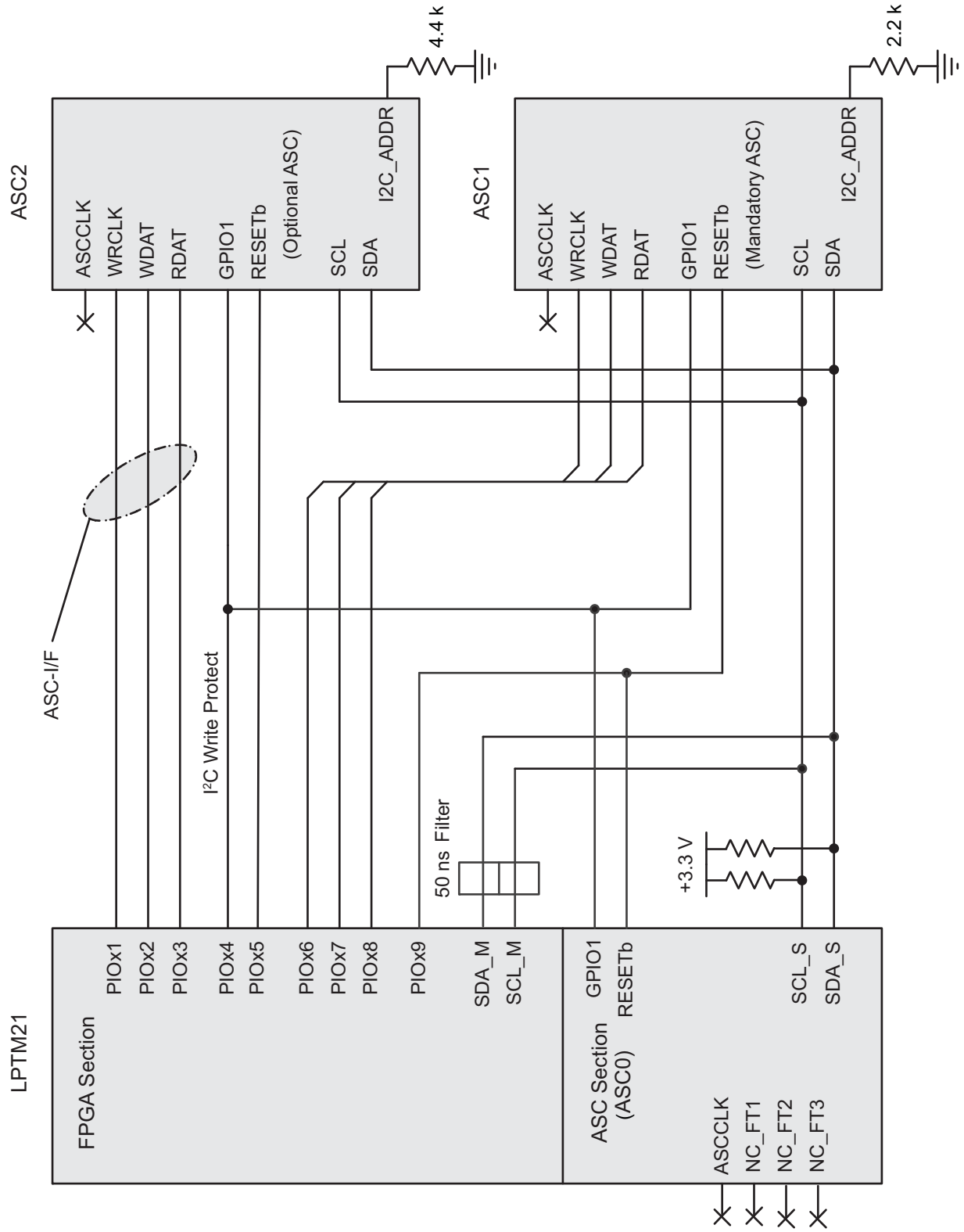

Figure 2. MachXO2 and ASC System Connections Example