MachXO3 Hardware Checklist

Technical Note

FPGA-TN-02061-1.3

March 2020

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
PCB	Printed Circuit Board
I^2C	Inter-Integrated Circuit
SRAM	Static Random Access Memory
NVCM	Non Volatile Configuration Memory

1. Introduction

When designing complex hardware using the MachXO3™ PLD, specifically the L version, designers must pay special attention to critical hardware configuration requirements. This technical note steps through these critical hardware requirements related to the MachXO3L/LF devices. This document does not provide detailed step-by-step instructions but gives a high-level summary checklist to assist in the design process.

The MachXO3L/LF ultra-low power, instant-on, non-volatile PLDs are available in two versions C and E devices. C devices have an internal linear voltage regulator which supports external V_{CC} supply voltages of 3.3 V or 2.5 V. E devices only accept 1.2 V as the external V_{CC} supply voltage. With the exception of power supply voltage, both types of devices (C and E) are functionally and pin compatible with each other.

This technical note assumes that the reader is familiar with the MachXO3L/LF device features as described in the MachXO3 Family Data Sheet (FPGA-DS-02032).

The critical hardware areas covered in this technical note include:

- Power supplies as they relate to the MachXO3L/LF supply rails and how to connect them to the PCB and the associated system.
- Configuration and how to connect the configuration mode selection for proper power up configuration.
- Device I/O interface and critical signals.

Important: Refer to the following documents for detailed recommendations.

- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02083)
- Power and Thermal Estimation and Management for MachXO3 Devices (FPGA-TN-02059)
- MachXO3 sysIO Usage Guide (FPGA-TN-02056)
- Implementing High-Speed Interfaces with MachXO3 Devices (FPGA-TN-02057)
- MachXO3 Programming and Configuration Usage Guide (FPGA-TN-02055)
- Using Hardened Control Functions in MachXO3 Devices (FPGA-TN-02063)

2. Power Supply

The V_{CC} and V_{CCIO0} power supplies determine the MachXO3L/LF internal *power good* condition. These supplies need to be at a valid and stable level before the device can become operational. In addition, there are five (V_{CCIO1} to V_{CCIO5}) supplies that power the remaining I/O banks. Table 2.1 shows the power supplies and the appropriate voltage levels for each.

Refer to the MachXO3 Family Data Sheet (FPGA-DS-02032) for more information on the voltage levels.

Table 2.1. Power Supply Description and Voltage Levels

Supply	Voltage (Nominal Value)	Description
V_{CC}	1.2 V	Core power supply for 1.2 V devices (E)
	2.5 V/3.3 V	Core power supply for 2.5 V/3.3 V devices (C)
V_{CCIOx}	1.2 V to 3.3 V	Power supply pins for I/O Bank x. There are up to five I/O banks.

3. Power Estimation

Once the MachXO3L/LF device density, package and logic implementation is decided, power estimation can be performed using the Power Calculator tool which is provided as part of the Lattice Diamond® design software. While performing power estimation, the user should keep two specific goals in mind.

- Power supply budgeting should be considered based on the maximum of the power-up in-rush current, configuration current or maximum DC and AC current for a given system environmental condition.
- The ability of the system environment and MachXO3L/LF device packaging to support the specified maximum operating junction temperature.

By determining these two criteria, system design planning can take the MachXO3L/LF power requirements into consideration early in the design phase.

This is explained in Power Estimation and Management for MachXO3 Devices (FPGA-TN-02059).

4. Configuration Considerations

MachXO3L/LF devices contain two types of memory, SRAM and either NVCM in MachXO3L devices or Flash in MachXO3LF devices. SRAM is volatile memory and contains the active configuration. NVCM or Flash is non-volatile memory that provides on-chip storage for the SRAM configuration data.

The MachXO3L/LF includes multiple programming and configuration interfaces:

- 1149.1 JTAG
- Self-download
- Slave SPI
- Master SPI
- Dual Boot
- I^2C
- WISHBONE bus

For ease of prototype debugging it is recommended that every PCB should have easy access to the programming and configuration pins.

The configuration logic arbitrates access from the interfaces by the following priority. When higher priority ports are enabled, NVCM or Flash access by lower priority ports will be blocked.

- JTAG Port
- Slave SPI Port (SN low activates the SPI port)
- I^2C Primary Port

Note: Erased device have all programming and configuration ports enabled by default. When the device is erase ensure SN and ProgramN are not driven low.

For a detailed description of the programming and configuration interfaces please refer to MachXO3 Programming and Configuration Usage Guide (FPGA-TN-02055).

The use of external resistors is always needed if the configuration signals are being used to handshake with other devices. Pull-up and pull-down resistor (4.7K) recommendations on different configuration pins are listed below.

Table 4.1. Default State of the sysCONFIG Pins

Pin Name	Pin Function (Configuration Mode)	Pin Direction (8-Bit Size)	Data In Bits that Get Masked (9-Bit Size)
PROGRAMN	PROGRAMN	Input with weak pull-up, external pull-up to V_{CCIO0}.	PROGRAMN
INITN	I/O	I/O with weak pull-up.	User-defined I/O
DONE	I/O	I/O with weak pull-up, external pull-up to V_{CCIO0}.	User-defined I/O
MCLK/CCLK	SSPI	Input with weak pull-up. MCLK function requires external 1k Ω pull-up.	User-defined I/O
SN	SSPI	Input with weak pull-up, external pull-up to V_{CCIO2}.	User-defined I/O
SI/SPISI	SSPI	Input	User-defined I/O
SO/SOSPI	SSPI	Output	User-defined I/O
CSSPIN	I/O	I/O with weak pull-up, external pullup to V_{CCIO2}.	User-defined I/O
SCL	I^2C	Bi-Directional open drain, external pull.	User-defined I/O
SDA	I^2C	Bi-Directional open drain, external pull.	User-defined I/O
TDI	TDI	Input with weak pull-up.	TDI
TDO	TDO	Output with weak pull-up.	TDO
TCK	TCK	Input. Recommended 4.7k Ω pull-down.	TCK
TMS	TMS	Input with weak pull-up.	TMS
JTAGENB	I/O	Input with weak pull-down.	I/O

5. Master SPI

When configuring from an external SPI Flash, ensure that the SPI Flash V_{CC} and the MachXO3L/LF V_{CCIO2} are at the same level. Ensure that the SPI Flash V_{CC} is at the recommended operating level.

6. PROGRAMN Initial Power Considerations

The MachXO3L/LF PROGRAMN is permitted to become a general purpose I/O. The PROGRAMN only becomes a general purpose I/O after the configuration bitstream is loaded. When power is applied to the MachXO3L/LF the PROGRAMN input performs the PROGRAMN function. It is critical that any signal input to the PROGRAMN have a high-to-low transition period that is longer than the V_{CC} (min) to INITN rising edge time period. Transitions faster than this time period prevent the MachXO3L/LF from becoming operational. Refer to the description of PROGRAMN in MachXO3 Programming and Configuration Usage Guide (FPGA-TN-02055).

7. Pin-out Considerations

The MachXO3L/LF PLDs support many applications with high-speed interfaces. These include various rule-based pin-outs that need to be understood prior to the implementation of the PCB design. The pin-out selection must be completed with an understanding of the interface building blocks of the FPGA fabric. These include IOLOGIC blocks such as DDR, clock resource connectivity, and PLL usage. Refer to Implementing High-Speed Interfaces with MachXO3 Devices (FPGA-TN-02057) for rules pertaining to these interface types.

8. True-LVDS Output Pin Assignments

True-LVDS outputs are on the top bank (Bank 0) of the MachXO3L/LF-1300 and higher density devices. When using the LVDS outputs, a 2.5 V or 3.3 V supply needs to be connected to the Bank 0 V_{CCIO} supply rails. Refer to MachXO3 sysIO Usage Guide (FPGA-TN-02056) for more information on this.

9. PCI Clamp Pin Assignment

PCI clamps are available on the bottom I/O bank (Bank 2) of the MachXO3L/LF-1300 and higher density devices. When the system design calls for PCI clamp, these pins should be assigned to I/O Bank 2. For the clamp characteristic, refer to the IBIS buffer models either on the Lattice web site or in the Lattice Diamond design software.

10. Back Leakage Considerations

When the part is powered down, there are some situations where current is still present due to active I/O, similar to a hot socketing situation. This can potentially cause the internal voltage supply to rise to power-on reset levels and start device operation. To mitigate for this back leakage current, it is recommended to add a weak pulldown resistor to the voltage supply. This should be set to value sufficient to keep the voltage below the POR trip point of the device with the worst case I/O back leakage current applied.

11. Checklist

	MachXO3L Hardware Checklist Item	OK	N/A
1	Power Supply		
1.1	Core Supply VCC at 1.2 V		
1.2	Core Supply VCC at 2.5 V or 3.3 V		
1.3	I/O power supply VCCIO 0-5 at 1.2 V to 3.3 V		
1.4	Power Estimation		
2	Configuration		
2.1	Configuration options		
2.2	Pull-up on PROGRAMN, INITN, DONE		
2.3	Pull-up on SPI mode pins		
2.4	Pull-up on I^2C mode pins		
2.5	JTAG default logic levels		
2.6	PROGRAMN high-to-low transition time period is larger than the VCC (min) to INITN rising edge time period		
3	I/O pin assignment		
3.1	True LVDS pin assignment considerations		
3.2	PCI clamp requirement considerations		

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.3, March 2020

Section	Change Summary
All	• Changed document number from TN1291 to FPGA-TN-02061. • Updated document template.
Disclaimers	Added this section.
Back Leakage Considerations	Added this section.

Revision 1.2, March 2016

Section	Change Summary
Master SPI	Minor editorial correction.
Technical Support Assistance	Updated contact information.

Revision 1.1, March 2015

Section	Change Summary
All	Product name/trademark adjustment. Included MachXO3LF device.

Revision 1.0, April 2014

Section	Change Summary
All	Initial release

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