

Overview of ORCA Series 4 I/O Features

In today's world of high-performance networking systems, designers require flexible, high-performance programmable solutions. Lattice's ORCA Series 4 FPGAs provide next generation performance. Especially critical for overall system performance and functionality are the capabilities of the I/O. The major I/O features of the ORCA Series 4 platform are:

- Support for multiple single-ended I/O standards including: LVTTTL, LVCMOS2, LVCMOS18, GTL, GTL+, HSTL Class I/III/IV, SSTL3/2 Class I/II, PECL, 3 V PCI.
- Support for multiple differential I/O standards including LVPECL and low-voltage differential signaling (LVDS).
- Programmable integrated LVDS termination resistor.
- Double data rate (DDR) interfaces that support 311 MHz, 622 Mbits/s data flow.
- Zero bus turnaround (*ZBT**) interface running at 200 Mbits/s.
- 420 MHz I/O performance to support UTOPIA 4 standards.
- Input/output shift register to divide/multiply data rates by either 2X or 4X.

Table 1. Series 4 Programmable I/O Standards

Standard	VDDIO (V)	VREF (V)	Interface Usage
LVTTTL	3.3	NA	General purpose.
LVCMOS2	2.5	NA	
LVCMOS1.8	1.8	NA	
PCI	3.3	NA	PCI.
LVDS	2.5	NA	Point-to-point and multidrop backplanes, high noise immunity.
Bused-LVDS	2.5	NA	Network backplanes, high noise immunity, bus architecture backplanes.
LVPECL	3.3	NA	Network backplanes, differential 100 MHz+ clocking, optical transceiver, high-speed networking.
PECL	3.3	2.0	Backplanes.
GTL	3.3	0.8	Backplane or processor interface.
GTL+	3.3	1.0	
HSTL-class I	1.5	0.75	High-speed SRAM and networking interfaces.
HTSL-class III and IV	1.5	0.9	
SSTL3-class I and II	3.3	1.5	Synchronous DRAM interface.
SSTL2-class I and II	2.5	1.25	

Note: interfaces to DDR and *ZBT* memories are supported through the interface standards shown above.

* *ZBT* is a trademark of Integrated Device Technology Inc.

Overview of I/O Standards

The following overview reviews the many I/O standards made available to designs with the Series 4 programmable I/O cell. It also summarizes the specifications for each interface standard.

Traditional I/O Standards

LVTTTL

LVTTTL is a general-purpose standard, defined by JEDEC standard JESD-8B (September 1999), *Interface Standard for Nominal 3.0 V/3.3 V Supply Digital Integrated Circuits*. This standard supports single-ended signaling in 3.3 V applications.

Table 2. . LVTTTL dc Operating Specifications

Parameter	Min	Typical	Max	Unit
VDDIO	3	3.3	3.6	V
VREF	—	—	—	V
VTT	—	—	—	V
VIH	2	—	VDDIO + 0.3	V
VIL	-0.5	—	0.8	V
VOH	2.4	—	—	V
VOL	—	—	0.4	V
IOH at VOH	-24, 12, 6	—	—	mA
IOL at VOL	12, 6, 3	—	—	mA

3.3 V PCI

PCI Local Bus Specification 2.2 Compliant for 3.3 V Operation supports up to 32-bit bus widths at both 33 MHz or 66 MHz.

A programmable PLL needs to be used to meet the 6 ns clock to out specification for 66 MHz PCI. Please refer to the Series 4 FPGA PLL Elements Technical Note TN1014 for PLL usage.

Table 3. . PCI dc Operating Specifications

Parameter	Min	Typical	Max	Unit
VDDIO	3	3.3	3.6	V
VREF	—	—	—	V
VTT	—	—	—	V
VIH	1.4	1.5	VDDIO + 0.3	V
VIL	-0.5	1	1.05	V
VOH	2.7	—	—	V
IOH at VOH	Tested per specified test conditions			mA
IOL at VOL	Tested per specified test conditions			mA

LVC MOS2

Low-voltage CMOS (LVC MOS2) is a general-purpose standard similar to LVC MOS. Defined by JEDEC standard JESD-8-5 (October 1995), 2.5 V \pm 0.2 V (normal range), and 1.8 V to 2.7 V (wide range) *Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits*, this standard supports single-ended signaling in 2.5 V applications.

Table 4 . LVC MOS2 dc Operating Specifications

Parameter	Min	Typical	Max	Unit
VDDIO	2.3	2.5	2.7	V
VREF	—	—	—	V
VTT	—	—	—	V
VIH	2	—	VDDIO + 0.3	V
VIL	-0.5	—	0.8	V
VOH	VDDIO - 0.2	—	—	V
VOL	—	—	0.2	V
IOH at VOH	-24, 12, 6	—	—	mA
IOL at VOL	12, 6, 3	—	—	mA

LVC MOS18

Low-voltage CMOS (LVC MOS18) is a general-purpose standard similar to LVC MOS. Defined by JEDEC standard JESD-8-7 (February 1997), 1.8 V \pm 0.15 V (normal range), and 1.7 V to 1.95 V (wide range) *Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits*, this standard supports single-ended signaling in 1.8 V applications.

Table 5. LVC MOS18 dc Operating Specifications

Parameter	Min	Typical	Max	Unit
VDDIO	1.7	1.8	1.9	V
VREF	—	—	—	V
VTT	—	—	—	V
VIH	2	—	VDDIO + 0.3	V
VIL	-0.5	—	0.8	V
VOH	VDDIO - 0.2	—	—	V
VOL	—	—	0.2	V
IOH at VOH	-24, 12, 6	—	—	mA
IOL at VOL	12, 6, 3	—	—	mA

High-Speed Single-Ended I/O Standards

GTL

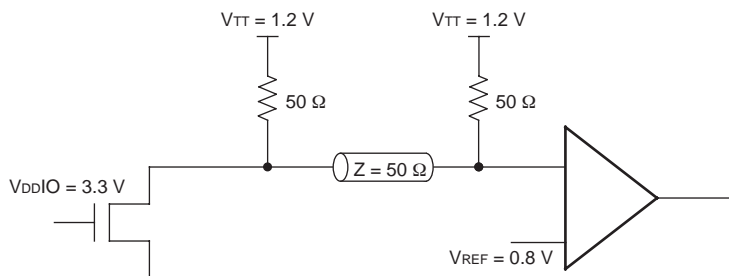
Gunning transceiver logic (GTL) is a standard for I/O pads developed to provide a high bus bandwidth of 100 MHz with low voltage swings and lower power dissipation. To guarantee signal with no reflections, GTL uses parallel termination connecting the line with characteristic impedance at both ends. GTL contains a reference receiver and an open-drain output. Following JEDEC standard JESD-8-3 (November 1993), it uses a typical input reference voltage of 0.8 V with a 1.2 V board termination.

Table 6. GTL dc Operating Specifications

Parameter	Condition	Min	Typical	Max	Unit
VDDIO	—	3	3.3	3.6	V
VREF	—	0.74	0.8	0.86	V
VTT	—	1.14	1.2	1.26	V
VIH	—	0.79	0.85	—	V
VIL	—	—	0.75	—	V
VOH	—	—	—	—	V
VOL	IOL = 40 mA	—	0.2	0.4	V
IOH	—	—	—	—	mA
IOL	VOL = 0.4 V	32			mA
IOL	VOL = 0.2 V			40	mA

Note: VTT=VREF

Figure 1. GTL Termination Scheme



GTL+

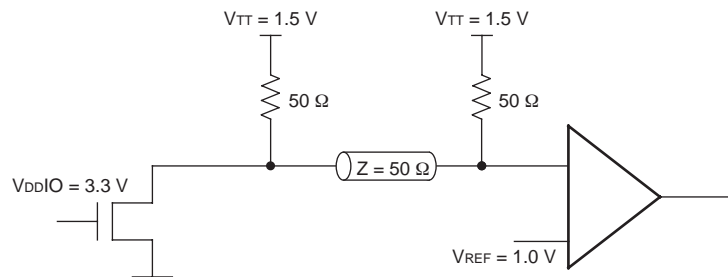
Gunning transceiver logic plus (GTL+) is a standard similar to GTL. However, it uses a typical input reference voltage of 1.0 V with a 1.5 V board termination.

Table 7. GTL+ dc Operating Specifications

Parameter	Condition	Min	Typical	Max	Unit
VDDIO	—	3	3.3	3.6	V
VREF	—	0.88	1	1.12	V
VTT	—	1.35	1.5	1.65	V
VIH	—	0.98	1.2	—	V
VIL	—	—	0.8	1.02	V
VOH	—	—	—	—	V
VOL	IOL = 32 mA	0.3	0.45	0.6	V
IOH	—	—	—	—	mA
IOL	VOL = 0.4 V	36			mA
IOL	VOL = 0.3 V			48	mA

Note: VTT=VREF

Figure 2. GTL+ Termination Scheme



HSTL Class I, III, IV

HSTL (high-speed transceiver logic) -JEDEC standard JESD 8-6 (August 1995), is a technology-independent interface standard for digital integrated circuits. It is a voltage scalable and technology independent I/O structure. The I/O structures required by this standard contains a reference receiver (which is typically 50% of the VDDIO) and an open-drain output described as a VREF for single-ended inputs and outputs using output power supply inputs (VDDIO) that may differ from those operating the device itself. This buffer is meant to receive high-speed transceiver logic (HSTL) signal levels, HSTL also allow chips with different power supplies to easily communicate with each other.

Table 8. HTSL Class I dc Operating Specifications

Parameter	Condition	Min	Typical	Max	Unit
VDDIO	—	1.4	1.5	1.8	V
VREF	—	0.68	0.75	0.9	V
VTT ¹	—	—	0.75	—	V
VIH	—	VREF + 100 mV	0.85	VDDIO + 0.3	V
VIL	—	-0.3	0.65	VREF - 100 mV	V
VOH ²	IOH > 8 mA	1	1.1	—	V
VOL	IOL > -8 mA	—	—	0.4	V

1. 50% VDDIO.
 2. VDDIO - 400 mV.

Figure 3. HTSL Termination Scheme

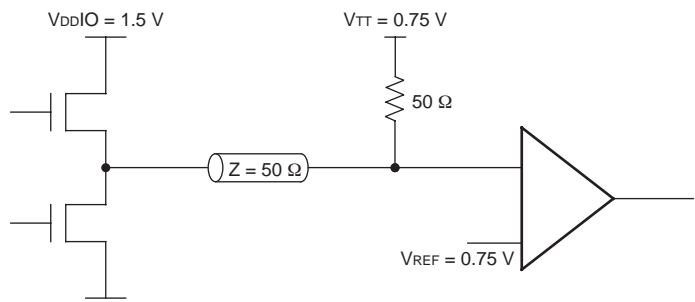


Table 9. HSTL Class III dc Operating Specifications

Parameter	Condition	Min	Typical	Max	Unit
VDDIO	—	1.4	1.5	1.6	V
VREF	—	0.81	0.9	1.0	V
VTT ¹	—	—	1.5	—	V
VIH	—	VREF + 100 mV	0.65	VDDIO + 0.3	V
VIL	—	-0.3	—	.VREF - 100 mV.	V
VOH ²	IOH > 8 mA	1	1.1	—	V
VOL	IOL > -24 mA	—	—	0.4	V

- 1. VDDIO=VTT
- 2. VDDIO - 400 mV.

Figure 4. HTSL Class III Termination Scheme

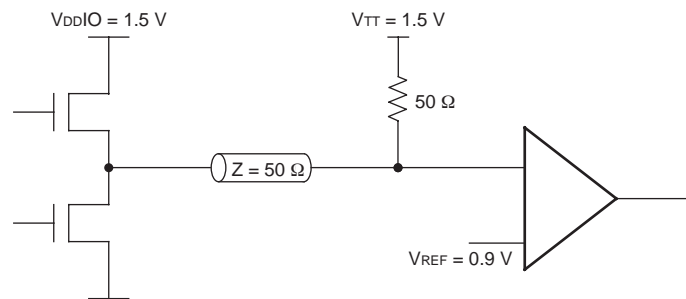
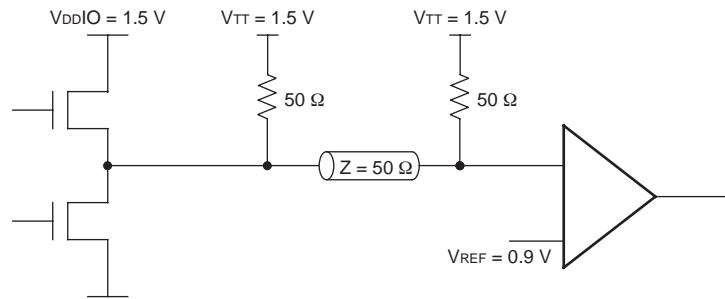


Table 10. HSTL Class IV dc Operating Specifications

Parameter	Condition	Min	Typical	Max	Unit
VDDIO	—	1.4	1.5	1.6	V
VREF	—	0.81	0.9	1.0	V
VTT ¹	—	—	0.75	—	V
VIH	—	VREF + 100 mV	0.85	VDDIO + 0.3	V
VIL	—	-0.3	0.65	VREF - 100 mV	V
VOH ²	IOH > 8 mA	VDDIO - 400 mV	—	—	V
VOL	IOL > -48 mA	—	—	0.4	V

- 1. 50% VDDIO.
- 2. VDDIO - 400 mV.

Figure 5. HSTL Class IV Termination Scheme



SSTL3

This standard is a noninverting bidirectional buffer designed to comply with the JEDEC standard JESD8-8 (August 1996) standard for Stub Series Terminated Logic (SSTL) operating at 3.3 V. The standard is intended to improve operation in situations where busses must be isolated from relatively large stubs. External resistors provide this isolation and also reduce the on-chip power dissipation of the drivers. Busses may be terminated by resistors to an external termination voltage (V_{TT}). The standard utilizes a differential amplifier input stage and a push-pull output stage. The standard defines a reference voltage V_{REF} which is used at the receivers as well as a voltage V_{TT} to which the termination resistors are connected.

Table 11. SSTL3 Class I dc Operating Specifications

Parameter	Condition	Min	Typical	Max	Unit
VDDIO	—	3	3.3	3.6	V
VREF	—	1.3	1.5	1.7	V
V_{TT}^1	—	1.3	1.5	1.7	V
V_{IH}	—	$V_{REF} + 200\text{ mV}$	—	$V_{DDIO} + 0.3$	V
V_{IL}	—	-0.3	—	$V_{REF} - 200\text{ mV}$	V
V_{OH}	—	$V_{REF} + 600\text{ mV}$	2.1	—	V
V_{OL}	—	—	0.9	$V_{REF} - 600\text{ mV}$	V
I_{OH}	$V_{OH} = 1.9\text{ V}$	-8	—	—	mA
I_{OL}	$V_{OL} = 0.7\text{ V}$	8	—	—	mA

1. $V_{TT} = V_{REF} + 50\text{ mV}$.

Figure 6. SSTL3 Class I Termination Scheme

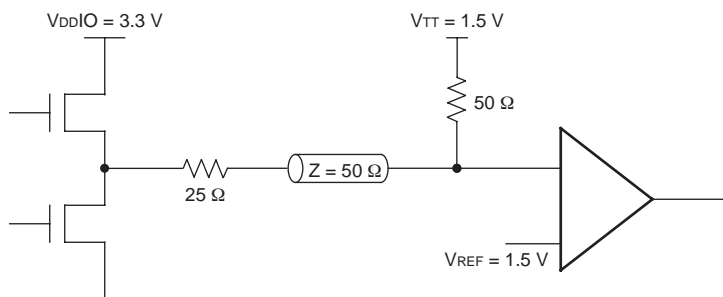
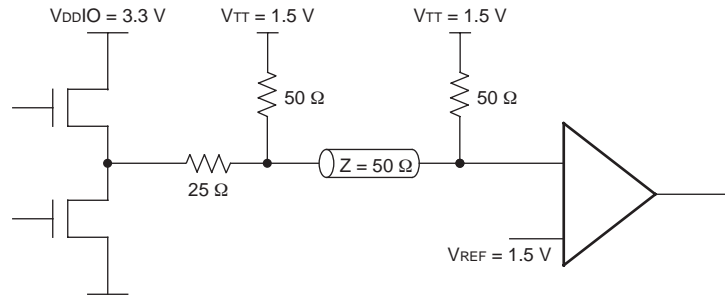


Table 12. SSTL3 Class II dc Operating Specifications

Parameter	Condition	Min	Typical	Max	Unit
VDDIO	—	3	3.3	3.6	V
VREF	—	1.3	1.5	1.7	V
VTT ¹	—	1.3	1.5	1.7	V
VIH	—	VREF + 200 mV	1.9	VDDIO + 0.3	V
VIL	—	-0.3	1.1	VREF - 200 mV	V
VOH	—	VREF + 800 mV	2.3	—	V
VOL	—	—	0.7	VREF - 800 mV	V
IOH	VOH = 2.1 V	-16	—	—	mA
IOL	VOL = 0.5 V	16	—	—	mA

1. VTT = VREF + 50mV.

Figure 7. SSTL3 Class II Termination Scheme



SSTL2

SSTL2 is a standard similar to SSTL3. However, it operates in the SSTL2 logic switching range of 0 V to 2.5 V. The I/O are designed to comply with the JEDEC standard JESD8-9 (September 1998) *Standard for Stub Series Terminated Logic (SSTL) Operating at 2.5 V*.

Table 13. SSTL2 Class I dc Operating Specifications

Parameter	Condition	Min	Typical	Max	Unit
VDDIO	—	2.3	2.5	2.7	V
VREF ¹	—	1.15	1.25	1.35	V
VTT ²	—	1.11	1.25	1.39	V
VIH	—	VREF + 0.18 V	1.43	VDDIO + 0.3	V
VIL	—	-0.3	—	VREF - 0.18 V	V
VOH	—	VTT + 0.57 V	1.85	—	V
VOL	—	—	0.65	VTT - 0.57 V	V
IOH	VOH = 1.68 V	-7.6	—	—	mA
IOL	VOL = 0.54 V	7.6	—	—	mA

- 1. 50% VDDIO.
- 2. VREF ± 0.04 V.

Figure 8. SSTL2 Class I Termination Scheme

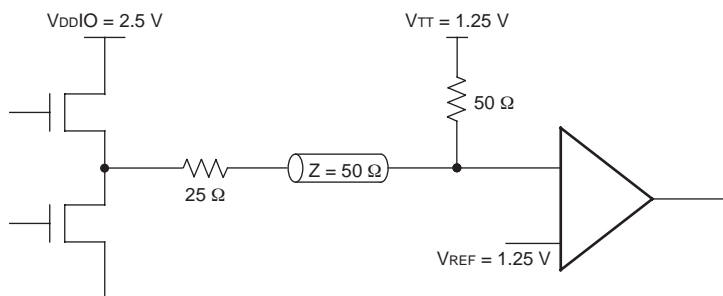
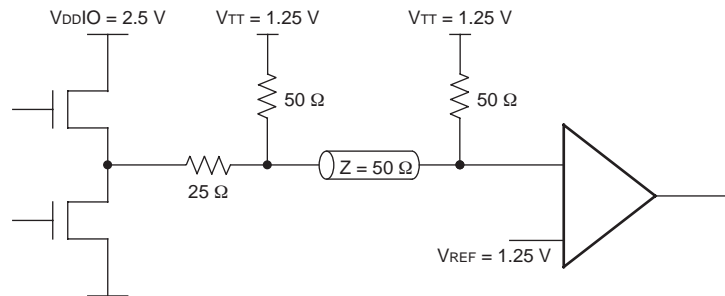


Table 14. SSTL2 Class II dc Operating Specifications

Parameter	Condition	Min	Typical	Max	Unit
VDDIO	—	2.3	2.5	2.7	V
VREF ¹	—	1.15	1.25	1.35	V
VTT ²	—	1.11	1.25	1.39	V
VIH ³	—	VREF - 0.18 V	1.43	VDDIO + 0.3	V
VIL ⁴	—	-0.3	1.07	VREF - 0.18 V	V
VOH ⁵	—	VTT + 0.76 V	2.05	—	V
VOL ⁶	—	—	0.45	VTT - 0.76 V	V
IOH	VOH = 1.87 V	-15.2	—	—	mA
IOL	VOL = 0.35 V	15.2	—	—	mA

- 1. 50% VDDIO.
- 2. VREF ± 0.04 V.

Figure 9. SSTL2 Class II Termination Scheme



PECL

Pseudo-emitter coupled logic (PECL) is a well-known bipolar circuit technique which is used extensively in high-speed systems. Its main attractions are low noise, good capacitive drive capability, and very high speed. Emitter-coupled logic (ECL) is also capable of driving low-impedance lines with single-ended signals. Since most ECL circuits are manufactured with a bipolar technology, the main drawback with ECL logic is its very high power consumption. The problem of interfacing TTL and ECL levels is that TTL levels are positive and ECL levels are negative. CMOS ECL buffers operate from a single power supply, either +3.3 V or -3.3 V, depending on the system. A chip containing both ECL and TTL buffers can communicate with true TTL levels and with PECL levels. These are ECL levels referenced to VDD (3.3 V nominal).

Table 15. PECL dc Operating Specifications

Parameter	Min	Typical	Max	Unit
VDDIO	3	3.3	3.6	V
VREF	—	2.0	—	V
VTT ¹	1	1.3	1.6	V
VIH ²	-1.16	-1	-0.88	V
VIL ²	-1.81	-1.65	-1.47	V
VOH ²	-1.02	-0.95	-0.88	V
VOL ²	-1.81	-1.7	-1.62	V
I _{IH}	—	—	—	mA
I _{IL}	—	—	—	mA

1. V_{DDIO} - 2V.

Differential I/O Standards

LVDS

LVDS is used in high-speed systems as a reliable means to communicate using very low voltage swings (typically 350 mV). Its low swing and current mode driver outputs create low noise and low power consumption. LVDS is less susceptible to common-mode noise than single-ended I/O. Noise is equally coupled to both differential leads as common-mode that is easily rejected by the receivers. The current-mode drivers are also less prone to ringing and switching spikes also reducing noise. The low-voltage swings allow for fast switching and also migrate well across many power operating levels. Compliant to *ANSI*/TIA/EIA†-644* standards, the *ORCA* LVDS driver output and receiver inputs meet all electrical specifications.

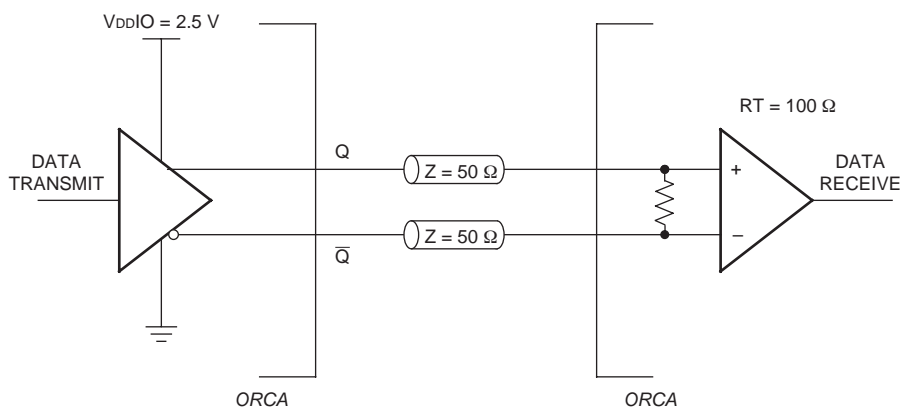
LVDS requires termination across input receivers. This is necessary to complete the current loop that must be matched with the signaling medium. To do this precisely, it is necessary to place the resistor as close as possible to the receiver input. A later section will discuss the *ORCA* advantage for differential termination.

Table 16. LVDS dc Operating Specifications

Parameter	Min	Typical	Max	Unit
VDDIO	2.3	2.5	2.7	V
Receiver Input Voltage	0	—	2.4	V
Differential Input Threshold	-100	—	100	mV
Output Common-mode Voltage ¹	1.125	1.25	1.357	V
Input Common-mode Voltage	0.2	1.25	2.2	V
Integrated Receiver Termination Resistor	90	100	110	W

1. Offset voltage.

Figure 10. LVDS Termination Scheme



* *ANSI* is a registered trademark of American National Standards Institute, Inc.

† *EIA* is a trademark of Electronic Industries Association.

LVPECL

Low-voltage positive-emitter coupled logic or low-voltage pseudo-emitter coupled logic (LVPECL) is used for differential data transmission which translates into a substantial improvement to the backplane data transfer rate. Since LVPECL is a differential mode transmission, the noise issue becomes less significant because the noise component is being included in the common mode signals. The small output voltage swing requirement makes high-speed data transfer possible with LVPECL. The output voltage swing maintains at about 760 mV.

Table 17. LVPECL dc Operating Specifications

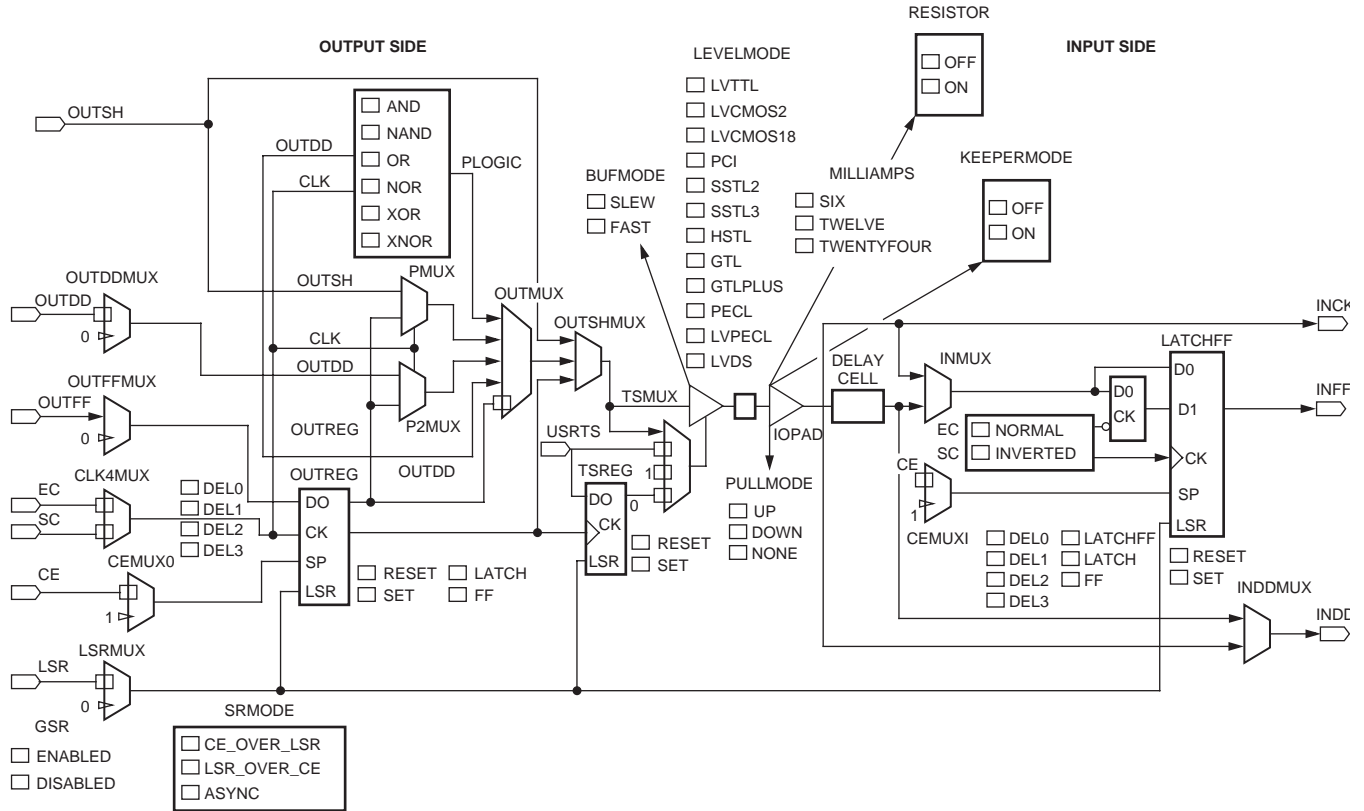
Parameter	Min	Typical	Max	Unit
VDDIO	3	3.3	3.6	V
Vp-p	600		900	mV
Input Common Mode	1.2		2.4	V
Receiver Termination Resistor	90	100	110	W
VIH	1.5		2.7	V
VIL	0.9		2.1	V
VOH ¹	2.2		2.4	V
VOL ¹	1.5	1.6	1.7	V

1. 750 mV differential swing.

Understanding and Using Series 4 I/O

The programmable I/O cell offers the mix of traditional I/O options of previous ORCA devices and also enables designers to select I/Os that meet many new communication standards permitting the device to hookup directly without any external interface translation. A programmable I/O cell (PIC) similar to previous generations of the ORCA family has been upgraded to meet the demands of high-speed communication designs. They support high-speed single-ended differential amplifier inputs with both open-drain and push-pull outputs. They are also designed to the high-speed specifications of LVDS and LVPECL differential signaling.

Figure 11. Series 4 PIO Image from ORCA Foundry



Each PIC contains up to four programmable I/O pads (PIO) and are interfaced through a common interface block to the FPGA array. The PIC is split into two pairs of I/O pads with each pair having independent clock enables, local set/ reset, and global set/reset.

On the input side, each PIO contains a programmable latch/flip-flop (FF) which enables very fast latching of data from any pad. The combination provides for very low setup requirements and zero hold times for signals coming on-chip. It may also be used to demultiplex an input signal, such as a multiplexed address/data signal, and register the signals without explicitly building a demultiplexer with a PFU.

On the output side of each PIO, an output from the PLC array can be routed to each output FF, and logic can be associated with each I/O pad. The output logic associated with each pad allows for multiplexing of output signals and other functions of two output signals.

The output FF, in combination with output signal multiplexing, is particularly useful for registering address signals to be multiplexed with data, allowing a full clock cycle for the data to propagate to the output. The output buffer signal can be inverted, and the 3-state control can be made active-high, active-low, or always enabled. In addition, this 3-state signal can be registered or nonregistered.

Output Drive Source Voltage (VDDIO) Banks

The flexible I/O features allow the user to select output drive source voltages to meet different high-speed interface requirements. The perimeter of the device is divided into eight distributed banks of PIOs. For each bank there are separate groups of VDDIO supply pins. The VDDIO supplies the correct output source drive voltage for a particular standard. The user must supply the appropriate power supply to the VDDIO pin. Within a bank, several I/O standards may be mixed as long as they use a common VDDIO. Table # highlights the compatible output drive source voltages that can be mixed within an I/O bank.

Table 18. IO Bank Designations

IO Bank Designation	Physical Location
VDDIO0	TL
VDDIO1	TC
VDDIO2	TR
VDDIO3	CR
VDDIO4	BR
VDDIO5	BC
VDDIO6	BL
VDDIO7	CL

Figure 12. ORCA High-Speed I/O Banks

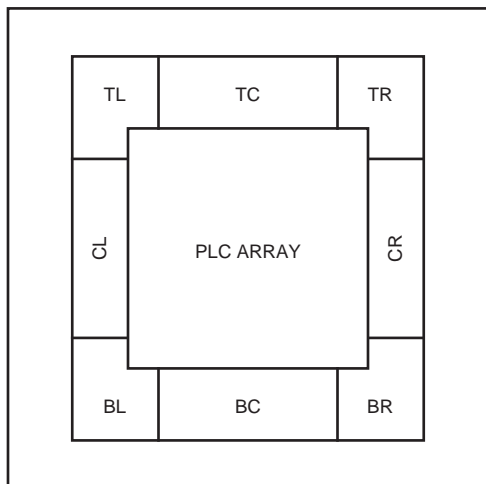


Table 19. VDDIO Compatibility

VDDIO Bank	Compatible Standards
3.3 V	LVTTTL, SSTL3-I, SSTL3-II, GTL, GTL+, PECL, LVPECL
2.5 V	LVDS, LVCMOS2, SSTL2-I, SSTL2-II
1.8 V	LVCMOS18
1.5 V	HSTL

Input Reference Voltage (VREF) Groups

Some interface standards require a specified threshold voltage known as VREF. I/O standards with a differential input buffer require such an input reference. The VREF is dedicated exclusively to a grouping of I/Os within a bank and cannot be intermixed with other signaling requiring other VREF voltages. Groups are subsets of the VDDIO banks. These groups are distributed, based on array size and package type, within each VDDIO bank. In these modes, where a particular VREF is required, the device is automatically programmed to dedicate a fixed I/O pin for the appropriate VREF, which must be supplied a voltage reference by the user. The VREF pad is no longer available to the user for general use. However, pins not requiring VREF can be mixed in the bank and the VREF pad can be used as a general I/O..

Table 20. Input Reference

Standard	VREF Group
GTL	0.8 V
GTL+	1.0 V
HSTL—Class I	0.75 V
HTSL—Class III & IV	0.9 V
SSTL3—Class I & II	1.5 V
SSTL2—Class I & II	1.25 V
PECL	2.0 V

Differential and Single-Ended Primary Clock Pins

The eight primary clock nets can be driven by programmable-dedicated I/O on each edge of the device. The primary clock is sourced from a dedicated input pin designed for fast, low-skew operation at the I/Os. These dedicated pads are located in pairs in the center of each side of the array and, if not utilized by the clock spine, can be used as general user I/O.

Two pins on each side or two pairs on each side for differential clocks are only dedicated when used with the primary clocks. If not used with the primary clocks, the pads become available for use as general I/O. The I/O can be programmed to any single-ended or differential I/O standard. When used with single-ended signals the associated pad, used when needed for differential signaling, is freed up for general I/O use. These associated pads are noted by P[T, B, R, L]CK[0, 1][T, C], where the edge is denoted by T, B, R, L, and 0 and 1 denote the particular primary net connected to the I/O. The T and C designates the differential signal of the I/O pair. This is illustrated in Figure #.

Phase-Lock Loop Inputs

A combination of eight dedicated and programmable PLLs are on-chip. Two PLLs are physically located in each corner of the device. All eight have a single-ended or differential pair of pads to provide the input clock to the PLL. These pins have the same flexibility to be used as general purpose I/O when not used with a PLL. They are designated by PLL_CK[0:7][TC]. Figure # illustrates the location of these pins. Table # outlines the pad relationship to each PLL.

Figure 13. Primary Clock and PLL Inputs

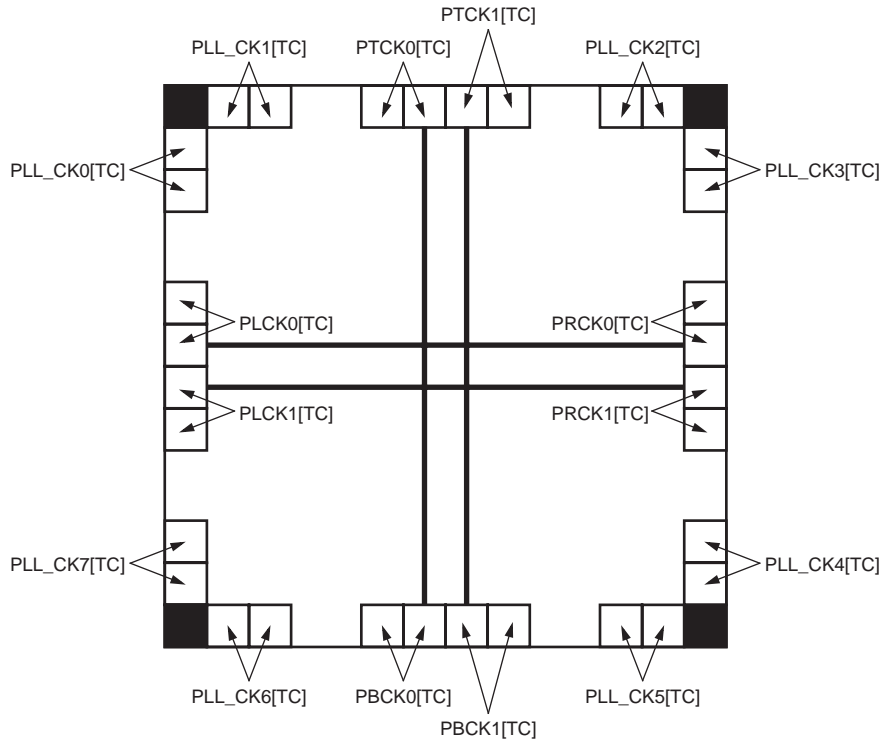


Table 21. PLL Clock Input Pins

Pin Name	PLL
PLL_CK0	HPPLL
PLL_CK1	PPLL
PLL_CK2	PPLL
PLL_CK3	PLL1 (1.554/2.048 MHz)
PLL_CK4	PLL2 (155.52 MHz)
PLL_CK5	PPLL
PLL_CK6	PPLL
PLL_CK7	HPPLL

Shared Control Signals on I/O Registers

The ORCA Series 4 architecture shares clock and control signals between two adjacent I/O pads. If I/O registers are used, incompatibilities may arise between devices when different clock or control signals are needed on adjacent package pins. This is because one device may allow independent clock or control signals on these adjacent pins, while the other may force them to be the same. There are two ways to avoid this issue.

- Always keep an open bonded pin (non-bonded pins do not count) between pins that require different clock or control signals. Note that this open pin can be used to connect signals that do not require the use of I/O registers to meet timing.
- Place and route the design in all target devices to verify they produce valid designs. Note that this method guarantees the current design, but does not necessarily guard against issues that can occur when design changes are made that affect I/O registers.

ORCA Series 4 LVDS/LVPECL I/O Solution

Introduction

Lattice's ORCA Series 4 devices provide the option of LVDS or LVPECL at every user I/O pin and in every speed-grade and device. The flexibility of the Series 4 incorporates differential pins that permit direct connections to the clock spines on all four sides of the devices. It also addresses high-speed system issues by adding the capability to hook up to all the programmable PLLs as well as the dedicated PLLs.

The implementation allows the flexibility for a designer to choose any I/O location on the entire device for LVDS or LVPECL. Designed in true differential fashion, there is no need to use any external devices for level adjustment or receiver termination. In LVDS/LVPECL modes, two pads are used per PIC. In this manner the A/B or C/D sites become a differential pair. The complimentary pads of a pair (B and D sites) are essentially invisible to the ispLEVER software excluding the placer algorithm. This allows the simulators to drive and report the true input and outputs reducing complex design issues.

It is appropriate to provide a background of LVDS, where it is used, the advantages of LVDS transmission, and guidelines in using it.

LVDS is defined in the *IEEE** 1596.3 and TIA/EIA-644 standards. The LVDS standards only provide the electrical characteristics, but not protocol functional specifications. LVDS is becoming one of the main transmission mediums for routers, switches, DSLAMs, and digital cross connects in networking equipment. The advantages of LVDS are as follows:

- High-speed transmission of data into the low Gbits/s range.
- Low EMI.
- Low voltage swing.
- Low power.
- High immunity to outside common mode noise and reflections. The low-voltage swing and low power allow a higher data bandwidth in networking systems. LVDS transmission may be point-to-point or multidrop/multipoint configurations. These configurations will be described in later sections.

The LVDS Standards

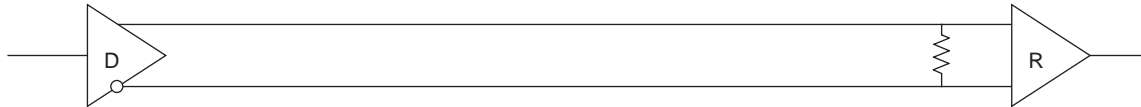
The TIA standard does recommend a maximum data rate of 655 Mbits/s and a theoretical maximum of 1.923 Gbits/s. From a practical point of view, LVDS is used in systems at a maximum data rate of 622 Mbits/s.

Bus LVDS is optimized for multipoint cable and backplane applications; bus LVDS differs from LVDS by providing the drive current to handle double terminations that are required by multipoint applications. However, bus LVDS provides lower-voltage swings than LVDS and fast transition times minimize power consumption and noise.

Point-to-Point LVDS Transmission

Point-to-point LVDS transmission is used where two devices directly communicate with LVDS signaling. This scenario is used for unidirectional, where a LVDS driver connects to a LVDS receiver through a single differential pair. Or a bidirectional scheme that connects a driver/receiver to a driver/receiver through a single differential pair sharing a half-duplex link for point-to-point communications and is used when interconnections must have superior signal quality.

Figure 14. Point-to-Point Bus Configuration

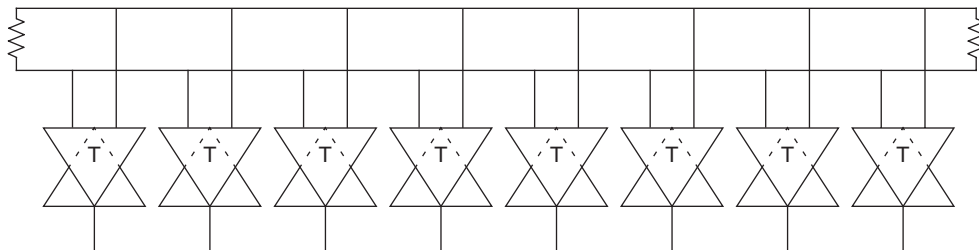


* IEEE is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Multidrop LVDS Transmission

Multidrop LVDS utilizes one driver or transmitter connecting to multiple receivers. Multidrop has a driver located at the start of the bus and is terminated on the far end of the bus. This link is very useful when data needs to be delivered to many locations.

Figure 15. Multidrop Bus Configuration



Easy Differential Termination

The LVDS standards typically require a 100 Ω termination resistor between the differential leads of the receiver for any type of LVDS communications. This termination provides the specified differential output voltage across the receiver input. The termination must be as close to the receiver as possible. This is necessary to prevent impedance mismatches to typical 50 Ω differential traces or cables which can produce unwanted reflections and electromagnetic interference (EMI). The ORCA solution includes a built-in programmable termination that eliminates the need to add external resistors to the board.

The ORCA LVDS easy termination allows the flexibility to add termination to every used LVDS receiver in the case of a point-to-point scheme. For multipoint/multidrop where termination is only necessary at the end of a bus, the programmability offers the designer the choice of only terminating a selected receiver. This integrated termination provides ideal matching, as well as reduces board clutter.

Termination matching is guaranteed by connecting a single 100 Ω resistor across the LVDS_R pin and VSS of the ORCA device. This single resistor is translated internally in the device and provides device matched 100 Ω termination to any programmed LVDS termination.

Enhanced Library Resources

The ORCA FPGA library includes all the elements supported by past families. These libraries are supported to ease migration of designs into new generations. However, the new library for Series 4 family must support the variety of new I/O standards. These standards are supported using enhancements of previously supported library elements. The IBM, OB6, and BMZ6 elements provide all the variations to moving the design into the I/O interface standards.

The following *Synplicity* Verilog†* example illustrates the use of the IBM and OB6 library elements to support the programmable SSTL2 I/O standards of the ORCA Series 4.

```
module IO10 (IN0,OUT0)
input IN0
output OUT0

IBM IN0_inst (IN0,S0) /* synthesis LEVELMODE="SSTL2" */ ;

OB6 OUT0_inst (S0,OUT0) /* synthesis LEVELMODE="SSTL2" */ ;

endmodule
```

A simple *VHDL†* attribute example would be as follows:

```
attribute LEVELMODE: string;
IBM1: IBM port map (I=>a, O=>b) ;
attribute LEVELMODE of IBM1: label is "SSTL2";
OB61: OB6 port map (I=>c, O=>d);
attribute LEVELMODE of OB61: label is "SSTL2";
```

Available I/O LEVELMODE attribute values:

- LVCMOS18
- LVCMOS2
- LVTTTL
- PCI
- PECL
- SSTL2
- SSTL3
- HSTL
- GTL
- GTLPLUS
- LVDS
- LVPECL

* *Synplicity* is a registered trademark of Synplicity, Inc.

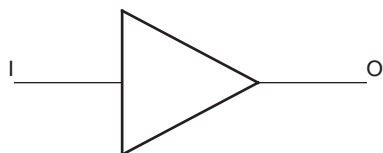
† *Verilog* and *VHDL* are trademarks of Cadence Design Systems, Inc.

Assigning Levelmode attributes without instantiated I/O

```
entity chip is
  port (
    clk : in std_logic;
    reset_n : in std_logic;
    d_in_aa, d_in_ab, d_in_ac, d_in_ad : in std_logic_vector(31 downto 0);
    err_inj_n : in std_logic;
    d_out_aa, d_out_ab, d_out_ac, d_out_ad : out std_logic_vector(31 downto
0);
    error_aa, error_ab, error_ac, error_ad : out std_logic;
    error_cnt : out std_logic_vector(7 downto 0)
  );

  attribute levelmode : string;
  attribute levelmode of d_out_aa : signal is "LVDS" ;
end chip;
```

Figure 16. IBM—Input Buffer

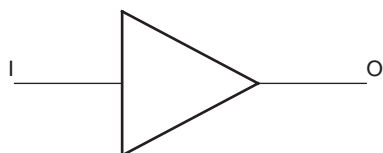


INPUTS: I, OUTPUTS = O.
 PINORDER: I O.
 ATTRIBUTES
 LEVELMODE: LVTTTL, LVCMOS18, LVCMOS2 (default),
 PCI, PECL, SSTL2, SSTL3, HSTL, GTL, GTLPLUS.
 DELAYMODE: 1, 0 (default).

Input delay mode is selected to delay the signal from the input pin. This ensures that a zero-hold time will be met by delaying the signal from the input pin. When enabled, this delay affects the INFF and INDD signals of each PIO, but not the clock input. The delay allows any signal to have a guaranteed zero hold time when input.

The OB6 element can be utilized to support the wide range of the Series 4 output buffers. This use supports either a push-pull or open-drain outputs to meet a particular interface standard. Similar to the input library instance, the output requirements are selected by the LEVELMODE attribute. This flexibility is limited by the required output source drive voltage for a particular standard which is supplied by a predefined VDDIO bank, as discussed previously.

Figure 17. OB6—Output Buffer



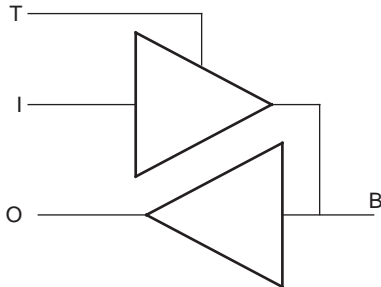
INPUTS: I.
 OUTPUTS: O.
 PINORDER: I O.
 ATTRIBUTES
 LEVELMODE: LVTTTL, LVCMOS18, LVCMOS2 (default),

PCI, PECL, SSTL2, SSTL3, HSTL, GTL, GTLPLUS.
 BUFMODE: SLEW (default), FAST.
 AMPSMODE: 6 (default), 12, 24.
 CLKMODE: SCLK (default), ECLK.

Note: BUFMODE and AMPSMODE are only supported when LEVELMODE = "LVTTTL" or "LVCMOS2."

In the case of LVTTTL or LVCMOS2 instances, the BUFMODE attribute allows the propagation delays of the output driver to be adjusted between slew and fast. By default the outputs are programmed to slew-limited mode to power concerns. The desired output drive strength can also be altered through the AMPSMODE attribute. The output buffer sink and source capabilities can be programmed to be 6 mA/3 mA, 12 mA/6 mA, or 24 mA/12 mA.

Figure 18. BMZ6—Bidirectional Buffer



INPUTS: I,T; OUTPUTS: O; IOPUTS: B.

PINORDER: B I T O.

ATTRIBUTES

LEVELMODE: LVTTTL, LVCMOS18, LVCMOS2 (default),
 PCI, PECL, SSTL2, SSTL3, HSTL, GTL, GTLPLUS.
 BUFMODE: SLEW (default), FAST.
 AMPSMODE: 6 (default), 12, 24.
 DELAYMODE: 1, 0 (default).
 CLKMODE: SCLK (default), ECLK.

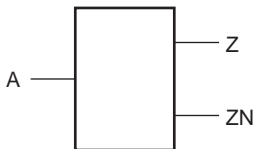
Note: BUFMODE and AMPSMODE are only supported when LEVELMODE = "LVTTTL" or "LVCMOS2."

Each PIO can be programmed with a KEEPERMODE feature. This element is user programmed for bus hold requirements. This mode retains the last known state of a bus when the bus goes into 3-state. It prevents floating busses and saves system power. The OBW and BMW library elements incorporates a weak pull-up or pull-down when 3-stated. When the 3-state signal is asserted, the device will hold a 1 or 0 based on the output state at 3-state. This element is available for LVTTTL and LVCMOS2 modes and attributes.

LVDS and LVPECL Library Support

Differential I/Os are supported through the use of a single input and output I/O element. The ILVDS element supports both LVDS and LVPECL. When instantiated for LVDS, there is no LEVELMODE attribute. The resistor is connected by default to the differential pads and can be disabled. This method of changing between LVPECL levels is also incorporated in the LVDS output I/O.

Figure 19. OLVDS



INPUTS: A.

OUTPUTS: Z, ZN.

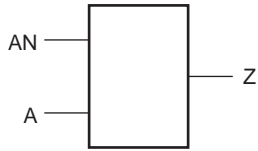
PINORDER: A, Z, ZN.

ATTRIBUTES

RESISTOR: FALSE (default), TRUE.

Note: If you wish to use the LVPECL buffer, pass the property "LEVELMODE=LVPECL" in both ILVDS and OLVDS elements.

Figure 20. ILVDS



INPUTS: A, AN.

OUTPUTS: Z.

PINORDER: A, AN, Z.

ATTRIBUTES

RESISTOR: FALSE (default), TRUE.

LVDS/LVPECL Examples

```
ILVDS ILVDS_INST (LVDS0_IN,LVDS1_IN, Z); Typical
ILVDS ILVDS_INST (LVDS0_IN,LVDS1_IN, Z) /* synthesis RESISTOR="FALSE" */;
    Disabled receiver termination
ILVDS ILVDS_INST (LVDS0_IN,LVDS1_IN, Z) /* synthesis LEVELMODE="LVPECL" */ ;
    LVPECL levels
OLVDS OLVDS_INST (Z, LVDS0_O, LVDS1_O); Typical
OLVDS OLVDS_INST (Z, LVDS0_O, LVDS1_O) /* synthesis LEVELMODE="LVPECL" */ ;
    LVPECL levels
```

IBM/OB6/OBZ6 Exceptions

A special instantiation to the LVDS and LVPECL library has been included to allow the user the flexibility to include a single node variation using IBM, OB6, and OBZ6 elements. In this case, as noted in the previous section, the user can add LVDS or LVPECL to the LEVELMODE attribute.

Example:

```
IBM IN9_inst (IN9,S9) /* synthesis LEVELMODE="LVDS" */ ;
OB6 OUT1_inst (S1,OUT1) /* synthesis LEVELMODE="LVPECL" */ ;
OBZ6 OUT2_inst (S2,OUT2) /* synthesis LEVELMODE="LVDS" */ ; used for bussed LVDS
implementations
```

Considerations for Locating I/O

Care must be taken when designers are placing the various I/O types into their design. Designs which use the various input buffers that need VREF supplies must take into consideration the placement limitations needed for the necessary physical restrictions. Following the rule of grouping the various inputs requiring common VREF pads together, the ispLEVER placer algorithm understands the rules needed to supply VREF to a particular I/O or group of I/Os. Therefore, the design may appear to be inefficiently placed due to the limitations. The following examples illustrate potential problems that may arise if these types of situations occur and how the software reports this occurrence.

Too Many Buffers of Different Types

ERROR—par: Unable to find location. PIO component OUT10 not placed.

ERROR—par: There were not enough sites to place all selected components.

This type of error can be prompted if the user constrains the placement of I/O buffers which need various VDDIO levels in the same VDDIO bank. In this case, the physical bank that is preferenced by the user must consider only the use of up to eight VDDIO supplies combined with the available VREF pins within a particular bank. If the mixture of too many standards are attempted, this will cause a similar problem as shown above as the placer searches to meet all the user I/O requirements.

Another user constraint problem can be caused by a design which locks the placement of I/O components. In this scenario, the designer may physically attempt to place I/O that have incompatible VDDIO levels in the same bank. The following example illustrates such an error.

Bad Locate Preference—Mixing VDDIO Within Bank

ERROR—par: chipcheck: LEVELMODE for PIO sig_ex (1) is LVTTTL. This is not compatible with the LEVELMODE for the majority of the bank power supply (VDDIO), 2.5 V.

Differential I/O also need to be thoughtfully addressed during placement. The ispLEVER placer algorithm understands the necessary rules for differential pairing of pads. However, if the user constrains the design and locks pins to certain locations this may also limit pin utilization. In the following error example, the design located a single-ended I/O component on a pad needed for the adjacent complimentary pad of a LVDS differential pair.

Bad Locate Preference—Conflict on an LVDS Pin

```
LOCATE COMP LVDS0_IN SITE P29;
LOCATE COMP FH_0 SITE P30;
Warning - par: Pref conflict: Multi-locate on site. Ignoring LOCATE COMP
"LVDS_IN" SITE "P29";
Keeping LOCATE COMP "FH_0" SITE "P30".
```

In the above example, an LVDS pin was located at site P29, and another buffer at site P30. However, LVDS buffers are differential, and hence need both the True(P29) and complementary(P30) pads on an I/O pair. Since the complementary pad was used by another buffer, the locate on the LVDS buffer was removed.

LOCATE on GSR dedicated PIN.

Locating any pin to the GSR (Global Reset) dedicated pin will not succeed unless a locate Attribute is passed to the Synthesis tool prior to PAR.

The following locate statement in a preference file:

```
LOCATE COMP "inj_err_n" SITE "F5";      #(GSR pin for 82g5 device )
```

Will not be acknowledged on its own. A workaround is to insert the following synthesis attribute in the HDL code: (Verilog)

```
input inj_err_n /*synthesis PAD_TYPE="IBMPU" LOC="F5" */;
```

Input register after GSR dedicated PIN.

If an input is located at the GSR pin, then the user must make sure that the input register it goes to is not located in the Primary IO Cell (PIC).

Synthesis normally inserts any input flops in the PIC. PAR however does not like it when the input register is in the GSR PIC:

During Map:

Optimizing

```
ERROR - map: IO register/latch
      pkt_top_i_pkt_gen_chk_i_pkt_gen_inst_inj_err_n_l1io cannot be implemented
      in PIC.
ERROR - map: Errors found in users design. Output files not written.
```

Workaround:

In synthesis, use an option to prevent IO register insertion:

```
Synplify : define_attribute inj_err_n syn_iof {0}
```

Proper Decoupling and Voltage Source Considerations

Designers must keep in mind the effects of transient currents when designing into high speed systems. The large varying current is seen by the more sensitive input stages through the common power supply rail, which serves all stages. This can happen if the power rail, be it a wire or PCB traces, is of sufficiently high impedance. Even if the power supply were "Ideal," (zero ohms) this can still happen: as the frequencies go higher, the inductive reactance, of the leads or PCB traces, increases.

PCB designs need to be properly decoupled to ensure these power supply noise issues do not effect the system performance. Inadequate sizing and power location of power supply decoupling capacitors can result in numerous board problems. The most common problem associated with inadequate decoupling capacitance is power supply noise (i.e, high frequency noise and or droop). If the decoupling capacitor does not support the switching charge requirements of the device, the power supply must deliver the additional charge (i.e., current). The additional switching current flowing from the power supply to the device on a printed circuit board (PCB) trace creates a voltage drop between the supply and device. Use a minimum of one capacitor per power pin, placed as physically close to the power pins of the device as possible to reduce the parasitic inductance.

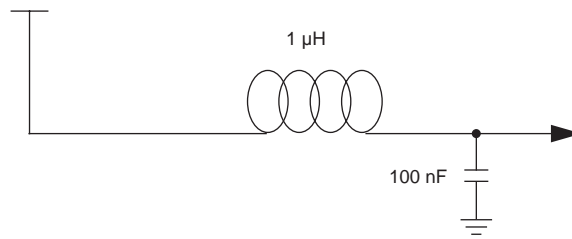
SMT (Surface Mount Technology) or chip capacitors made of ceramic are best such as EIA (Electronic Industries Alliance) sizes 0603 or 0805. Also, it is recommended that use of several size caps in parallel are appropriate, e.g., 1ufd, .1ufd, .001ufd, and etc. The reason for this is as the capacitors become smaller in value, they also get physically smaller, hence less inductance which may not be the most optimal for the design. However this is less the case with SMT caps: consult your capacitor data sheets for the impedance verses frequency plots.

There are instances where the power distribution between stages cannot be sufficiently bypassed. In this case, the designer might be tempted to use several different power supplies. However, by supplying the DC power to each stage through a separate inductor or "choke," while also bypassing to ground that stage, the effect is the same. The choke offers a high impedance path to any errant signals or noise between stages, while offering a very low resistance path to supply. Ferrite Bead Inductors such as Murata BLM31B601S, BLM11B601SPB, or equivalent offer good inductive supply isolation.

These techniques should be considered especially with common-rails for input voltage references and termination voltages. Designers need to isolate these supplies from the noise present on the supply. It is recommended that designers use a "choke and capacitor network" to provide isolation between common supply rails and voltage refer-

ences. AC ripple should be $< 50\text{mVp-p}$ on input DC voltage reference supplies to insure proper input switching characteristics.

Figure 21. Typical voltage reference isolation from common source



Using The I/O Shift Registers

An input/output shift register (IOSR) is available to each group of four pads of a PIC. This feature allows high-speed input data to be divided down by 1/2 or 1/4 and output data-transfer speed can be increased by 2x or 4x its internal speed. Both the input and output shift registers can be programmed to operate at the same time; however, the IOSR should not be connected simultaneously to the same pad. The output shift register can drive any bonded pad of a PIC. Likewise, the input shift register can be driven by any one of the pads of a PIC as long as it is available in a particular package.

For input shift register mode, the high-speed serial data from INDD node of the related pad is connected to the input shift register (IOSR2/IOSR4) via the associated PIC logic. The user has the flexibility to pick any input pad to connect to the register on a per PIC basis. The input data is clocked into the IOSR via a user selectable inverted or noninverted high-speed clock (CK), then divided down into parallel data and is returned to the routing through the INSH[4:1] nodes of the PIC. The data-transfer out of the IOSR is based on the synchronous relationship of the UPDATE signal to CK. The UPDATE signal provides the synchronization to the IOSR which indicates the beginning of the shift cycle. In 4x mode, all the INSH nodes are used. In the 2x mode, only INSH[4:3] are used.

Similarly, the output shift register brings data into the register from the PLC array. The parallel low-speed data from the FPGA fabric is shifted into the register on OUTSH[4:1] nodes and shifted out serially to OUTSH[A:D] nodes of the IOSR to the equivalent node of the PIC. In 4x mode, all OUTSH[4:1] are used to shift in data to the shift register; however, 2x mode only OUTSH[2:1] are used.

The shift register clock (CK) and the UPDATE signals can be sourced from a primary or secondary clock nets of the FPGA array. With this in mind, the user must take into consideration any inherent timing requirements that may be introduced from the routing interface.

Table 22. IOSR Library Support

Library Element Signal	Description
IND	Input signal from associated pad via PIC.
OUTD0	Input to shift register from PLC routing during output mode.
OUTD1	Input to shift register from PLC routing during output mode.
OUTD2	Input to shift register from PLC routing during output mode.
OUTD3	Input to shift register from PLC routing during output mode.
CK	Input/output high-speed clock from primary or secondary clock net.
UPDATE	Clock synchronization from primary/secondary/PPLL/PLLs/general routing.
INQ0	Output from shift register during input mode.
INQ1	Output from shift register during input mode.
INQ2	Output from shift register during input mode.
INQ3	Output from shift register during input mode.
OUTQ	Output to pad via OUTSH node of PIC from shift register during output mode.

Figure 22. Output Shift Register Timing Diagram

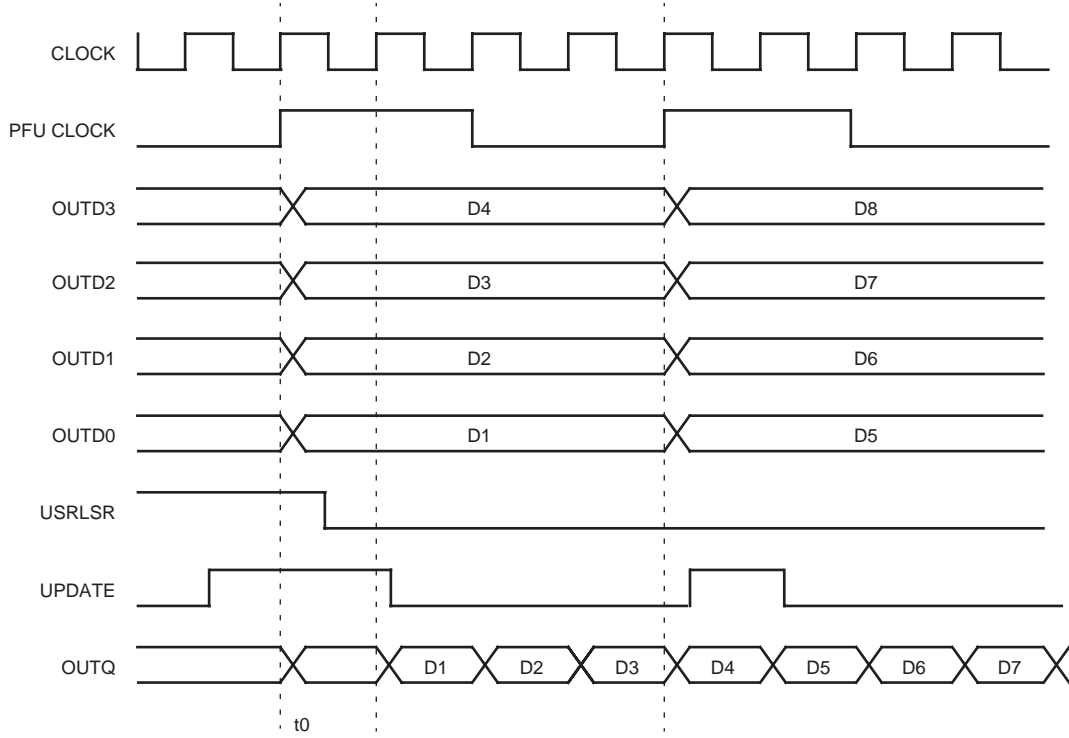


Figure 23. Input Shift Register Timing Diagram

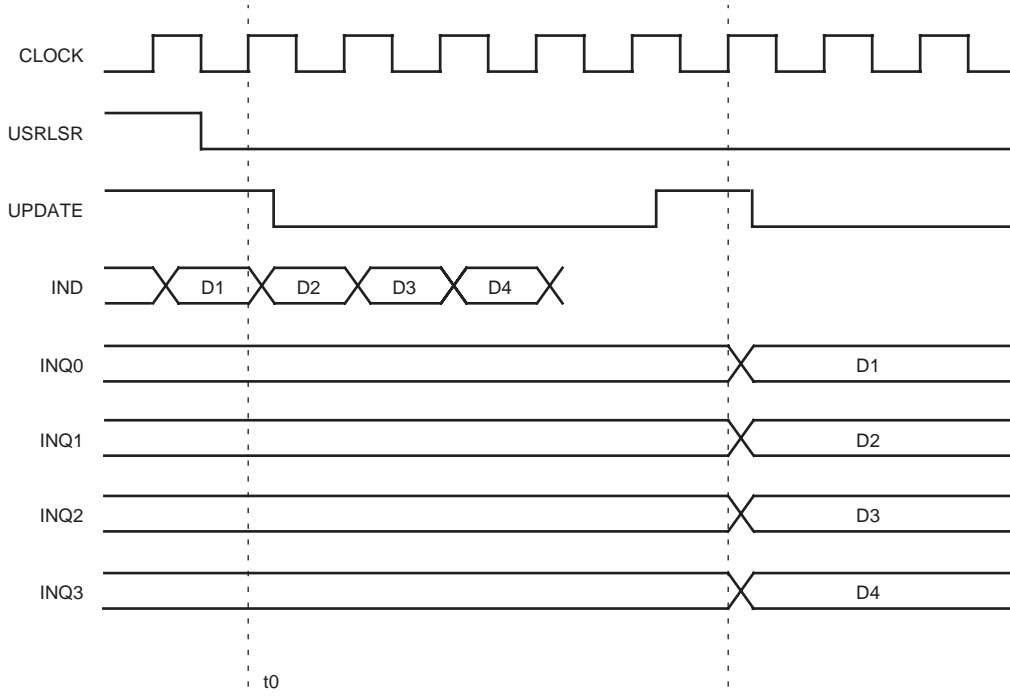
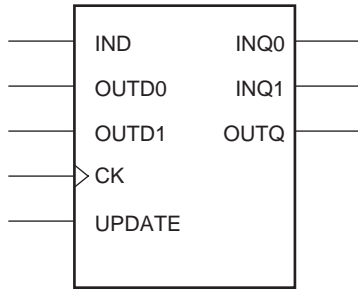


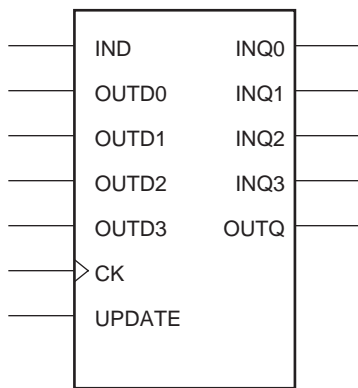
Figure 24. Input/Output 2-bit Shift Register (IOSR2) Macro



INPUT: IND, OUTD0, OUTD1, CK, UPDATE
 OUTPUTS: INQ1, INQ0, OUTQ
 PINORDER: IND, OUTD0, OUTD1, CK, UPDATE, INQ0, INQ1, OUTQ

For input shift registers, IND is the input and INQ0 and INQ1 are the two outputs. For output shift registers, OUTD0 and OUTD1 are the two inputs and OUTQ is the output.

Figure 25. Input/Output 4-bit Shift Register (IOSR4) Macro



INPUTS: IND, OUTD0, OUTD1, OUTD2, OUTD3, CK, UPDATE
 OUTPUTS: INQ0, INQ1, INQ2, INQ3, OUTQ
 PINORDER: IND, OUTD0, OUTD1, OUTD2, OUTD3, CK, UPDATE, INQ0, INQ1, INQ2, INQ3, OUTQ

For input shift registers, IND is the input and INQ0, INQ1, INQ2, and INQ3 are the four outputs. For output shift registers, OUTD0, OUTD1, OUTD2, and OUTD3 are the four inputs and OUTQ is the output.

Double-Data Rate (DDR)

Double-data rate (DDR) allows data to be read on both the rising and the falling edge of the clock which delivers two times the band-width without the need for increased I/O. DDR doubles the memory speed from SDRAMs without the need to increase clock frequency. The flexibility of the PIO allows up to 311 MHz/622 Mbits/s performance using the features of the Series 4.

This type of scheme is necessary for DDR applications, which require data clocking out of the I/O on both edges of the clock. DDR is accomplished by a deviation of the IOSR. The proper instantiation of the IODDR programs the shift register functionality to drive or receive data on both edges of the clock.

When DDR mode is used to receive DDR data from an external source, the input pad passes the data to the DDR register via the PIC logic nodes INFF and INSH. The data is split into odd and even data bits on the rising and falling edges of the data clock and passed to the FPGA logic.

In the output DDR scheme, the output data is received via the DDR register, which are serialized and shifted out on both the positive and negative edges of the clock. This is accomplished by allowing the signal coming to the OUTFF and OUTSH access to only one-half the output clock cycle.

Figure 26. Input DDR Mode Timing Diagram

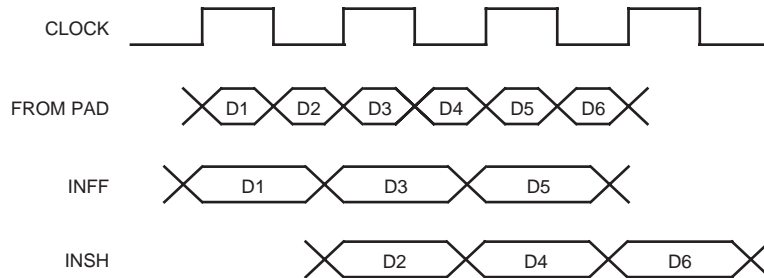


Figure 27. Output DDR Mode Timing Diagram

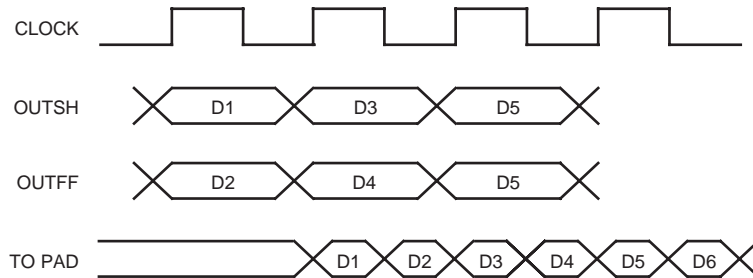
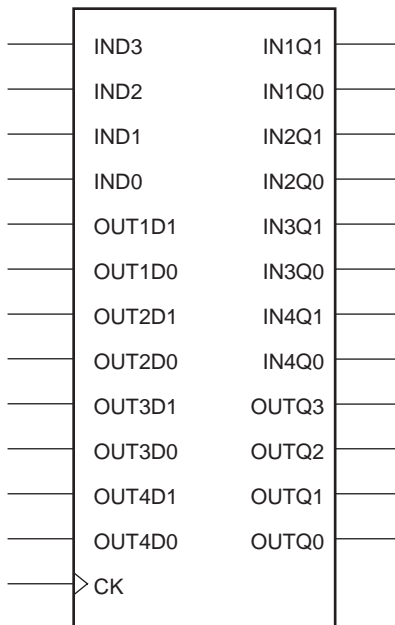


Table 23. Library Support

Library Element Signal	Description
IND[3:0]	Input signal coming from associated pad via PIC.
OUT1D[1:0]	Input to shift register from PLC routing during output mode.
OUT2D[1:0]	Input to shift register from PLC routing during output mode.
OUT3D[1:0]	Input to shift register from PLC routing during output mode.
OUT4D[1:0]	Input to shift register from PLC routing during output mode.
CK	Input/output clock from primary or secondary clock net.
IN1Q[1:0]	Output from shift register during input mode.
IN2Q[1:0]	Output from shift register during input mode.
IN3Q[1:0]	Output from shift register during input mode.
IN4Q[1:0]	Output from shift register during input mode.
OUTQ[3:0]	Output going to pad via PIC from shift register during output mode.

Figure 28. Input/Output DDR (IODDR)



INPUTS: IND0, IND1, IND2, IND3, OUT1D0, OUT1D1, OUT2D0, OUT2D1, OUT3D0, OUT3D1, OUT4D0, OUT4D1, CK
OUTPUTS: IN1Q0, IN1Q1, IN2Q0, IN2Q1, IN3Q0, IN3Q1, IN4Q0, IN4Q1, OUTQ0, OUTQ1, OUTQ2, OUTQ3
PINORDER: IND0 IND1 IND2 IND3 OUT1D0 OUT1D1 OUT2D0 OUT2D1 OUT3D0 OUT3D1 OUT4D0 OUT4D1 CK IN1Q0 IN1Q1 IN2Q0 IN2Q1 IN3Q0 IN3Q1 IN4Q0 IN4Q1 OUTQ0 OUTQ1 OUTQ2 OUTQ3
MINIMUM CELL AREA (All Series): 0
INPUT DDR MODE: IN (D0, D1, D2, D0) CK
IN1, IN2, IN3, IN4 (Q0, Q)

OUTPUT DDR MODE: OUT1, OUT2, OUT3, OUT4 (D0, D1), CK
 OUT (Q0, Q1, Q2, Q3)

Description:

Note that each IODDR is only available to four PIOs. IND0 to IND3 come from the PADS and OUTQ0 to OUTQ3 go to the PADS, so at any given time the input and output with the same index cannot be connected to the same PAD. For example, IND0 and OUTQ0 cannot be used at the same time. Any combination of corresponding input and output mode pins in this element is allowable with respect to the PAD limitation. The designer must be careful in selecting the pins used by the DDR function as to whether or not the designated pads are bonded out in a particular package type.

Figure 29. Connectivity and Functionality of the IODDR in DDR Output Mode

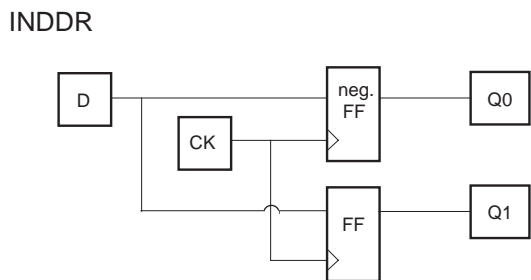
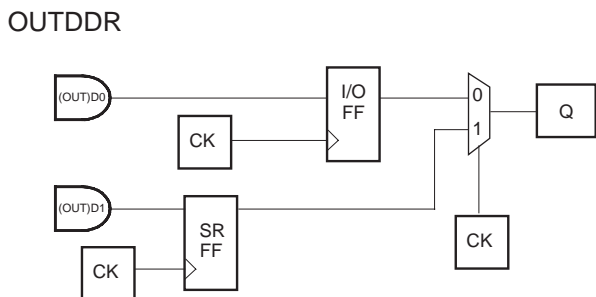


Figure 30. Connectivity and Functionality of the IODDR in DDR Output Mode



To further illustrate the pin functionality and connectivity of the IODDR, the table below shows the functionality of pin combinations when the inputs are connected to their possible outputs to the right.

Table 24. Pin Functionality and Connectivity of the IODDR

Input Pin(s)	Functionality	Output Pin(s)
Input DDR Mode		
IND0	Flip-flop output (negative edge-triggered) Flip-flop output (positive edge-triggered)	IN1Q0 IN1Q1
IND1	Flip-flop output (negative edge-triggered) Flip-flop output (positive edge-triggered)	IN2Q0 IN2Q1
IND2	Flip-flop output (negative edge-triggered) Flip-flop output (positive edge-triggered)	IN3Q0 IN3Q1
IND3	Flip-flop output (negative edge-triggered) Flip-flop output (positive edge-triggered)	IN4Q0 IN4Q1
Output DDR Mode		
OUT1D0 OUT1D1	I/O Flip-flop input (positive edge-triggered) SR Flip-flop input (positive edge-triggered)	OUTQ0
OUT2D0 OUT2D1	I/O Flip-flop input (positive edge-triggered) SR Flip-flop input (positive edge-triggered)	OUTQ1
OUT3D0 OUT3D1	I/O Flip-flop input (positive edge-triggered) SR Flip-flop input (positive edge-triggered)	OUTQ2
OUT4D0 OUT4D1	I/O Flip-flop input (positive edge-triggered) SR Flip-flop input (positive edge-triggered)	OUTQ3

Designers need to locate (LOC) your shift registers with care. One has to look at the bonded pads for each PIC for the package you are targeting and match up the wiring to fit the hardware. Also, the shift registers or the IO pins need to be located correctly. Below are two respective example errors that may be received from the Place and Route (PAR) software when IODDR macros are wired to pads in a way that is inconsistent with the package.

```

---
ERROR - par: can not find initial placement for shift comp RX_CH0
Dedicated connected PIO comps for this shift comp are:
CH0_IN_14, CH0_IN_15,
Among possible reasons are too small package and preference conflict.
---
ERROR - par: Based on physical connectivity, comp CH0_IN has to be
placed at site PT47A. However, due to reference/power voltage or
signal sharing conflict, the placer is not able to place it at the
site. It will be placed somewhere else and will result in a
un-routable placement
---
```

Additional information on DDR applications can be found in Lattice's Technical Note TN1037.

ZBT Memory Interfaces with Series 4

Series 4 I/O provide 200 MHz ZBT requirements when switching between write and read cycles. ZBT allows 100% use of bus cycles during back-to-back read/write and write/read cycles. However, this maximum utilization of the bus increases probability of bus contention when the interfaced devices attempt to drive the bus to opposite logic values. The LVTTTL I/O interfaces directly with commercial ZBT SRAMs signaling and allows the versatility to program the FPGA drive strengths from 6 mA to 24 mA.

Bus contention with ZBT SRAMs is a particular concern when shifting from write to read with no dead cycles, as performed in the past with traditional SRAM designs. Previously, writes being performed by the FPGA based SRAM controller typically had to go into a high-Z state before the SRAM output drivers turned on for the next read cycle to prevent bus contention. This was needed for both the SRAM and the FPGA to protect the devices from the voltage drops caused by bus contention. But today, SRAM manufacturers have made improvements to the SRAM I/O to eliminate the concern and improve the speed and bandwidth of ZBT devices. The ORCA I/O is designed to operate without dead cycles as well as to tolerate the small amounts of bus contention that occur. This optimization not only provides a seamless interface to ZBT SRAMs but also is an excellent solution for high-performance telecommunication and networking applications.

Figure 31. ZBT Bus Turnaround for Flow through

