# MachXO2 Hardware Checklist

## Technical Note

FPGA-TN-02154-1.9

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# Tables

# Acronyms in This Document

A list of acronyms used in this document.

| Acronym | Definition |
|---|---|
| FPGA | Field Programmable Gate Array |
| $I^2C$ | Inter-Integrated Circuit |
| JTAG | Joint Test Action Group |
| PCB | Printed Circuit Board |
| PLD | Programmable Logic Device |
| POR | Power-On Reset |
| SPI | Serial Peripheral Interface |
| SRAM | Static Random-Access Memory |

# 1. Introduction

When designing complex hardware using the MachXO2™ PLD, designers must pay special attention to critical hardware configuration requirements. This technical note steps through these critical hardware requirements related to the MachXO2 device. This document does not provide detailed step-by-step instructions but gives a high-level summary checklist to assist in the design process.

The MachXO2 ultra-low power, instant-on, non-volatile PLDs are available in three versions – ultra low power (ZE) and high performance (HC and HE) devices. HC devices have an internal linear voltage regulator which supports external VCC supply voltages of 3.3 V or 2.5 V. ZE and HE devices only accept 1.2 V as the external VCC supply voltage. With the exception of power supply voltage, all three types of devices (ZE, HC and HE) are functionally and pin compatible with each other.

This technical note assumes that the reader is familiar with the MachXO2 device features as described in MachXO2 Family Data Sheet (FPGA-DS-02056).

The critical hardware areas covered in this technical note include:

- Power supplies as they relate to the MachXO2 supply rails and how to connect them to the PCB and the associated system
- Configuration and how to connect the configuration mode selection for proper power up configuration
- Device I/O interface and critical signals

Important: Users should refer to the following documents for detailed recommendations.

- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02115)
- Power Estimation and Management for MachXO2 Devices (FPGA-TN-02161)
- MachXO2 sysIO Usage Guide (FPGA-TN-02158)
- Implementing High-Speed Interfaces with MachXO2 Devices (FPGA-TN-02153)
- MachXO2 Programming and Configuration Usage Guide (FPGA-TN-02155)
- Using User Flash Memory and Hardened Control Functions in MachXO2 Devices (FPGA-TN-02162)

# 2. Power Supply

The VCC and VCCIO0 power supplies determine the MachXO2 internal *power good* condition. These supplies need to be at a valid and stable level before the device can become operational. In addition, there are VCCIO1-5 supplies that power the remaining I/O banks. Table 2.1. shows the power supplies and the appropriate voltage levels for each.

Refer to MachXO2 Family Data Sheet (FPGA-DS-02056) for more information on the voltage levels.

**Table 2.1. Power Supply Description and Voltage Levels**

| Supply | Voltage (Nominal Value) | Description |
|---|---|---|
| VCC | 1.2 V | Core power supply for 1.2 V devices (ZE and HE) |
| | 2.5 V/3.3 V | Core power supply for 2.5 V/3.3 V devices (HC) |
| VCCIOx | 1.2 V to 3.3 V | Power supply pins for I/O Bank x. There are up to five I/O banks. |

# 3. Power Estimation

Once the MachXO2 device density, package and logic implementation is decided, power estimation can be performed using the Power Calculator tool which is provided as part of the Lattice Diamond® design software. While performing power estimation the user should keep two specific goals in mind.

1. Power supply budgeting should be considered based on the maximum of the power-up in- rush current, configuration current or maximum DC and AC current for a given system environmental condition.
2. The ability of the system environment and MachXO2 device packaging to support the specified maximum operating junction temperature.

By determining these two criteria, system design planning can take the MachXO2 power requirements into consideration early in the design phase.

This is explained in Power Estimation and Management for MachXO2 Devices (FPGA-TN-02161).

# 4. Configuration Considerations

MachXO2 devices contain two types of memory, SRAM and Flash. SRAM is volatile memory and contains the active configuration. Flash is non-volatile memory that provides on-chip storage for the SRAM configuration data.

The MachXO2 includes multiple programming and configuration interfaces:

- 1149.1 JTAG
- Self download
- Slave SPI
- Master SPI
- Dual Boot
- $I^2C$
- WISHBONE bus

For ease of prototype debugging it is recommended that every PCB should have easy access to the programming and configuration pins.

The configuration logic arbitrates access from the interfaces by the following priority. When higher priority ports are enabled, Flash Memory access by lower priority ports are blocked.

1. JTAG Port
2. Slave SPI Port (SN low activates the SPI port)
3. $I^2C$ Primary Port

**Note:** Erased device have all programming and configuration ports enabled by default. When the device is erased, ensure SN and ProgramN are not driven low.

For a detailed description of the programming and configuration interfaces, refer to MachXO2 Programming and Configuration Usage Guide (FPGA-TN-02155).

The use of external resistors is always needed if the configuration signals are being used to handshake with other devices. Pull-up and pull-down resistor (4.7k) recommendations on different configuration pins are listed below.

**Table 4.1. Default State of the sysCONFIG Pins**

| Pin Name | Pin Function (Configuration Mode) | Pin Direction (Configuration Mode) | Default Function (User Mode) |
|---|---|---|---|
| PROGRAMN | PROGRAMN | Input with weak pull-up, external pullup to $V_{CCIO0}$. | PROGRAMN |
| INITN | I/O | I/O with weak pull-up | User-defined I/O |
| DONE | I/O | I/O with weak pull-up, external pullup to $V_{CCIO0}$ | User-defined I/O |
| MCLK/CCLK | SSPI | Input with weak pull-up. MCLK function requires external 1kΩ pull-up. | User-defined I/O |
| SN | SSPI | Input with weak pull-up, external pull-up to $V_{CCIO2}$ | User-defined I/O |
| SI/SPISI | SSPI | Input | User-defined I/O |
| SO/SOSPI | SSPI | Output | User-defined I/O |
| CSSPIN | I/O | I/O with weak pull-up, external pullup to $V_{CCIO2}$. | User-defined I/O |
| SCL | $I^2C$ | Bi-Directional open drain, external pull-up, noise filter (200 Ω series/100pF to GND). | User-defined I/O |
| SDA | $I^2C$ | Bi-Directional open drain, external pull-up, noise filter (100 Ω series/100pF to GND). | User-defined I/O |
| TDI | TDI | Input with weak pull-up | TDI |
| TDO | TDO | Output with weak pull-up | TDO |
| TCK | TCK | Input. Recommended 4.7kΩ pull down | TCK |
| TMS | TMS | Input with weak pull-up | TMS |
| JTAGENB | I/O | Input with weak pull-down | I/O |

# 5. Master SPI

When configuring from an external SPI Flash, ensure:

- The SPI Flash $V_{CC}$ and the MachXO2 $V_{CCIO2}$ are at the same level.
- The SPI Flash $V_{CC}$ meets is at the vendor's data sheet recommended operating level.
- The SPI Flash POR level is lower than the MachXO2 POR level.
  - If the SPI Flash POR is higher than the MachXO2 POR refer to MachXO2 Programming and Configuration Usage Guide (FPGA-TN-02155).

# 6. PROGRAMN Initial Power Considerations

The MachXO2 PROGRAMN is permitted to become a general purpose I/O. The PROGRAMN only becomes a general purpose I/O after the configuration bitstream is loaded. When power is applied to the MachXO2 the PROGRAMN input performs the PROGRAMN function. It is critical that any signal input to the PROGRAMN have a high-to-low transition period that is longer than the VCC (min) to INITN rising edge time period. Transitions faster than this time period prevent the MachXO2 from becoming operational. Refer to the description of PROGRAMN in MachXO2 Programming and Configuration Usage Guide (FPGA-TN-02155).

# 7. Pin-out Considerations

The MachXO2 PLDs support many applications with high-speed interfaces. These include various rule-based pinouts that need to be understood prior to the implementation of the PCB design. The pin-out selection must be completed with an understanding of the interface building blocks of the FPGA fabric. These include IOLOGIC blocks such as DDR, clock resource connectivity, and PLL usage. Refer to Implementing High-Speed Interfaces with MachXO2 Devices (FPGA-TN-02153) for rules pertaining to these interface types.

# 8. True-LVDS Output Pin Assignments

True-LVDS outputs are on the top bank (Bank 0) of the MachXO2-1200 and higher density devices. When using the LVDS outputs, a 2.5 V or 3.3 V supply needs to be connected to the Bank 0 VCCIO supply rails. Refer to MachXO2 sysIO Usage Guide (FPGA-TN-02158) for more information on this.

# 9. HSTL, SSTL and Referenced LVCMOS Pin Assignments

The externally-referenced I/O standards (HSTL and SSTL) and internally referenced LVCMOS require an external reference voltage. Each I/O bank supports one reference voltage (VREF). Any I/O in the bank can be configured as the input reference voltage pin. This pin is a regular I/O if it is not used as a reference voltage input. The VREF pin(s) should get the highest priority for pin assignment. The input reference voltage can also be generated internally from the VREF generator. Again, there is one VREF generator per bank and its programmable settings include OFF, 45% of VCCIO, 50% of VCCIO, and 55% of VCCIO. Programming of the internal VREF generator and the external VREF pin cannot be set at the same time for a particular bank since there is only one VREF per bank.

# 10. PCI Clamp Pin Assignment

PCI clamps are available on the bottom I/O bank (Bank 2) of the MachXO2-1200 and higher density devices. When the system design calls for PCI clamp, these pins should be assigned to I/O Bank 2. For the clamp characteristic, refer to the IBIS buffer models either on the Lattice web site or in the Lattice Diamond design software.

# 11. Back Leakage Considerations

When the part is powered down, there are some situations where current is still present due to active I/O, similar to a hot socketing situation. This can potentially cause the internal voltage supply to rise to power-on reset levels and start device operation. To mitigate for this back leakage current, it is recommended to add a weak pulldown resistor to the voltage supply. This should be set to value sufficient to keep the voltage below the POR trip point of the device with the worst case I/O back leakage current applied.

# 12. Checklist

**Table 12.1. Default State of the sysCONFIG Pins**

| | MachXO2 Hardware Checklist Item | OK | N/A |
|---|---|---|---|
| 1 | Power Supply | | |
| 1.1 | Core Supply VCC at 1.2 V | | |
| 1.2 | Core Supply VCC at 2.5 V or 3.3 V | | |
| 1.3 | I/O power supply VCCIO 0-5 at 1.2 V to 3.3 V | | |
| 1.4 | Power Estimation | | |
| 2 | Configuration | | |
| 2.1 | Configuration options | | |
| 2.2 | Pull-up on PROGRAMN, INITN, DONE | | |
| 2.3 | Pull-up on SPI mode pins | | |
| 2.4 | Pull-up on $I^2C$ mode pins | | |
| 2.5 | JTAG default logic levels | | |
| 2.6 | PROGRAMN high-to-low transition time period is larger than the VCC (min) to INITN rising edge time period | | |
| 3 | I/O pin assignment | | |
| 3.1 | True LVDS pin assignment considerations | | |
| 3.2 | HSTL, SSTL and referenced LVCMOS pin assignment considerations | | |
| 3.3 | PCI clamp requirement considerations | | |

# Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

# Revision History

**Revision 1.9, January 2022**

| Section | Change Summary |
|---|---|
| All | Minor adjustments in formatting across the document. |
| Acronyms in This Document | Added this section. |
| Introduction | Updated document link for Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02115). |

**Revision 1.8, March 2020**

| Section | Change Summary |
|---|---|
| All | • Changed document number from TN1208 to FPGA-TN-02154.<br>• Updated document template. |
| Disclaimers | Added this section. |
| Back Leakage Considerations | Added this section. |

**Revision 1.7, April 2015**

| Section | Change Summary |
|---|---|
| Master SPI | Updated this section. Revised the third item to consider when configuring from an external SPI Flash. |
| Technical Support Assistance | Updated this section. |

**Revision 1.6, June 2014**

| Section | Change Summary |
|---|---|
| Master SPI | Updated this section. |

**Revision 1.5, January 2014**

| Section | Change Summary |
|---|---|
| Configuration Considerations | Updated this section. Defined termination for SN and ProgramN when the device is erased. |

**Revision 1.4, September 2013**

| Section | Change Summary |
|---|---|
| Configuration Considerations | Updated CSSPIN information in Default State of the sysCONFIG Pins table. |

**Revision 1.3, August 2013**

| Section | Change Summary |
|---|---|
| Configuration Considerations | • Added access priority information to the this section.<br>• Added requirement of including a 1 kOhm pullup on SN.<br>• Updated the Default State of the sysCONFIG Pins table. |
| Master SPI | Added information on configuring from an external SPI Flash. |
| Technical Support Assistance | Updated Technical Support Assistance information. |

**Revision 1.2, September 2012**

| Section | Change Summary |
|---|---|
| PROGRAMN Initial Power Considerations | Added this section. |
| Checklist | Added item 2.6 to the Checklist table. |

**Revision 1.1, June 2012**

| Section | Change Summary |
|---|---|
| All | Updated document with new corporate logo. |
| Configuration Considerations | Added external pull-up requirement on SPI signals and updated this section. |

**Revision 1.0, April 2011**

| Section | Change Summary |
|---|---|
| All | Initial release. |


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