

## Introduction

Starting a complex system with a large FPGA hardware design requires that the FPGA designer pay attention to the critical hardware implementation to increase the chances of success for the hardware. This technical note systematically steps through these critical hardware implementation items relative to the LatticeXP2™ device. LatticeXP2 is the third-generation non-volatile FPGA from Lattice with on-chip Flash to store the configuration. The device family consists of FPGA LUT densities ranging from 5K to 40K. This technical note assumes that the reader is familiar with the LatticeXP2 device features as described in the [LatticeXP2 Family Data Sheet](#).

The critical hardware areas covered in this technical note are:

- Power supplies as they related to the LatticeXP2 supply rails and how to connect them to the PCB and the associated system
- Configuration and how to connect the configuration mode selection for proper power up configuration
- Device I/O interface and critical signals

## Power Supply

The  $V_{CC}$  and  $V_{CCAUX}$  power supplies determine the LatticeXP2 internal “power good” condition. In addition to the two power supplies, there are  $V_{CCIO0-7}$ ,  $V_{CCPLL}$  and  $V_{CCJ}$  supplies that power the I/O banks, PLL and JTAG port. All power supplies are required for the proper device operation but since  $V_{CC}$  and  $V_{CCAUX}$  determine the device power-on condition, it is recommended to have one of these supplies be the final power supply to power up the LatticeXP2 device after all other power supplies are stable. Table 18-1 shows the power supplies and the appropriate voltage levels for each supply.

**Table 18-1. Power Supply Description and Voltage Levels**

Supply	Voltage (Typ.)	Description
$V_{CC}$	1.2V	Core power supply. A typical $V_{CC}$ device internal power up and power down trip point is between 0.7V and 0.9V.
$V_{CCAUX}$	3.3V	Auxiliary power supply. A 3.3V supply that provides an internal reference to the input buffers. A typical $V_{CCAUX}$ device internal power up and power down trip point is between 2.0V and 2.8V.
$V_{CCPLL}$	3.3V	Power supply for PLL.
$V_{CCIO0-7}$	1.2V to 3.3V	I/O power supply. There are eight banks of I/Os and each bank has its own supply $V_{CCIO0}$ to $V_{CCIO7}$ .
$V_{CCJ}$	1.2V to 3.3V	JTAG power supply for TAP controller port.

## Power Supply Sequencing

There is no specific power sequencing requirement for the LatticeXP2 device family. If the user's system has the option to design for power sequencing, a practical sequencing to keep in mind is based on the fact that  $V_{CC}$  and  $V_{CCAUX}$  determine when the core powers up. In order insure proper functional behavior, it is desirable to bring up the  $V_{CCIO}$ ,  $V_{CCJ}$  and  $V_{CCPLL}$  first in any order and bring up  $V_{CC}$  first and  $V_{CCAUX}$  next in a sequential order. Power sequencing considerations should also consider that common supplies generally are tied together to the same rail. For example, if there is a 3.3V  $V_{CCIO}$ , it should be tied to the same supply as the 3.3V rail for  $V_{CCAUX}$ . LatticeXP2 is able to tolerate any order of power sequencing without causing any high current leakage paths during power up.

## Power Supply Ramp

Similar to the power supply sequencing, there is no specific requirement for the LatticeXP2 but care must be given to the power supply ramp times in a reasonable range. The reasonable range is defined by the majority of the power supply related device test data taken as part of the device characterization. The fast end of the spectrum is defined to be 100 $\mu$ s for the supply to transition from zero volts to minimum supply voltage level. The slow end of the spectrum is defined to be 100ms for the supply to transition from zero volts to minimum supply voltage. These ranges should be used as general guidelines for the system design consideration.

## Power Estimation

Once the LatticeXP2 device density, package and logic implementation is decided, power estimation for the system environment should be determined based on the software Power Calculator provided as part of ispLEVER<sup>®</sup> design tool. The power estimation should keep two specific goals in mind.

1. Power supply budgeting should be considered based on the maximum of the power-up in-rush current, configuration current or maximum DC and AC current for given system environmental condition.
2. The ability for the system environment and LatticeXP2 device packaging to be able to support the specified maximum operating junction temperature.

By determining these two criteria, system design planning can take the LatticeXP2 power requirements into consideration early in the design phase.

## Configuration

There are two options to configure the LatticeXP2 devices. The obvious and most common method is using the on-chip Flash memory. This method is called the Self Download Mode or SDM. The SDM is determined by the CFG0 signal. CFG0 needs to be pulled high in order to boot the device from the on-chip flash memory. Table 18-2 shows the proper CFG bit setting.

**Table 18-2. Configuration Mode Selection**

Configuration Mode	CFG1	CFG0	Description
SPI Flash Boot	0	0	Master SPI Boot first then embedded Flash.
Embedded Flash Boot	1	0	Embedded flash boot first then external SPI Flash.
Self Download Mode (SDM)	X	1	SDM only.

The SPI configuration port resides in I/O bank 7. Accordingly, the  $V_{CCI07}$  must match the supply rail of the SPI Flash. For example, if the external SPI Flash uses 3.3V rail,  $V_{CCI07}$  must be tied to 3.3V supply rail as well.

There are several dual-purpose pins that can be used as general-purpose I/O pins when not used for configuration. Table 18-3 lists these dual-purpose pins. When CFGx is set to one of the two external SPI flash options and persistence is OFF, the dual-purpose configuration pins will become general-purpose I/O pins after configuration. These pins should be used only when they are not used for configuration. When used for configuration, persistence should be ON, to dedicate these pins for configuration. In order to insure proper configuration, it is recommended to use external resistors for the configuration pins. The CFG0 must have external resistor for any configuration mode. When CFG0=0, CFG1, PROGRAMN, INITN and DONE pins must have the appropriate external pull-up or pull-down resistors.

**Table 18-3. Configuration Pin Descriptions**

Pin Name	I/O Type	Pin Type	Description
CFG0	Input, weak pull-up	Dedicated	FPGA configuration mode selection
CFG1	Input, weak pull-up	Dual-Purpose	
PROGRAMN	Input, weak pull-up	Dual-Purpose	FPGA Configuration control and status signals
INITN	Bi-Directional Open Drain, weak pull-up	Dual-Purpose	
DONE	Bi-Directional Open Drain with weak pull-up or Active Drive	Dual-Purpose	
CCLK	Input or Output	Dual-Purpose	Configuration clock
SISPI	Input or Output	Dual-Purpose	SPI control and data signals
SOSPI	Input or Output	Dual-Purpose	
CSSPISN	Input, weak pull-up	Dual-Purpose	
CSSPIN	Output, tri-state, weak pull-up	Dual-Purpose	

### JTAG Interface

The JTAG interface pins are referenced to  $V_{CCJ}$ . Typically, JTAG pins are referenced to 3.3V supply.  $V_{CCJ}$  can support supplies from 1.2V to 3.3V. In cases where  $V_{CCJ}$  is connected to supplies other than 3.3V, validate that the JTAG interface cable or tester can support I/O interface with the same I/O voltage standard.

### I/O Interface and Critical Pins

There are eight I/O banks on every LatticeXP2 device. I/O Bank 7 contains the configuration pins and as such, the configuration requirements should have the highest priority to determine the supply voltage levels for  $V_{CCIO7}$ .

### I/O Pin Assignments Around $V_{CCPLL}$

The  $V_{CCPLL}$  provides a “quiet” supply for the internal PLLs. For the best PLL jitter performance, careful pin assignment must keep away the “noisy” I/O pins away from the BGA ball location that are identified as sensitive pins as shown in Figure 18-1. In this case the sensitive pins would be one of the  $V_{CCPLL}$  supply pins. The “noisy” I/O pins are generally defined to have the highest switching frequency, highest  $V_{CCIO}$  standard and fastest output slew rates. For example, using the Figure 18-1 3x3 and 5x5 grid of ball locations, one can identify the “keep out” ball locations for the potentially “noisy” signals. *Note: In fpBGA and ftBGA packages,  $V_{CCPLL}$  is not provided from its own pins; it is connected to the  $V_{CCAUX}$  pins. In this case, this discussion applies to the  $V_{CCAUX}$  pins.*

**Figure 18-1. “Quiet” Pin Assignment Consideration for BGA Package**

5x5	5x5	5x5	5x5	5x5
5x5	3x3	3x3	3x3	5x5
5x5	3x3	<b>Sensitive Pin</b>	3x3	5x5
5x5	3x3	3x3	3x3	5x5
5x5	5x5	5x5	5x5	5x5

## **DDR/DDR2 Memory Interface Pin Assignments**

The DDR Memory interface on the LatticeXP2 device family is provided with a pre-engineered I/O register along with the precision I/O DLL timing control. There are two I/O DLL specifically assigned to the two halves of the device. One I/O DLL supports I/O banks 1, 2, 3 and 4; another I/O DLL supports I/O banks 0, 5, 6 and 7.

In addition to the I/O DLL assignments, there are pre-defined data strobes (DQS) signals that can support a span of I/O pins as part of the memory data lanes. When assigning DDR memory interface I/O pins, the FPGA designer must insure that there is enough I/O pins to assign DDR memory data pins for each of the assigned DQS signals.

## **True-LVDS Output Pin Assignments**

True-LVDS outputs are available on 50% of the I/O pins on the left and right sides of the device. The left and right side I/O banks are banks 2, 3, 6 and 7. When using the LVDS outputs, a 2.5V supply needs to be connected to these VCCIO supply rails.

## **HSTL and SSTL Pin Assignments**

These externally referenced I/O standards require an external reference voltage. Each of the LatticeXP2 device family I/O banks allows up to two pre-defined  $V_{REF}$  pins. The  $V_{REF}$  pin(s) should get the highest priority for pin assignment.

## **PCI Clamp Pin Assignment**

PCI clamps are available on the top and bottom sides of the device. When the system design calls for PCI clamp, those pins should be assigned to I/O banks 0, 1, 4 and 5. For the clamp characteristic, refer to the IBIS buffer models either on the Lattice website at [www.latticesemi.com](http://www.latticesemi.com) or in the ispLEVER design tool.

## **Test Output Enable (TOE)**

TOE signal is used to tri-state all I/O pins and override the functional outputs for board level test. It is recommended to have a pull-up resistor to make sure that when not in use, the TOE will not interfere with the normal functionality of the I/O pins.

## Checklist

	LatticeXP2 Hardware Checklist Item	OK	N/A
1	<b>Power Supply</b>		
1.1	Core Supply VCC @ 1.2V		
1.2	Auxiliary Supply V <sub>CCAUX</sub> @ 3.3V		
1.3	PLL Supply V <sub>CCPLL</sub> @ 3.3V		
1.4	JTAG Supply V <sub>CCJ</sub> from 1.2V to 3.3V		
1.5	I/O Supply V <sub>CCIO0-7</sub> from 1.2V to 3.3V		
1.6	Supply Sequencing considerations		
1.7	Supply Ramp considerations		
1.8	Power Estimation		
2	<b>Configuration</b>		
2.1	Consistency of V <sub>CCIO7</sub> Supply if external SPI Flash is used		
2.2	Configuration control and status selections		
2.2.1	Pull-up or Pull-down on CFG0 <sup>2</sup>		
2.2.2	Pull-up or Pull-down on CFG1 <sup>1,2</sup>		
2.2.3	Pull-up on PROGRAMN <sup>1,3</sup> , INITN <sup>1,3</sup> , DONE <sup>1,3</sup> , TOE <sup>2</sup>		
2.2.4	Pull-down on TCK		
2.3	JTAG Supply and default logic levels		
3	<b>I/O Pin Assignment</b>		
3.1	I/O pin assignments around V <sub>CCPLL</sub>		
3.2	DDR Memory pin assignment considerations		
3.3	True-LVDS pin assignment considerations		
3.4	HSTL and SSTL pin assignment considerations		
3.5	PCI clamp requirement considerations		

1. Only necessary when CFG1=0.
2. CFG0, TOE pins are internally linked to the VCC core voltage and can be pulled up to VCC core. CFG1 pins are internally linked to VCCIO7 and can be pulled up to same voltage as VCCIO7.
3. When used, PROGRAMN, INITN, and DONE pulled up to same voltage as VCCIO7.

## Technical Support Assistance

e-mail: [techsupport@latticesemi.com](mailto:techsupport@latticesemi.com)

Internet: [www.latticesemi.com](http://www.latticesemi.com)

## Revision History

Date	Version	Change Summary
June 2007	01.0	Initial release.
March 2011	01.1	Added note to "I/O Pin Assignments Around V <sub>CCPLL</sub> " text section.
May 2011	01.2	Updated Checklist table footnotes.
September 2013	01.3	Updated CFG0 signal information in Configuration section.
		Updated Checklist table footnotes.
		Updated corporate logo.
		Updated Technical Support Assistance information.