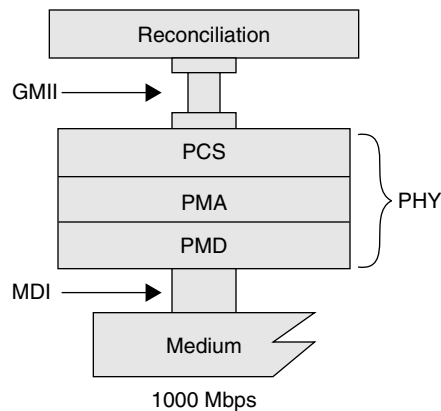


Introduction

The IEEE 802.3-2002 Gigabit Ethernet standard is organized along architectural lines, emphasizing the large-scale separation of the system into two parts: the Media Access Control (MAC) sub-layer of the Data Link Layer and the Physical Layer.

Figure 1 highlights the sub-layers that constitute the Gigabit Ethernet Physical Layer.

Figure 1. Gigabit Ethernet Physical Layer



According to the 802.3-2002 standard, two important compatibility interfaces are defined within what is architecturally the Physical Layer:

- **Medium Dependent Interfaces (MDI).** To communicate in a compatible manner, all stations shall adhere rigidly to the exact specification of physical media signals defined in Clause 8 (and beyond) in the IEEE 802.3-2002 standard, and to the procedures that define correct behavior of a station. Local Area Network requires complete compatibility at the Physical Medium interface (that is, the physical cable interface).
- **Gigabit Media Independent Interface (GMII).** The GMII is designed to connect a gigabit-capable MAC or repeater unit to a gigabit PHY. While conformance with implementation of this interface is not strictly necessary to ensure communication, it is highly recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at gigabit speeds. The GMII is intended for use as a chip-to-chip interface. No mechanical connector is specified for use with the GMII. The GMII is optional.

The objective of this technical note is to provide a report on the Gigabit Ethernet Physical Layer interoperability tests between a LatticeSC™ device and the MARVELL 88E1111/88E1112 devices. Specifically, this technical note discusses the following topics:

- Overview of LatticeSC devices and MARVELL Alaska™ Ultra 88E1111/ 88E1112 devices.
- Gigabit Ethernet Physical Layer Interoperability testing of the LatticeSC and MARVELL 88E1111/88E1112 devices.

LatticeSC/flexiPCS™ Overview

LatticeSC Features

The LatticeSC family equipped with ASIC-like system level building blocks was designed as a platform technology to facilitate the implementation of the many connectivity challenges that designers face today. This family of devices

includes features to meet the needs of today's communication network systems. These features include up to 7.8 Mbits of embedded block RAM, dedicated logic to support system level standards such as Rapid IO, HyperTransport, SPI4.2, SFI-4, UTOPIA, XGMII and CSIX. Furthermore, the devices in this family feature clock multiply, divide and phase shift PLLs, numerous DLLs and dynamic glitch free clock MUX that are required in today's high-end system designs.

All LatticeSC devices also feature up to 32 channels of embedded SERDES with associated Physical Coding Sublayer (PCS) logic. The flexiPCS logic can be configured to support numerous industry standard high-speed data transfer protocols.

Each channel of flexiPCS logic contains dedicated transmit and receive SERDES

flexiPCS Gigabit Ethernet Features

The Gigabit Ethernet mode of the flexiPCS (Physical Coding Sublayer) block supports full compatibility, from the Serial I/O to the GMII interface of the IEEE 802.3-2002 Gigabit Ethernet standard.

The LatticeSC flexiPCS in Gigabit Ethernet mode supports the following operations:

Transmit Path (From LatticeSC Device to Line):

- Cyclic Redundancy Check (CRC) generation and insertion into Gigabit Ethernet frame
- Transmit State Machine, which performs 8-bit data encapsulation and formatting, including the Auto-Negotiation code word insertion and outputting the correct 8-bit code/data word and k control characters according to the IEEE 802.3-2002 specification
- 8b/10b encoding

Receive Path (From line to LatticeSC Device):

- Word alignment based on IEEE 802.3-2002 defined alignment characters
- 8b/10b decoding
- Link State Machine functions compliant with the IEEE 802.3-2002 specification
- Clock Tolerance Compensation logic capable of accommodating clock domain differences
- Receive State Machine including Auto-Negotiation support compliant to the IEEE 802.3-2002 specification
- Cyclic Redundancy Code (CRC) checking.

Marvell Alaska Ultra 88E1111/88E1112 Overview

88E1111/88E1112 Features

The Alaska Ultra 88E1111/88E1112 Gigabit Ethernet Transceivers are physical layer devices for Ethernet 1000BASE-T, 100BASE-TX, and 10BASE-T applications. They contain all the active circuitry required to implement the physical layer functions to transmit and receive data on standard CAT 3 and CAT 5 unshielded twisted pair.

The 88E1111/88E1112 devices support the Gigabit Media Independent Interface (GMII), Reduced GMII (RGMII), Serial GMII (SGMII), the Ten-Bit Interface (TBI), and Reduced TBI (RTBI) for direct connection to a MAC/Switch port.

The 88E1111/88E1112 devices incorporate a 1.25GHz SERDES, which may be directly connected to a fiber-optic transceiver for 1000BASE-T/1000BASE-X media conversion applications. Additionally, the 88E1111/88E1112 devices may be used to implement 1000BASE-T Gigabit Interface Converter (GBIC) or Small Form Factor Pluggable (SFP) modules.

The 88E1111/88E1112 devices use advanced mixed-signal processing to perform equalization, echo and crosstalk cancellation, data recovery, and error correction at a gigabit per second data rate. The devices achieve robust performance in noisy environments with very low power dissipation.

Lattice Semiconductor

The Alaska Ultra 88E1111/88E1112 features include:

- 10/100/100BASE-T IEEE 802.3 compliant
- Support for GMII, TBI, RGMII, RTBI, and SGMII
- Integrated 1.25GHZ SERDES for 1000BASE-X fiber applications
- The 88E1112 device also supports 100BASE-FX
- Four RGMII timing modes
- Three energy detect modes as well as a low power COMA mode
- Three loopback modes for diagnostics
- Fully integrated digital adaptive equalizers, echo cancellers, and crosstalk cancellers
- Advanced digital baseline wander correction
- Automatic polarity correction
- IEEE 802.3u compliant Auto-Negotiation
- CRC checker, packet counter
- Automatic detection of fiber or copper media
- Virtual Cable Tester (VCT)
- Selectable MDC/MDIO interface or Two-Wire Serial Interface

Test Equipment

Below is the equipment used in the interoperability tests:

Spirent SmartBits 2000 Protocol Analyzer

Spirent Communications' SmartBits 2000 (SMB-2000) has become the industry standard for measuring the performance limits of everything from an emerging technology in a development lab to the largest enterprise network. The SMB-2000 is widely used to test a variety of network devices and complex network configurations, including 10/100 Mbps Ethernet, Gigabit Ethernet, ATM, and Frame Relay.

Figure 2 illustrates the SMB-2000 analyzer with a 1000BASE-T copper module (GX-1420B, right-most module with RJ45 cable attached).

Figure 3 illustrates the GUI command console for the SMB-2000. The GX-1420B module is also shown to the right of the screen.

Figure 2. SmartBits 2000 Protocol Analyzer with 1000BASE-T Module

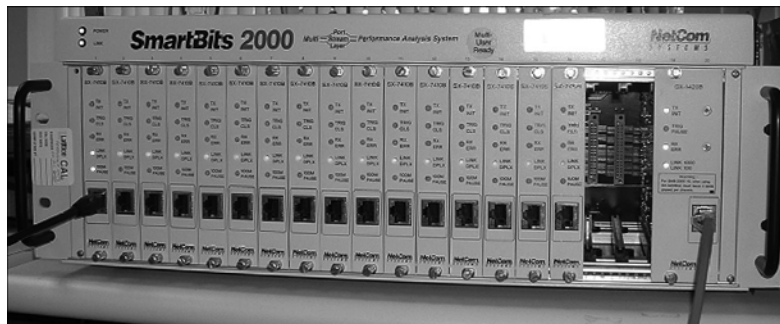
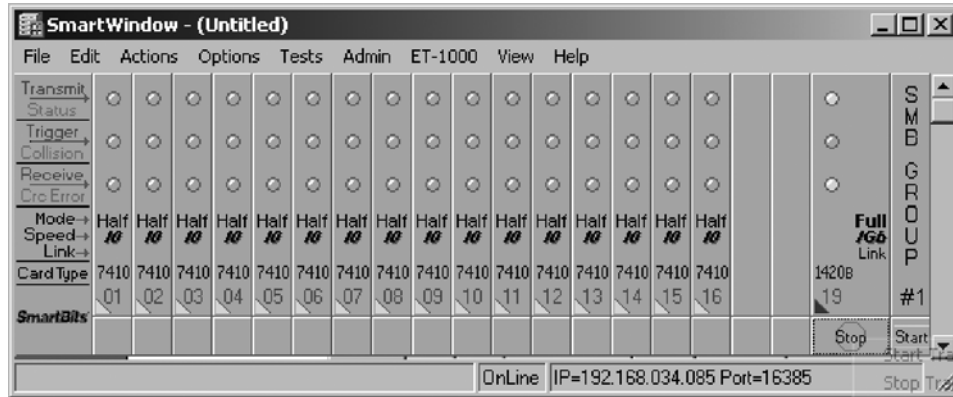


Figure 3. SmartBits 2000 GUI Controls



Marvell 88E1112 64 QFN Evaluation Board

The Marvell 88E1112 64 QFN Evaluation Board includes among others:

- An 88E1111 device
- An 88E1112 device
- On-board oscillator clock sources
- MDIO/MDC monitoring/control to both devices
- An SGMII interface between the 88E1111 and the 88E1112
- An RJ45 connector for MDI access to the 88E1111
- Two Transmit SMAs and two Receive SMAs for access to the 88E1112 SERDES

Marvell Alaska Virtual Cable Tester Software

The Alaska Virtual Cable Tester Software GUI is used to control the 88E1111/88E1112 parts and monitor status bits. Agilent 81130A Pulse/Data Generator

The Agilent 81130A pulse/data generator was used to supply an external 125MHz reference clock source to the LatticeSC flexiPCS.

For more information this module, please refer to Agilent’s website: www.agilent.com.

LatticeSC Evaluation Board

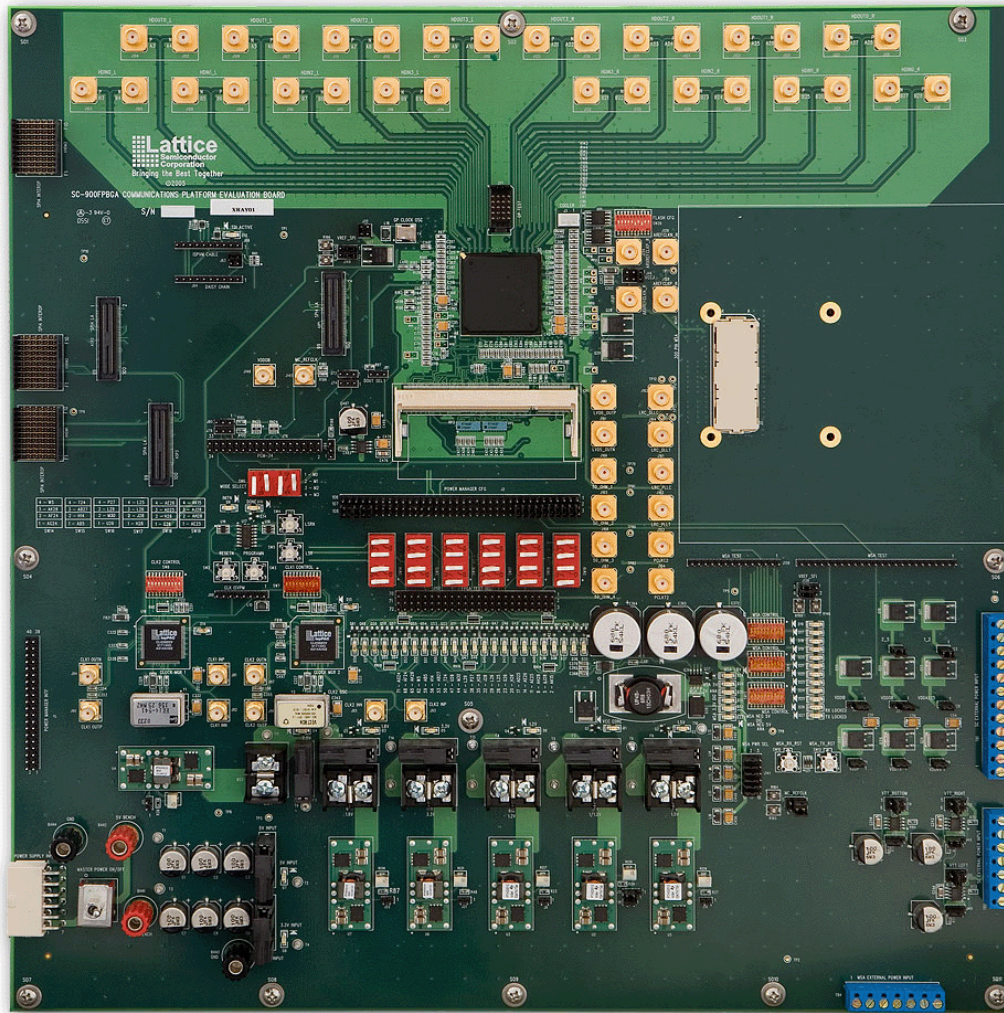
The LatticeSC Communications Board provides a stable yet flexible platform designed to help the user quickly evaluate the performance of the LatticeSC FPGA or aid in development of custom designs. Each LatticeSC communications board contains among others:

- An LFSC3GA25E-6F900C FPGA device
- SMA test points for high-speed SERDES and clock I/O
- On-board power connections and power sources
- An on-board interchangeable clock oscillator
- On-board reference clock management using Lattice ispClock™ devices
- Various high-speed layout structures
- On-board Flash configuration memory

- Various LEDs, switches, connectors, headers, SMA connections for external clocking, and on-board power control

Figure 4 shows the LatticeSC Communications board.

Figure 4. LatticeSC Communications Board



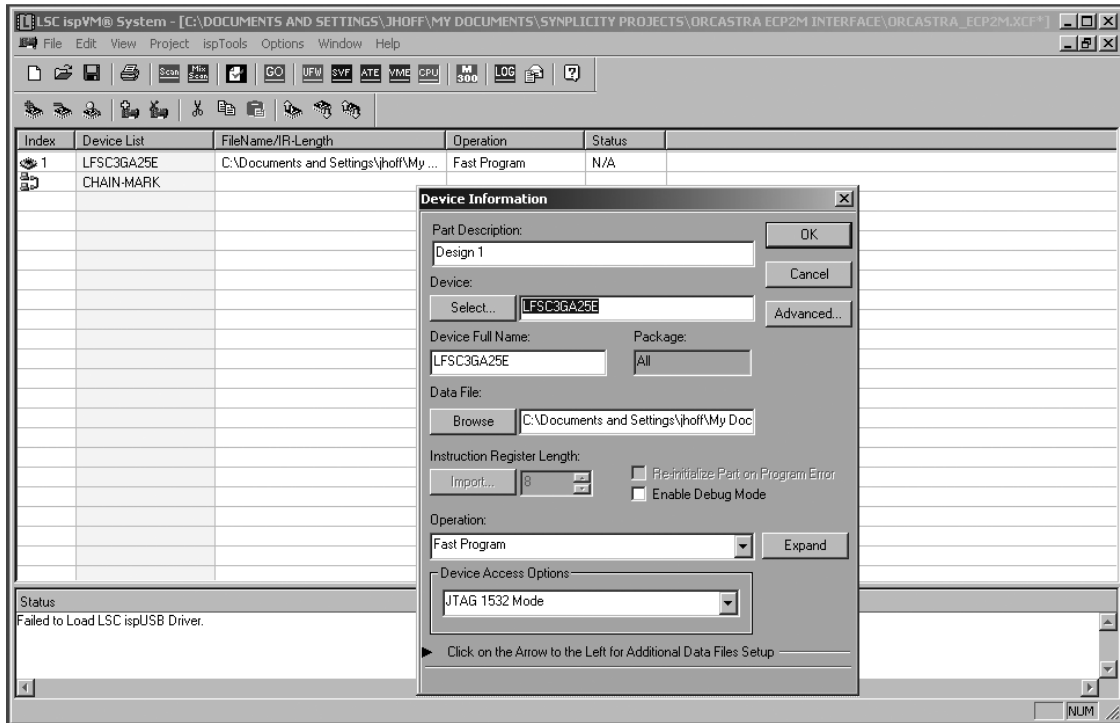
ispVM[®] System Software

The ispVM System is included with Lattice’s ispLEVER[®] software, and is also available as a stand-alone device programming manager. The ispVM System is a comprehensive design download package that provides an efficient method of programming ISP[™] devices using JEDEC and bitstream files generated by Lattice Semiconductor, and other, design tools. This complete device programming tool allows the user to quickly and easily download designs through an ispSTREAM to devices and includes features that facilitate ispATE, ispTEST, and ispSVF programming as well as gang-programming with DLxConnect.

The ispVM System is used in this interoperability test to download the LatticeSC bitstream to configure the FPGA in Gigabit Ethernet mode.

Figure 5 shows a screen shot of the ispVM System.

Figure 5. ispVM System



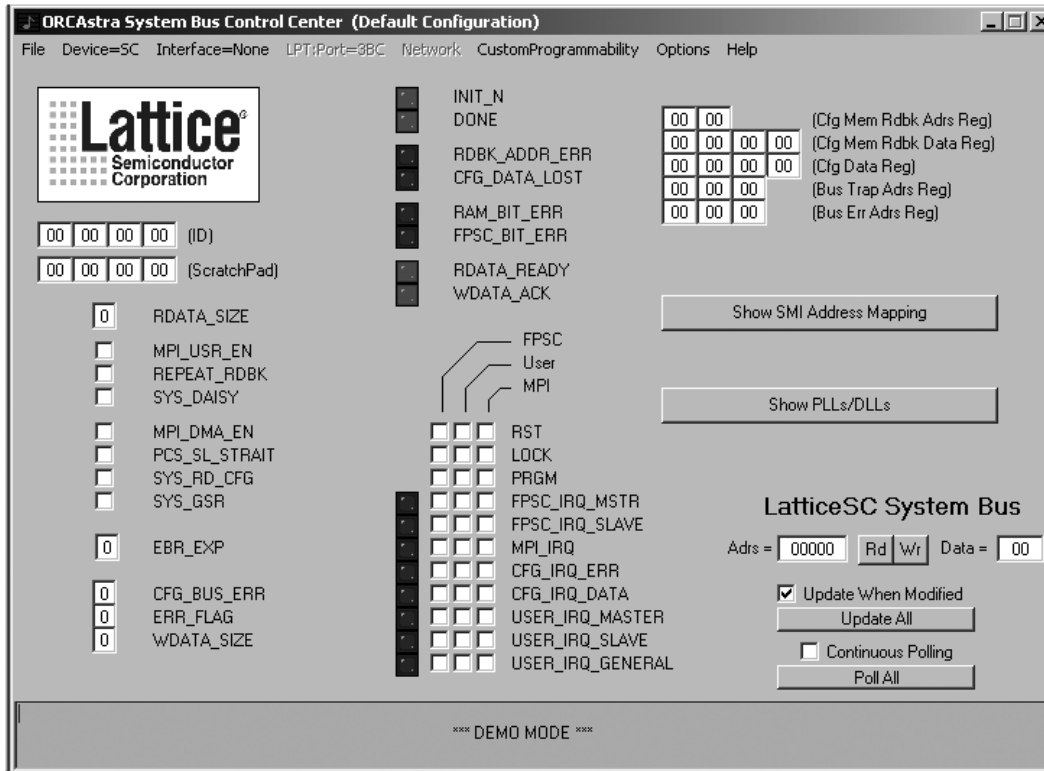
ORCAstra System

The Lattice ORCAstra software is a PC-based graphical user interface that allows the user to configure the operational mode of an FPGA or FPSC by programming control bits in the on-chip registers. This helps users quickly explore configuration options without going through a lengthy re-compile process or making changes to their board.

Configurations created in the GUI can be saved to memory and re-loaded for later use. A macro capability is also available to support script-based configuration and testing. The GUI can also be used to display system status information in real time. Use of the ORCAstra software does not interfere with the programming of the FPGA portion of the FPSC.

Figure 6 is a screen shot of ORCAstra system

Figure 6. ORCAstra System



Interoperability Testing

This section provides details on Gigabit Ethernet Physical Layer interoperability tests between a LatticeSC device and the MARVELL 88E1111/ 88E1112 devices. The purpose of these tests is to confirm the correct processing of 1000BASE-T copper protocol from the SMB-2000, through the 88E1111/88E1112 devices, and ending at the LatticeSC 1000BASE-X device, and then back in the other direction. Particularly, the tests verify:

- The ability to transfer packets across the system in an asynchronous way.
- The ability to handle random length packets.

Test Setup

Figure 7 shows the test setup. Figure 8 is a block diagram of the test setup.

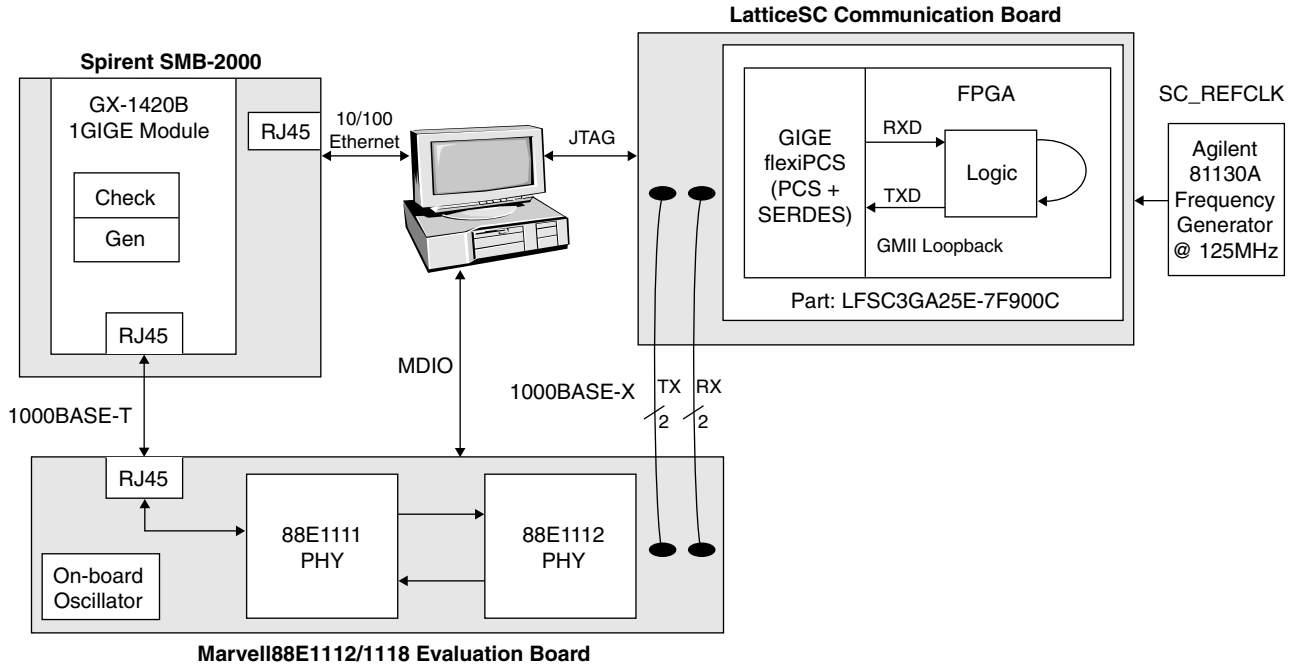
The set-up includes:

- A Spirent SMB-2000 with a GX-1420B module
- Marvell 88E1112 evaluation board (with the 88E1111/88E1112 parts)
- LatticeSC Communications Platform evaluation board
- A PC for software control/monitoring
- The Agilent 811130A Data/Pulse Generator to provide an external 125MHZ reference clock to the LatticeSC flex-iPCS

Figure 7. Test Setup



Figure 8. Test Setup Block Diagram



Test Description

The following describes how the Gigabit Ethernet Physical Layer Interoperability is achieved:

SMB-2000

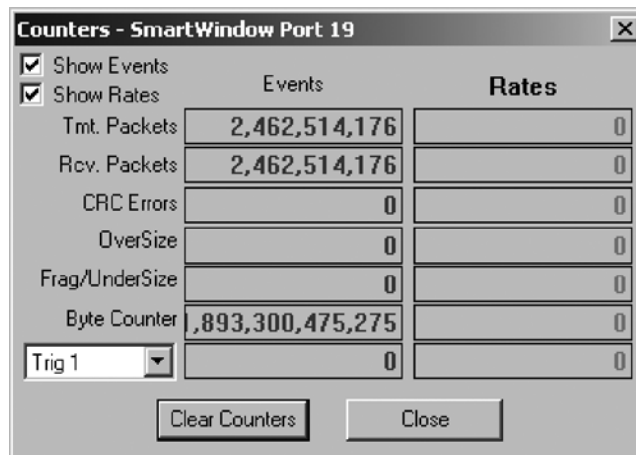
The GX-1420B module generates and checks full protocol compliant gigabit ethernet packets. The setup is as follows:

- Random source/destination addresses
- Random payload content
- Random payload length
- 0.096uSec IPG GAP

Figure 9 illustrates the SMB-2000 counter window used to keep track of transmission and reception statistics.

The SMB-2000 connects to the Marvell 88E1112/ 88E1118 EVAL Board via an RJ45 cable. It transmits the gigabit Ethernet packets to the 88E1111 device in the TX direction, and checks them back from the 88E1111 device in the RX direction.

Figure 9. SMB-2000 Counter Window



Marvell 88E1112/88E111 Evaluation Board

In one direction, the 88E1111 device receives 1000BASE-T packets from the SMB-2000 and sends it to the 88E1112 device via its SGMII interface. In the other direction, the opposite flow of data occurs.

In one direction, the 88E1112 part receives SGMII packets from the 88E1111 and sends it to the LatticeSC board via SMAs on its 1000BASE-X interface. In the other direction, the opposite flow of data occurs.

LatticeSC Communications Platform Evaluation Board

In the RX direction, the LatticeSC SERDES recovers the 1000BASE-X packets from the 88E1112 device and the flexiPCS converts them into GMII format.

The GMII loopback logic in the FPGA portion loops the GMII data back into the TX direction. The LatticeSC device then transmits the 1000BASE-X packets back to the 88E1112 device.

Results

The Smartbits SMB-2000 GX-1420B counter window (as shown in Figure 9) was monitored for error-free packet transmission and reception. Additionally, the Marvell ALASKA Virtual Cable Tester Software GUI and the Lattice

ORCAstra System GUI (as shown in Figure 6) were also monitored for proper link synchronization across the system. The setup ran for over four hours, during which about 2.4 billion packets were transmitted/received error-free (see Figure 9).

Summary

In conclusion, the LatticeSC FPGA family offers users built-in Gigabit Ethernet Physical Layer support and is fully inter-operable with Marvell 88E1111/88E1112 devices.

Technical Support Assistance

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 +1-503-268-8001 (Outside North America)
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Internet: www.latticesemi.com

Revision History

| Date | Version | Change Summary |
|--------------|---------|---|
| August 2006 | 01.0 | Initial release. |
| October 2008 | 01.1 | Removed Marvell 88E1112 board photo. |
| | | Removed Alaska Virtual Cable Tester Software GUI screen shot. |