iCE40 Hardware Checklist

Technical Note

FPGA-TN-02006-1.8

April 2020

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
CRAM	Configuration RAM
PLL	Phase Locked Loop
POR	Power-on-Reset
NVCM	Non-volatile Configuration Memory

1. Introduction

When designing complex hardware using the iCE40™ device family (iCE40 LP/HX, iCE40LM, iCE40 Ultra™, iCE40 UltraLite™, iCE40 UltraPlus™), designers must pay special attention to critical hardware configuration requirements. This technical note steps through these critical hardware requirements related to the iCE40 device. This document does not provide detailed step-by-step instructions but gives a high-level summary checklist to assist in the design process.

The iCE40 ultra-low power, non-volatile devices are available in four versions – LP series for low power applications, HX series for high performance applications, LM and Ultra/UltraLite/UltraPlus series for ultra-low power for mobile applications.

This technical note assumes that the reader is familiar with the iCE40 device features as described in the following documents:

- iCE40LP/HX Family Data Sheet (FPGA-DS-02029)
- iCE40LM Family Data Sheet (FPGA-DS-02043)
- iCE40 Ultra Family Data Sheet (FPGA-DS-02028)
- iCE40 UltraLite Family Data Sheet (FPGA-DS-02028)
- iCE40 UltraPlus Family Data Sheet (FPGA-DS-02008)

The critical hardware areas covered in this technical note include:

- Power supplies as they relate to the supply rails and how to connect them to the PCB and the associated system
- Configuration and how to connect the configuration mode selection
- Device I/O interface and critical signals

2. Power Supply

The VCC (core supply voltage) VCCIO_2, SPI_VCC and VPP_2V5 determine the iCE40 device's stable condition. These supplies need to be at a valid and stable level before the device can become operational. Refer to the family data sheets for voltage requirements.

In order to evenly balance the stress in the solder joints, Lattice recommends that PCB solder pads match the corresponding package solder pad type and dimensions. If a different PCB solder pad type is used, the recommended pad dimension is based on an equivalent surface contact area.

Table 2.1. Power Supply Description and Voltage Levels

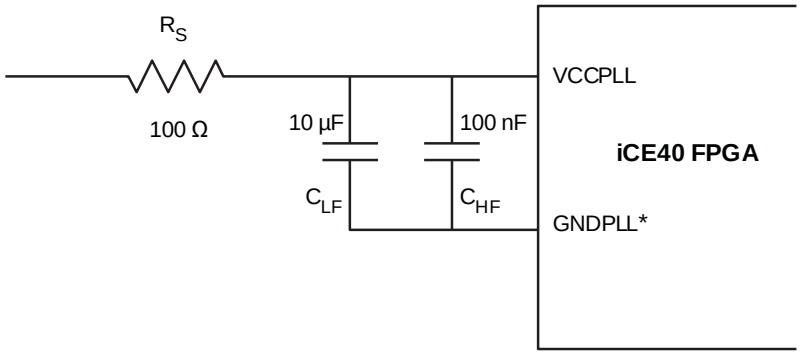
Supply[3, 4]	Voltage (Nominal Value)	Description
VCC	1.20 V	Core supply voltage
VCCIO_X	1.5 V to 3.3 V	Power supply for I/O banks
VPP_2V5	2.5 V	NVCM programming and operating supply voltage
VPP_FAST5	Leave unconnected	Optional fast NVCM programming supply
SPI_VCC	1.8 V to 3.3 V	SPI interface supply voltage
VCCPLL1, 2	1.2 V	Analog voltage supply to Phase Locked Loop (PLL)

Notes:

1. VCCPLL must be tied to VCC when PLL is not used.
2. External power supply filter required for VCCPLL and GNDPLL.
3. iCE40LM family devices do not have VPP_2V5 and VPP_FAST supplies.
4. iCE40 Ultra/iCE40 UltraLite/iCE40 UltraPlus family devices do not have VPP_FAST.
5. VPP_FAST, used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the VPP_FAST ball connected to VCCIO_0 ball externally.

3. Analog Power Supply Filter for PLL

The iCE40 sysCLOCK™ PLL contains analog blocks, so the PLL requires a separate power and ground that is quiet and stable to reduce the output clock jitter of the PLL on device with external VCCPLL supply pins (PLL is not offered in some device/package combinations without the VCCPLL ball. Please refer to the data sheet and the device family Pin List to check the availability of VCCPLL ball.) The sysCLOCK PLL has the DC ground connection made on the FPGA, so the external PLL ground connection (GNDPLL) must NOT be connected to the board's ground. Figure 3.1 also includes sample values for the components that make up the PLL power supply filter.



*Note that GNDPLL should not be connected to the board's ground.

Figure 3.1. Isolating PLL Supplies

3.1. Configuration Considerations

The iCE40 LP/HX/Ultra/UltraLite/UltraPlus devices contain two types of memory, CRAM (Configuration RAM) and NVCM (Non-volatile Configuration Memory). The iCE40LM device contains only the CRAM. CRAM memory contains the active configuration. The NVCM provides on-chip storage of configuration data. It is one-time programmable and is recommended for mass-production.

For more information, refer to iCE40 Programming and Configuration (FPGA-TN-02001).

The configuration and programming of the iCE40 LP/HX/LM/Ultra/UltraLite/UltraPlus devices from external memory is using the SPI port, both in Master and Slave modes. In Master SPI mode, the device configures its CRAM from an external SPI Flash connected to it. In Slave mode, the device can be configured or programmed using the Lattice Diamond® Programmer or embedded processor.

On the iCE40LP/HX and iCE40 Ultra/UltraLite/UltraPlus family devices, the SPI_SS_B determines if the iCE40 CRAM is configured from an external SPI (SPI_SS_B=0) or from the NVCM (SPI_SS_B=1). This pin is sampled after Power-on-Reset (POR) is released or CRESET_B is held low or toggled (High-Low-High).

Table 3.1. Configuration Pins

Pin Name	Function	Direction	External Termination	Notes
CRESET_B	Configuration Reset input, active low.	Input	10 kΩ pull-up to VCCIO_X*.	A low on CRESET_B delay's configuration.
CDONE	Configuration Done output from iCE40.	Output	Pull-up to VCCIO_X*. The maximum Rpullup value is calculated as follows: Rpullup=1/(2 X ConfigFrequency X CDONETraceCap)	—
SPI_VCC	SPI interface supply voltage.	Supply	—	—
SPI_SI	SPI serial input to the iCE40, in both Master and Slave modes.	Input	—	Released to user I/O after configuration.

Pin Name	Function	Direction	External Termination	Notes
SPI_SO	SPI serial output from the iCE40, in both Master and Slave modes.	Output	—	Released to user I/O after configuration.
SPI_SCK	SPI clock	Input/Output	10 kΩ pull-up to VCC_SPI recommended.	Direction based on Master or Slave modes. Released to user I/O after configuration.
SPI_SS_B	Chip select	Input (Slave mode)/ Output (Master mode)	10 kΩ pull-up to VCC_SPI in Master mode and a 10 kΩ pull-down in Slave mode is recommended if not driven by a processor.	Refer to iCE40 Programming and Configuration (FPGA-TN-02001) for more details.

***Note:** Refer to the package pinlist document of each device to determine the correct VCCIO bank.

3.2. SPI Flash Requirement in Master SPI Mode

Users are free to select any industry standard SPI Flash. The SPI Flash must support the 0x0B Fast Read command, using a 24-bit start address with eight dummy bits before the PROM provides first data. Refer to iCE40 Programming and Configuration (FPGA-TN-02001) for additional information.

4. LVDS Pin Assignments (For iCE40LP/HX Devices Only)

The differential inputs are supported only by Bank 3; however, differential outputs are supported in all banks.

5. Checklist

Table 5.1. iCE40 Hardware Checklist

	iCE40 Hardware Checklist Item	OK	N/A
1	Power Supply		
1.1	Core supply VCC at 1.2 V		
1.2	I/O power supply VCCIO 0-3 at 1.5 V to 3.3 V		
1.3	SPI_VCC at 1.8 V to 3.3 V		
1.4	VCCPLL pulled to VCC even if PLL not used		
1.5	Power supply filter for VCCPLL and GNDPLL		
1.6	GNDPLL must NOT be connected to the board		
2	Power-on-Reset (POR) inputs		
2.1	VCC		
2.2	SPI_VCC		
2.3	VCCIO_0-3		
2.4	VPP_2V5		
	VPP_FAST		
3	Configuration		
3.1	Configuration mode based on SPI_SS_B		
3.2	Pull-up on CRESET_B,CDONE pin		
3.3	TRST_B is kept low for normal operation		
4	I/O pin assignment		
4.1	LVDS pin assignment considerations		

Technical Support Assistance

Submit a technical support case via www.latticesemi.com/techsupport.

Revision History

Revision 1.8, April 2020

Section	Change Summary
Disclaimers	Added this section.
Acronyms in This Document	Added this section.
Power Supply	Updated Table 3.1. Configuration Pins. Changed *VCCIO_2* to *VCCIO_X* and added footnote.
All	• Updated document IDs of referenced data sheets and technical notes. • Minor changes in formatting/styles.

Revision 1.7, December 2016

Section	Change Summary
All	• Changed document number from TN1252 to FPGA-TN-02006. • Updated document template.

Revision 1.6, June 2016

Section	Change Summary
All	Added support for iCE40 UltraPlus.
Introduction	Updated Introduction section. Added reference to FPGA-DS-02008, iCE40 UltraPlus Family Data Sheet.
Power Supply	Updated Power Supply section. Revised Table 2.1, Power Supply Description and Voltage Levels. Added footnote 5 to VPP_FAST.
Analog Power Supply Filter for PLL	Updated Analog Power Supply Filter for PLL section. Revised Figure 3.1, Isolating PLL Supplies. Changed 100 W to 100 Ohms.
Configuration Considerations	Updated Configuration Considerations section. Revised Table 3.1, Configuration Pins. Updated SPI_SS_B External Termination.
Technical Support Assistance	Updated Technical Support Assistance section.

Revision 1.5, January 2015

Section	Change Summary
All	Added support for iCE40 UltraLite.

Revision 1.4, June 2014

Section	Change Summary
All	Added support for iCE40 Ultra.
Analog Power Supply Filter for PLL	Updated Analog Power Supply Filter for PLL section.
Configuration Considerations	Updated Configuration Considerations section. Updated Table 3.1, Configuration Pins. Changed VCCIO_2 to VCC_SPI in SPI_SCK and SPI_SS_B.

Revision 1.3, October 2013

Section	Change Summary
Configuration Considerations	Updated Configuration Considerations section. Updated Table 3.1, Configuration Pins.
Technical Support Assistance	Updated Technical Support Assistance information.

Revision 1.2, December 2012

Section	Change Summary
Power Supply	Updated Power Supply section. Revised Table 2.1, Power Supply Description and Voltage Levels. Corrected VCC nominal voltage.

Revision 1.1, September 2012

Section	Change Summary
LVDS Pin Assignments (For iCE40LP/HX Devices Only)	Updated LVDS Pin Assignments (For iCE40LP/HX Devices Only) text section. Corrected description of differential input and output support.

Revision 1.0, September 2012

Section	Change Summary
All	Initial release.

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