ECP5 and ECP5-5G Hardware Checklist

Technical Note

FPGA-TN-02038-1.6

October 2020

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS and with all faults, and all risk associated with such information is entirely with Buyer. Buyer shall not rely on any data and performance specifications or parameters provided herein. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. No Lattice products should be used in conjunction with mission- or safety-critical or any other application in which the failure of Lattice's product could create a situation where personal injury, death, severe property or environmental damage may occur. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Contents

Tables

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
BGA	Ball Grid Array
CML	Current-Mode Logic
LUT	Look Up Table
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
PCB	Printed Circuit Board

1. Introduction

When designing complex hardware using the ECP5™ and ECP5-5G™ FPGA, you must pay special attention to critical hardware configuration requirements. This technical note steps through these critical hardware implementation items relative to the ECP5 and ECP5-5G device. The document does not provide detailed step-by-step instructions but gives a high-level summary checklist to assist in the design process.

The device family consists of FPGA LUT densities ranging from 25K to 85K. This technical note assumes that the reader is familiar with the ECP5 and ECP5-5G device features as described in ECP5 and ECP5-5G Family Data Sheet (FPGA-DS-02012). The data sheet includes the functional specification for the device. Topics covered in the data sheet include but are not limited to the following:

- High-level functional overview
- Pinouts and packaging information
- Signal descriptions
- Device-specific information about peripherals and registers
- Electrical specifications

Refer to ECP5 and ECP5-5G Family Data Sheet (FPGA-DS-02012) for details. The critical hardware areas covered in this technical note are:

- Power supplies as they relate to the ECP5 and ECP5-5G power supply rails and how to connect them to the PCB and the associated system
- Configuration mode selection for proper power-up behavior
- Device I/O interface and critical signals

Important: You should refer to the following documents for detailed recommendations.

- ECP5 and ECP5-5G sysCONFIG Usage Guide (FPGA-TN-02039)
- ECP5 and ECP5-5G SERDES/PCS Usage Guide (FPGA-TN-02206)
- ECP5 and ECP5-5G sysIO Usage Guide (FPGA-TN-02032)
- ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide (FPGA-TN-02200)
- ECP5 and ECP5-5G Memory Usage Guide (FPGA-TN-02204)
- ECP5 and ECP5-5G High-Speed I/O Interface (FPGA-TN-02035)
- Power Consumption and Management for ECP5 and ECP5-5G Devices (FPGA-TN-02210)
- ECP5 and ECP5-5G sysDSP Usage Guide (FPGA-TN-02205)
- Electrical Recommendations for Lattice SERDES (FPGA-TN-02077)
- High-Speed PCB Design Considerations (FPGA-TN-02024)
- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02210)
- LatticeSC SERDES Jitter (TN1084)
- ECP5 and ECP5-5G-related pinout information can be found on the Lattice website.
- HSPICE SERDES simulation package (available under NDA, contact the license administrator at lic_admin@latticesemi.com)

2. Power Supplies

The V_{CC}, V_{CCAUX}, and V_{CCIO8} power supplies are monitored to determine the ECP5 and ECP5-5G internal *power good* condition during power-up. These supplies need to be at a valid and stable level before the device can become operational and be configured. All other VCCIOX are not monitored during power-up, but need to be at valid and stable level before the device is configured and entered into User Mode. Several other supplies including V_{CCA}, V_{CCAUXA}, V_{CCHRX}, and V_{CCHTX} are used in conjunction with on-board SERDES on LFE5UM/LFE5UM5G devices. Table 2.1 lists the power supplies and the appropriate voltage levels for each supply.

Table 2.1. ECP5 and ECP5-5G FPGA Power Supplies

Supply	Voltage (Nominal Value)	Description
V_{CC}	V (LFE5U/5UM) V (LFE5UM5G)	FPGA core power supply.
V_{CCA}	V (LFE5UM) V (LFE5UM5G)	Analog power supply for SERDES blocks (For LFE5UM/LFE5UM5G devices). Should be isolated and *clean* from excessive noise.
V_{CCAUX}	2.5 V	Auxiliary power supply
$V_{CCIO[0\text{-}4,\ 6\text{-}8]}$[1]	1.2 V to 3.3 V	I/O power supply. Seven (eight on LFE5/LFE5UM5G-85 in 756 and 554 caBGA) general purpose I/O banks. Each bank has its own V_{CCIO} supply: V_{CCIO8} is used in conjunction with pins dedicated and shared with device configuration, include JTAG. $V_{CCIO1,\ 2,\ 3,\ 4,\ 6}$, and V_{CCIO7} are optionally used based on per bank usage of I/O.
V_{CCHRX}	V (LFE5UM) V (LFE5UM5G)	Input terminate voltage supply for SERDES inputs (For LFE5UM/LFE5UM5G devices)
V_{CCHTX}	V (LFE5UM) V (LFE5UM5G)	Output driver/termination voltage supply for SERDES outputs (for LFE5UM/LFE5UM5G devices)
V_{CCAUXA}	2.5 V	Auxiliary power supply for SERDES (for LFE5UM/LFE5UM5G devices)

Note: Bank 4 exists only on the LFE5/LFE5UM5G-85 device in 756 caBGA and 554 caBGA. It is not available in any other device/package combinations. When migrating LFE5/LFE5UM5G-85 to lower density devices, I/O on Bank 4 cannot be used.

The ECP5 and ECP5-5G FPGA device has a power-up reset state machine that monitors various power supplies.

These supplies should come up monotonically. The on-chip Power-On-Reset (POR) is de-asserted when the following conditions are met:

- V_{CC} reaches 0.9 V or above
- V_{CCAUX} reaches 2.0 V or above
- V_{CCIO8} reaches 0.95 V or above

Initialization of the device does not proceed until the last power supply above has reached its minimum operating voltage.

2.1. ECP5 and ECP5-5G SERDES/PCS Power Supplies

Supplies dedicated to the operation of the SERDES/PCS include V_{CCA}, V_{CCAUXA}, V_{CCHRX}, and V_{CCHTX}. All V_{CCA} supply pins must always be powered to the recommended operating voltage range with the LFE5UM/LFE5UM5G devices. However, if no SERDES is used at all in these devices, all power supply pins for the SERDES can be connected to GND (V_{CCA}, V_{CCAUXA}, V_{CCHRX}, and V_{CCHTX}).

Each ECP5 and ECP5-5G device has up to four SERDES channels. Each group of two SERDES channels makes up a Dual Channel Unit (DCU), also referred to as a dual.

- When one SERDES channel within a DCU is used, the unused channel within the same DCU's V_{CCA} and V_{CCHTX} should be connected to the appropriate power rail. Other power rails can be left open.
- When one SERDES channel within a DCU is used, the second unused DCU's V_{CCA} should be connected to the appropriate power rail. Other power rails can be left open.
- When both DCUs are not used, both DCU's V_{CCA} should be connected to the appropriate power rail. Other power rails can be left open.

On migrating across the ECP5, ECP5UM, and ECP5UM5G devices on same package, refer to the LFE5U to LFE5UM/LFE5UM5G and LFE5UM to LFE5UM5G Migration section for more details.

It is very important that the VCCA supply be low-noise and isolated from heavily loaded switching supplies. Refer to Electrical Recommendations for Lattice SERDES (FPGA-TN-02077) for recommendations.

2.2. Power Estimation

Once the ECP5 and ECP5-5G device density, package and logic implementation is decided, power estimation for the system environment should be determined based on the Power Calculator provided as part of the Lattice Diamond® design tool. When estimating power, you should keep two goals in mind:

- Power supply budgeting should be based on the maximum of the power-up in-rush current, configuration current and maximum DC and AC current for the given system's environmental conditions.
- The ability for the system environment and ECP5 and ECP5-5G device packaging to be able to support the specified maximum operating junction temperature. By determining these two criteria, the ECP5 and ECP5-5G device power requirements are taken into consideration early in the design phase.

3. Configuration Considerations

The ECP5 and ECP5-5G device includes provisions to configure the FPGA via the JTAG interface or several modes utilizing the sysCONFIG port. The JTAG port includes a 4-pin interface. The interface requires the following PCB considerations.

Table 3.1. JTAG Pin Recommendations

JTAG Pin	PCB Recommendation
TDI	4.7 kΩ pull-up to V_{CCIO8}
TMS	4.7 kΩ pull-up to V_{CCIO8}
TDO	4.7 kΩ pull-up to V_{CCIO8}
TCK	4.7 kΩ pull-down to GND

Every PCB is recommended to have easy access to FPGA JTAG pins, even if the primary configuration interface is not using the JTAG port. This JTAG port enables debugging in the final system. For best results, route the TCK, TMS, TDI, and TDO signals to a common test header along with V_{CCIO8} and ground.

Using JTAG for configuration, the MODE pins are not used. Using other programming modes requires the use of the CFG[2:0] input pins. The CFG[2:0] pins include internal weak internal pull-ups. It is recommended that 1-10 kΩ external resistors be used when using these sysCONFIG modes. Pull-up resistors should be connected to V_{CCIO8}.

External resistors are always needed if the configuration signals are being used to handshake with other devices. Recommended pull-up resistors to V_{CCIO8} and pull-down to board ground should be used on the following pins.

Table 3.2. Pull-up/Pull-down Recommendations for Configuration Pins

Pin	PCB Connection
PROGRAMN	4.7 kΩ pull-up to V_{CCIO8}
INITN	4.7 kΩ pull-up to V_{CCIO8}
MCLK/CCLK	1 kΩ pull-up to V_{CCIO8}
CSSPIN	4.7 kΩ to 10 kΩ pull-up to V_{CCIO8}
CFG[2:0]	1 kΩ to 10 kΩ pull-up to V_{CCIO8}, 0 = GND. See Table 3.3.

Table 3.3. Configuration Pins Needed per Programming Mode

Configuration Mode	Bus Size	Dedicated CFG[2:0]	Clock		Shared Pins	Dedicated Pins
			Pin	I/O		
SSPI	1 Bit	001	CCLK	Input	MISO, MOSI, SI, DOUT,	PROGRAMN, INITN, DONE
MSPI	1 Bit	010	MCLK	Output	MISO, MOSI, CSSPIN, DOUT	PROGRAMN, INITN, DONE
	2 Bits				D[1:0], CSSPIN, DOUT	
	4 Bits				D[3:0], CSSPIN, DOUT	
SCM	1 Bit	101	CCLK	Input	DI, DOUT	PROGRAMN, INITN, DONE
SPCM (Parallel)	8 Bits	111	CCLK	Input	D[7:0], DOUT, CSON, BUSY, WRITEN, CSN, CS1N	PROGRAMN, INITN, DONE
JTAG	1 Bit	xxx	TCK	Input	—	TCK, TMS, TDI, TDO

4. I/O Pin Assignments

The V_{CCA} provides a *quiet* supply for the SERDES blocks. For the best jitter performance, careful pin assignment keeps *noisy* I/O pins away from *sensitive* pins. The leading causes of PCB related SERDES crosstalk is related to FPGA outputs located in close proximity to the sensitive SERDES power supplies. These supplies require cautious board layout to insure noise immunity to the switching noise generated by FPGA outputs. Guidelines are provided to build quiet filtered supplies for the VCCA, however, robust PCB layout is required to insure that noise does not infiltrate into these analog supplies.

Although coupling has been reduced in the device packages of ECP5 and ECP5-5G devices where little crosstalk is generated, the PCB board can cause significant noise injection from any I/O pin adjacent to SERDES data, reference clock, and power pins as well as other critical I/O pins such as clock signals. Electrical Recommendations for Lattice SERDES (FPGA-TN-02077) provides detailed guidelines for optimizing the hardware to reduce the likelihood of crosstalk to the analog supplies. PCB traces running in parallel for long distances need careful analysis. Simulate any suspicious traces using a PCB crosstalk simulation tool to determine if they cause problems.

It is common practice for you to select pinouts for their system very early in the design cycle. For the FPGA designer, this requires a detailed knowledge of the targeted FPGA device. You can use a spreadsheet program to initially capture the list of the design I/O. Lattice Semiconductor provides detailed pinout information that can be downloaded from the Lattice Semiconductor website in .csv format for you to use as a resource to create pinout information. For example, by navigating to the pinout.csv file, you can gather the pinout details for all the different package offerings of the device in the family, including I/O banking, differential pairing, Dual Function of the pins, and input and output details.

5. Clock Inputs

The ECP5 and ECP5-5G devices provide clock inputs called PCLK. All clock inputs (PCLK) are shared with General Purpose I/O on dual function pins. When the pin is not used for clocking (PCLK), it can be used as a General Purpose I/O pin.

However, when these pins are used for clocking purposes, noise needs to be minimized on these pins. Refer to ECP5 and ECP5-5G High-Speed I/O Interface (FPGA-TN-02035).

These clock input pins can be found under the Dual Function column of the pinout csv file located on the Lattice website and in the pin assignment tab of Diamond software's Spreadsheet View.

6. Pinout Considerations

The ECP5 and ECP5-5G supports many applications with high-speed interfaces. These include various rule-based pinouts that need to be understood prior to implementation of the PCB design on these high-speed interfaces. The pinout selection must be completed with an understanding of the interface building blocks implemented in the FPGA fabric. These include IOLOGIC blocks such as DDR, clock resource connectivity, and PLL and DLL usage. Refer to ECP5 and ECP5-5G High-Speed I/O Interface (FPGA-TN-02035) for rules pertaining to these interface types.

7. LVDS Pin Assignments

True LVDS inputs and outputs are available on I/O pins on the left and right sides of the devices. Top and I/O banks do not support True LVDS standard, but can support emulated LVDS outputs. True LVDS input pairing on left and right banks can be found under the Differential column in the pinlist csv file. True LVDS output pair are available on any A and B pair of the left and right banks.

Emulated LVDS output are available on pairs around all banks, but this requires external termination resistors. This is described in ECP5 and ECP5-5G sysIO Usage Guide (FPGA-TN-02032).

8. HSUL and SSTL Pin Assignments

The HSUL and SSTL interfaces are referenced I/O standards require an external reference voltage. The VREF pin(s) should get high priority when assigning pins on the PCB. These pins can be found in the Dual Function column with VREF1 label. Each bank includes a separate VREF voltage. VREF1 sets the threshold for the referenced input buffers. Each I/O is individually configurable based on the bank's supply and reference voltages.

9. SERDES Pin Considerations

High-speed signaling requires careful PCB design. Maintaining good transmission line characteristics is a requirement. A continuous ground reference should be maintained with high-speed routing. This includes tightly matched differential routing with very few discontinuities. Refer to High-Speed PCB Design Considerations (FPGA-TN-02024) for the suggested methods and guidance.

For unused SERDES channels, the input pins can be left open.

10. LFE5U to LFE5UM/LFE5UM5G and LFE5UM to LFE5UM5G Migration

Besides migrating design from one device to another device (that is LFE5U-25 to LFE5U-45) on same package (that is caBGA554) within its own family in LFE5U and LFE5UM/LFE5UM5G, you can migrate from the non-SERDES (LFE5U) device to SERDES (LFE5UM) device, or migrating from LFE5UM device to LFE5UM5G device in the same package.

If you anticipate your design, you may use SERDES at a later time on your product. You can first design and make all the connections to all SERDES circuit on board.

For example, if you anticipate the need to use the two Dual SERDES on LFE5U-85 product, you have to design your board with LFE5UM, which contains the SERDES ports, to the not-yet-populated SERDES circuit on the board. This requires all SERDES power pins to be connected to power sources on the board, with the corresponding pins found on the LFE5U device. Note that these power pins on the ECP5U devices are required to be connected to GND when migrating to LFE5UM is not considered, but they need to be connected to SERDES power supplies when future migration is considered. He can still put in the LFE5U-85 device because the two devices are pin compatible, other than the SERDES pins and SERDES power supply pins. Also, to be taken into account, ensure the SERDES power supplies are isolated and implemented with different power rails to minimize any noise injection from other supplies.

When designing the board with LFE5UM and plan for future migration to LFE5UM5G to increase the SERDES throughput to 5G, care has to be taken that the V_{CC}/V_{CCA}/V_{CCHRX}/V_{CCHTX} need to be powered by 1.2 V nominal supply voltage for LFE5UM5G. Voltage regulators with adjustable voltage between 1.1 V and 1.2 V are needed when selecting to populate the board with either the LFE5UM or LFE5UM5G device.

The other consideration to migrate between the LFE5UM and LFE5UM5G devices is to ensure the signal quality of the Rx and Tx traces, which needs to be good for 5 Gbps operation.

Another consideration when migrating between the LFE5UM and LFE5UM5G devices is that if the reference clock supply from a source that cannot be changed, such as PCIe slot clock (100 MHz), the clock input to the LFE5UM5G needs 2X frequency of this clock source. An external clock generator, such as PLL, needs to be used to double this clock frequency (to 200 MHz) when used with LFE5UM5G device.

Table 10.1. Hardware Checklist

	Item	OK	NA
1	**FPGA Power Supplies**		
1.1	V_{CC} core @ 1.1 V ±5% (LFE5U/LFE5UM), @ 1.2 V +/- 5% (LFE5UM5G)		
1.1.1	Use a PCB plane for V_{CC} core with proper decoupling		
1.1.2	V_{CC} core sized to meet power requirement calculation from software		
1.2	All V_{CCIO} are between 1.2 V to 3.3 V		
1.2.1	V_{CCIO8} used with configuration interfaces (that is memory devices). Need to match specifications.		
1.2.2	V_{CCIO}[1:7] used based on user design		
1.3	V_{CCAUX} @ 2.5 V ±5%		
1.4	Power estimation		
2	**SERDES Power Supplies**		
2.1	V_{CCHRX} and V_{CCHTX} connected for USED SERDES channels		
2.2.1	V_{CCHTX} are at 1.1 V ±5% (LFE5UM), 1.2 V ±5% (LFE5UM5G)		
2.2.2	V_{CCHRX} are from 0.3 V to 1.1 V +5% (LFE5UM), 0.3 V to 1.2 V +5% (LFE5UM5G)		
2.3	V_{CCA} @ 1.1 V ±5% (LFE5UM), @1.2 V ±3% (LFE5UM5G)		
2.3.1	V_{CCAUXA} @ 2.5 V ±5%		
2.3.2	V_{CCA} quiet and isolated		
2.3.3	V_{CCA} pins should be ganged together and a solid PCB plane is recommended. This plane should not have adjacent non-SERDES signals passing above or below. It should also be isolated from the V_{CC} core power plane.		
2.4	If both DCU are not used, V_{CCA} should be connected and remaining SERDES power supplies can be left open.		

	Item	OK	NA
2.5	If only one channel is used, the un-used DCU's V_{CCA} should be connected and remaining SERDES power supplies can be left open.		
2.6	If only one channel is used, the un-used channel within the same DCU's V_{CCA} and V_{CCHTX} should be connected and remaining SERDES power supplies can be left open.		
3	**Configuration**		
3.1	Pull-ups and pull-downs on configuration specific pins		
3.2	V_{CCIO8} bank voltage matches sysCONFIG peripheral devices such as SPI Flash		
4	**SERDES**		
4.1	Dedicated reference clock input from clock source meets the DC and AC requirements		
4.1.1	External AC coupling caps may be required for compatibility to common-mode levels		
4.1.2	Ref clock termination resistors may be needed for compatible signaling levels		
4.2	Maintain good high-speed transmission line routing		
4.2.1	Continuous ground reference plane to serial channels		
4.2.2	Tightly length matched differential traces		
4.2.3	Do not pass other signals on the PCB above or below the high-speed SERDES without isolation.		
4.2.4	Keep non-SERDES signal traces from passing above or below the V_{CCA} power plane without isolation.		
5	**Special Pin Assignments**		
5.2	V_{REF} assignments followed for single-ended SSTL inputs		
5.2.1	Properly decouple the V_{REF} source		
6	**Critical Pinout Selection**		
6.1	Pinout has been chosen to address FPGA resource connections to I/O logic and clock resources per ECP5 and ECP5-5G High-Speed I/O Interface (FPGA-TN-02035).		
6.2	Shared general purpose I/O are used as inputs for FPGA PLL and Clock inputs.		
7	**JTAG**		
7.1	Pull-down on TCK. See Table 3.1.		
7.2	Pull-up on TDI, TMS, TDO. See Table 3.1.		
8	**LPDDR3 and DDR3 Interface Requirements**		
8.1	DQ, DM, and DQS signals should be routed in a data group and should have similar routing and matched via counts. Using more than three vias is not recommended in the route between the FPGA controller and memory device.		
8.2	Maintain a maximum of ±50 mil between any DQ/DM and its associated DQS strobe within a DQ group. Use careful serpentine routing to meet this requirement.		
8.3	All data groups must reference a ground plane within the stack-up.		
8.4	DDR trace reference must be solid without slots or breaks. It should be continuous between the FPGA and the memory.		
8.5	Provide a separation of 3 W spacing between a data group and any other unrelated signals to avoid crosstalk issues. Use a minimum of 2 W spacing between all DDR traces excluding differential CK and DQS signals. (W is the minimum width of the signal trace allowed.)		
8.6	Assigned FPGA I/O within a data group can be swapped to allow clean layout. Do not swap DQS assignments.		
8.7	Differential pair of DQS to DQS_N trace lengths should be matched at ±10 mil.		
8.8	Resistor terminations (DQ) placed in a fly-by fashion at the FPGA is highly recommended. Stub fashion terminations, if used, should not include a stub longer than 600 mil.		
8.9	LDQS/LDQS_N and UDQS/UDQS_N trace lengths should be matched within ±100 mil.		
8.10	Address/control signals and the associated CK and CK_N differential FPGA clock should be routed with a control trace matching ±100 mil.		
8.11	CK to CK_N trace lengths must be matched to within ±10 mil.		
8.12	Address and control signals can be referenced to a power plane if a ground plane is not available. Ground reference is preferred.		

	Item	OK	NA
8.13	Address and control signals should be kept on a different routing layer from DQ, DQS, and DM to isolate crosstalk between the signals.		
8.14	Differential terminations used by the CLK/CLKN pair must be located as close as possible to the memory.		
8.15	Address and control terminations placed after the memory component using a fly-by technique are highly recommended. Stub fashion terminations, if used, should not include a stub longer than 600 mils.		

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.6, October 2020

Section	Change Summary
Acronyms in This Document	Added this section.
Introduction	Added link to LatticeSC SERDES Jitter reference document.
Power Supplies	• Updated ECP5 and ECP5-5G SERDES/PCS Power Supplies section to add V_{CCAUXA} instance. • Added information to elaborate SERDES channels on ECP5 and ECP5-5G device.
Clock Inputs	Update content to correct information on clock inputs and clock routing.
SERDES Pin Considerations	Updated section content.
LFE5U to LFE5UM/LFE5UM5G and LFE5UM to LFE5UM5G Migration	Updated Table 10.1 to add row for V_{CCAUXA} instance in section 2.

Revision 1.5, August 2020

Section	Change Summary
All	Updated the document IDs across the technical note.
Disclaimers	Added this section.
Clock Inputs	Updated section content.
Revision History	Updated format.

Revision 1.4, August 2017

Section	Change Summary
Configuration Considerations	Updated Table 3.2 Pull-up/Pull-down Recommendations for Configuration Pins. Corrected MCLK/CCLK, CFG pull-up/pull-down values. Added CSSPIN pull-up recommendation.
All	Removed copyright page.

Revision 1.3, June 2017

Section	Change Summary
All	• Changed document number from TN1269 to FPGA-TN-02038. • Updated document template. • Changed reference to data sheet from DS1044 to FPGA-DS-02012. • Clarify descriptions on various sections.
Power Supplies	Updated Table 2.1 ECP5 and ECP5-5G FPGA Power Supplies changing CFG[0:2] to CFG[2:0].
Configuration Considerations	Updated Table 3.1 JTAG Pin Recommendations correcting the value in Dedicated CFG[2:0] SSPI Configuration Mode to 001.
Power Supplies	Update the Power Supplies section to correct SERDES power supply requirements.
LFE5U to LFE5UM/LFE5UM5G and LFE5UM to LFE5UM5G Migration	Added more details to the LFE5U to LFE5UM/LFE5UM5G and LFE5UM to LFE5UM5G Migration section.

Revision 1.2, December 2015

Section	Change Summary
Power Supplies	Updated Power Supplies section. Revised Voltage (Nominal Value) for V_{CCA}, V_{CCHRX} and V_{CCHTX} in Table 2.1 ECP5 and ECP5-5G FPGA Power Supplies.
LFE5U to LFE5UM/LFE5UM5G and LFE5UM to LFE5UM5G Migration	• Updated LFE5U to LFE5UM/LFE5UM5G and LFE5UM to LFE5UM5G Migration section. • Removed instances of LFE5U5G. • Revised items 1.2, 2.3.1 and 4.2.4 in Table 10.1 Hardware Checklist.
All	• Changed section title. • Added new paragraph content.

Revision 1.1, November 2015

Section	Change Summary
Power Supplies	Added support for ECP5-5G.
LFE5U to LFE5UM/LFE5UM5G and LFE5UM to LFE5UM5G Migration	• Changed document title to ECP5 and ECP5-5G Hardware Checklist • Changed ECP5U and ECP5UM to LFE5U and LFE5UM.
Configuration Considerations	Updated Configuration Considerations section. Revised PCB recommendation for TDI, TMS and TDO in Table 3.1 JTAG Pin Recommendations.
Technical Support Assistance	Updated Technical Support Assistance section.

Revision 1.0, March 2014

Section	Change Summary
All	Initial release.

www.latticesemi.com