Lattice Avant Hardware Checklist

Preliminary Technical Note

FPGA-TN-02317-0.80

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AC	Alternating Current
BGA	Ball Grid Array
DC	Direct Current
DLL	Delay-Locked Loop
DDR3	Double Data Rate 3
ESR	Equivalent Series Resistance
FPGA	Field-Programmable Gate Array
HCSL	High-Speed Current Steering Logic
HSUL	High-Speed Unterminated Logic
I/O	Input/Output
JTAG	Joint Test Action Group
LVDS	Low-Voltage Differential Signaling
LVSTL	Low-Voltage Swing Terminated Logic
MIPI	Mobile Industry Processor Interface
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
SSTL	Stub Series-Terminated Logic
SerDes	Serializer/Deserializer

1. Introduction

When designing complex hardware using the Lattice Avant™ device, the user must pay special attention to critical hardware configuration requirements. This technical note steps through these critical hardware implementation items relative to the Avant device. The document does not provide detailed step-by-step instructions but gives a high-level summary checklist to assist in the design process.

The device family consists of FPGA densities ranging from 196k to 477k Logic Cells. This technical note assumes that the reader is familiar with the Avant device features as described in the Lattice Avant Platform - Overview Data Sheet (FPGA-DS-02107) and Lattice Avant Platform - Specifications Data Sheet (FPGA-DS-02112). The data sheet includes the functional specification for the device. Topics covered in the data sheet include but are not limited to the following:

- High-level functional overview
- Pinouts and packaging information
- Signal descriptions
- Device-specific information about peripherals and registers
- Electrical specifications

The critical hardware areas covered in this technical note are listed below. Refer to the Lattice Avant Platform - Overview Data Sheet (FPGA-DS-02107) and Lattice Avant Platform – Specifications Data Sheet (FPGA-DS-02112) for details.

- Power supplies as they relate to the Avant power supply rails and how to connect them to the PCB and the associated system
- Configuration mode selection for proper power-up behavior
- Device I/O interface and critical signals

Important: Refer to the following documents for detailed recommendations.

- Lattice Avant sysCONFIG User Guide (FPGA-TN-02299)
- Lattice Avant sysI/O User Guide (FPGA-TN-02297)
- Lattice Avant sysCLOCK PLL Design and User Guide (FPGA-TN-02298)
- Lattice Avant Embedded Memory User Guide (FPGA-TN-02289)
- Lattice Avant High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02300)
- Lattice Avant sysDSP User Guide (FPGA-TN-02293)
- Thermal Management (FPGA-TN-02044)
- Electrical Recommendations for Lattice SerDes (FPGA-TN-02077)
- High-Speed PCB Design Considerations (FPGA-TN-02148)
- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02150)
- LatticeSC™ SerDes Jitter (TN1084)
- HSPICE SerDes simulation package (available under NDA, contact the license administrator at lic_admin@latticesemi.com)
- Lattice Avant-E Pinout (FPGA-SC-02037)

1.1. Power Supplies

Power supplies VCC, VCCAUXA, and VCCIOX for banks 1 and 2 are monitored by an internal Power-On-Reset (POR) circuit to determine the Avant's internal Power Good condition during power-up. These supplies need to be at a valid and stable level before the device becomes operational. All other supplies are not monitored during power-up but need to be at a valid and stable level before the device configuration completes and enters into User Mode.

Table 1.1 describes the power supplies and the appropriate voltage levels for each supply.

Table 1.1. Single-Ended I/O Standards

Supply Rail	Voltage (Nominal Value)[1]	Description
V_{SS}	—	Ground for internal FPGA logic and I/O
V_{CC}	0.82 V	FPGA core power supply. Required for Power Good condition.
V_{CCCLK}	0.82 V	Power supply for clock tree.
V_{CCHP}	0.82 V	Power supply for high-speed logic, mainly in the HPIO sectors.
V_{CCA_PLLx}	0.82 V	Power supply for PLL blocks. x = Specific PLL number.
V_{CCAUXA}	1.8 V	Auxiliary power supply for internal analog circuitry. Required for Power Good condition.
V_{CCAUX}	1.8 V	Auxiliary power supply. Used for generating stable drive current for the I/O.
V_{CCIOx}[2]	Banks 0-14 I/O Voltage	Power supply pins for I/O banks. x = Specific Bank number. Bank 1 and 2 V_{CCIOx} are monitored by POR circuit to provide Power Good condition. Wide-Range Banks: x = 0, 1, 2, 12, 13, and 14 supported V_{CCIOx} voltages: 1.2 V, 1.8 V, 2.5 V, or 3.3 V. High-Performance Banks: x = 3 – 11 supported V_{CCIOx} voltages: 0.9 V, 1.0 V, 1.1 V, 1.2 V, 1.35 V, 1.5 V, or 1.8 V.
V_{CC_BAT}	1.5 V	Optional power supply to allow a battery to preserve the volatile configuration RAM when the other DC supplies are absent.

Note:

1. The Avant FPGA device has a Power-On-Reset (POR) state machine that depends on several power supplies. These supplies should come up monotonically. Initialization of the device does not proceed until all monitored power supplies reach minimum operating voltages.
2. If V_{CCIO} is set to 1.8 V, they must come from the same power supply as V_{CCAUX}.

1.2. Power Source

The power rail voltages of the FPGA allow for a worst-case normal operating tolerance of ±3%. Power supply noise must not cause the voltage rail to exceed the ±3% tolerance.

It is recommended that the designed voltage regulators are accurate to within ±2% of the optimum voltage to allow ±1% for power noise and layout related losses.

When calculating the voltage regulator total tolerance, include:

- Regulator voltage reference tolerance
- Regulator line tolerance
- Regulator load tolerance
- Tolerances of any resistors connected to regulator's feedback pin which sets regulator's output voltage
- Expected voltage drops due to power filtering ferrite bead's ESR * expected current draw
- Expected voltage drops due to current measuring resistor's ESR * expected current draw

Rail voltages less than 1.8 V are especially sensitive to noise (for the 0.82 V rail every 8.2 mV is 1% of the rail voltage). For sensitive analog and PLL rails target less than ±0.25% peak noise.

1.3. Recommended Power Filtering Groups and Components

Table 1.2. Recommended Power Filtering Groups and Components

Power Input	Recommended Filter	Notes
V_{CC}	22 µF x 2 + 10 µF x 3 + 100 nF per pin	Core and clock logic. High current rail, source using switching regulator. 0.82 V
V_{CCCLK}	120 Ω FB (ESR <= 0.1 Ω) + 10 µF x 3 + 100 nF per pin	Power supply for clock tree. Can be sourced by switching regulator. 0.82 V
V_{CCHP}	120 Ω FB (ESR <= 0.01 Ω) + 10 µF x 3 + 100 nF per pin	Sensitive power supply for high-speed logic in the HPIO sectors. Use LDO regulator for low noise. 0.82 V
V_{CCA_PLLx}	600 Ω FB (ESR <= 0.4 Ω) + 1.0 µF + 100 nF	Sensitive power supply for PLL blocks. Low current, use LDO regulator for low noise. Separate FB + Capacitor filter for each V_{CCA_PLLx}. 0.82 V
V_{CCAUXA}	120 Ω FB (ESR <= 0.1 Ω) + 10 µF + 100 nF per pin	Sensitive Auxiliary power supply for internal analog circuitry. 1.8 V
V_{CCAUX}	120 Ω FB (ESR <= 0.1 Ω) + 10 µF x 2 + 100 nF per pin	Auxiliary power supply for internal analog circuitry. 1.8 V
V_{CCIOx}	10 µF + 100 nF per pin	Power supply for I/O banks. x = Specific Bank number. Unused banks can remove the 10 µF. Banks with lots of outputs (~ > 15) or large capacitive loading should replace the 10 µF with a 22 µF (or add a second 10 µF). Wide-Range Banks: x = 0, 1, 2, 12, 13, and 14 supported V_{CCIOx} voltages: 1.2 V, 1.8 V, 2.5 V, or 3.3 V. High-Performance Banks: x = 3 – 11 supported V_{CCIOx} voltages: 0.9 V, 1.0 V, 1.1 V, 1.2 V, 1.35 V, 1.5 V, or 1.8 V.
V_{CC_BAT}	10 µF + 100 nF	Optional power supply to allow a battery to preserve the volatile configuration RAM when the other DC supplies are absent. If not used the rail pin may be left unconnected. 1.5 V

1.4. Unused Banks (V_{CCIOx})

Connect unused V_{CCIOx} pins to a power rail. Do not leave them open.
Recommend bypassing unused rail pin with a 100 nF.

1.5. Ground Pins

All ground pins need to be connected to the board's ground plane.

Ground plane islands can be used to help isolate sensitive grounds from noisy ground areas. The ground plane islands must connect at only one location to the main ground plane. Connection locations should be at least 2 mm wide. Only signals in the same domain as the ground plane island should be referenced to that island.

1.6. Power Sequencing

There is no power up sequence required for the Avant device.
Note: Power supplies V_{CC}, V_{CCAUXA}, and V_{CCIOX} for banks 1 and 2 are monitored by an internal Power-On-Reset (POR) circuit to determine the Avant's internal Power Good condition during power-up.

1.7. Power Estimation

Once the Avant device density, package, and logic implementation are decided, power estimation for the system environment should be determined based on the Power Calculator provided as part of the Lattice Radiant™ design tool. When estimating power, the designer should keep two goals in mind:

- Power supply budgeting should be based on the maximum of the power-up in-rush current, configuration current, and maximum DC and AC current for the given system environmental conditions.
- The ability for the system environment and Avant device packaging to be able to support the specified maximum operating junction temperature.

By determining these two criteria, the Avant device power requirements can be taken into consideration early in the design phase.

2. Component Selection

2.1. Ferrite Bead Selection

- Ferrite bead induced noise voltage drops from ESR * CURRENT should target < 0.5% of rail voltage for non-analog rails and < 0.25% for sensitive rails.
- Small package size ferrite beads have higher ESR than large package size ferrite beads of same impedance.
- High impedance ferrite beads have higher ESR than low impedance ferrite beads in the same package size.

2.2. Capacitor Selection

When specifying components, choose good quality ceramic capacitors in small packages, and place them as close to the power supply pins as practically possible. Good quality capacitors for bypassing generally meet the requirements discussed in the following sections.

2.2.1. Capacitor Dielectric

Use X5R, X7R, and similar dielectrics with good capacitance tolerance (<= ±20%) over temperature range. Avoid Y5V, Z5U, and similarly poor capacitance-controlled dielectrics.

2.2.2. Voltage Rating

Capacitor working capacitance decreases non-linearly with higher voltage bias. To maintain capacitance, the capacitor voltage rating should target at least 80% higher than the voltage rail (maximum). For example: 3.3 V rail bypass capacitors should use the commonly available 6.3 V rating as a minimum.

2.2.3. Size

Smaller body capacitors have lower inductance, work to higher frequencies, and improve board layout. For a given voltage rating, smaller body capacitors tend to cost more than larger body capacitors. Optimizing between market pricing and size related inductance, recommended capacitor sizes are in Table 2.1.

Table 2.1. Recommended Capacitor Sizes

Capacitance	Size Preferred	Size Next Best
0.1 uF	0201	0402
1.0 uF	0402	0603
10 uF	0402	0603
22 uF	0805	0603

3. Clock Inputs

3.1. Clock Oscillator Supply Filtering

When providing an external reference clock to the FPGA from, for example, a single-ended or differential clock oscillator, proper power supply isolation and decoupling of the clock oscillator is recommended. A typical bypassing circuit is shown below in Figure 3.1.

The Avant device provides certain pins for use as clock inputs in each I/O bank. These pins are shared and can alternately be used for General Purpose I/O.

When these pins are used for clocking purpose, you need to pay attention to minimize signal noise on these pins. Refer to Lattice Avant High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02300).

These shared clock input pins can be found under the Dual Function column of the pinlist .csv file.

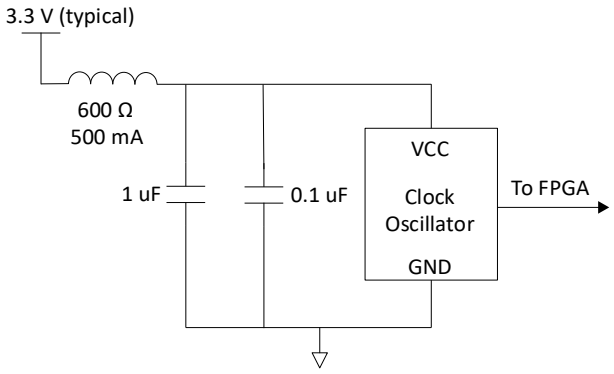

Figure 3.1. Clock Oscillator Bypassing

For differential clock inputs to banks with V_{CCIO} voltage of 1.5 V and lower, it is recommended to use an HCSL oscillator to keep the clock voltage less than or equal to the bank's V_{CCIO}. An LVDS oscillator can also be used if AC coupled and then DC biased at half the V_{CCIO} voltage. An example of dual footprint design supporting HCSL and LVDS shown in Figure 3.2.

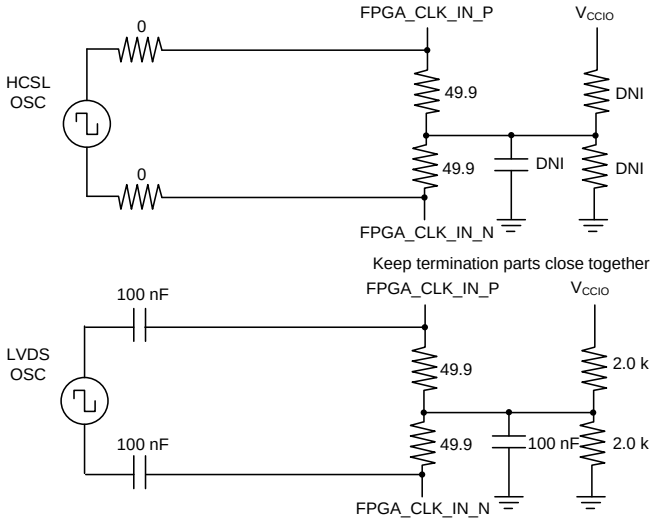

Figure 3.2 PCB Dual Footprint Supporting HCSL and LVDS Oscillators.

4. Configuration Considerations

PCB layout design and breakout suggestions are outlined in PCB Layout Recommendations for BGA Packages (FPGA-TN-02024).

4.1. JTAG

The Avant device includes provisions to configure the FPGA through the JTAG interface or several modes utilizing the sysCONFIG port. The JTAG port includes a 4-pin interface that requires PCB considerations, as shown in Table 4.1.

Table 4.1. JTAG Pin Recommendations

JTAG Pin	PCB Recommendation
CFGMODE	10 kΩ pull-down to GND for JTAG Configuration
TCK	2.2 kΩ pull-down to GND
TMS	10 kΩ pull-up to V_{CCIO2}
TDI	10 kΩ pull-up to V_{CCIO2}
TDO	10 kΩ pull-up to V_{CCIO2}

Every PCB is recommended to have easy access to FPGA JTAG pins, even if the primary configuration interface is not using the JTAG port. This JTAG port enables debugging in the final system. For best results, route the TCK, TMS, TDI, and TDO signals to a common test header along with V_{CCIO2} and ground.

4.2. SPI Configuration

The Avant device includes provisions to configure the FPGA through Master and Slave Serial Peripheral Interface (SPI) ports.

The pins listed in Table 4.2 have internal weak pull resistors, pull-up resistors to the appropriate bank V_{CCIO} and pull-down to board ground. It is recommended to provide external pull resistors as indicated in the table.

Table 4.2. Pull-up/Pull-down Recommendations for Configuration Pins

Pin	PCB Connection
PROGRAMN	4.7 kΩ pull-up to V_{CCIO2}
INITN	10 kΩ pull-up to V_{CCIO2}
DONE	10 kΩ pull-up to V_{CCIO2}
CFGMODE	10 kΩ pull-up to V_{CCIO2} for MSPI Configuration 10 kΩ pull-down to GND for SSPI or JTAG Configuration
MCSN	4.7 kΩ pull-up to V_{CCIO1}
MCLK	1.0 kΩ pull-down to GND (Not installed by default) 1.0 kΩ pull-up to V_{CCIO1} (Not installed by default)
MDQ0/MOSI	10 kΩ pull-up to V_{CCIO1} (Not installed by default)
MDQ1/MISO	10 kΩ pull-up to V_{CCIO1} (Not installed by default)
MDQ2 - MDQ7	10 kΩ pull-up to V_{CCIO1} (Not installed by default)
MDS	MSPI Octal Mode Data Strobe, 10 kΩ pull-down to GND (Not installed by default)
SCSN	4.7 kΩ pull-up to V_{CCIO1}
SCLK	1.0 kΩ pull-down to GND (Not installed by default) 1.0 kΩ pull-up to V_{CCIO2} (Not installed by default)
SDQ0/MOSI	10 kΩ pull-up to V_{CCIO2} (Not installed by default)
SDQ1/MISO	10 kΩ pull-up to V_{CCIO2} (Not installed by default)
SDQ2 - SDQ7	10 kΩ t pull-up o V_{CCIO2} (Not installed by default)
SDS	SSPI Octal Mode Data Strobe, 10 kΩ pull-down to GND (Not installed by default)

4.3. Configuration Pins per Programming Mode

Table 4.3 lists the signal pins required for each configuration-programming mode.

Table 4.3. Configuration Pins Needed per Programming Mode

Configuration Mode	Bank	Enablement	Clock		Bus Size	Pins
			Pin	I/O		
JTAG[1]	2	CFGMODE pin Low	TCLK	Input	1	TCK, TMS, TDI, TDO
MSPI	1	CFGMODE pin High	MCLK	Output	1	MCLK, MCSN, MOSI, MISO
					2	MCLK, MCSN, MD0, MD1
					4	MCLK, MCSN, MD0, MD1, MD2, MD3
					8	MCLK, MCSN, MDS, MD0, MD1, MD2, MD3, MD4, MD5, MD6, MD7
SSPI	1	CFGMODE pin Low	SCLK	Input	1	SCLK, SCSN, SI, SO
					2	SCLK, SCSN, SD0, SD1
					4	SCLK, SCSN, SD0, SD1, SD2, SD3
					8	SCLK, SCSN, SDS, SD0, SD1, SD2, SD3, SD4, SD5, SD6, SD7

Note:

1. JTAG port takes precedence over SSPI.

5. I/O Pin Assignments

Crosstalk coupling is reduced in the Avant device packages. The PCB board, however, can cause significant noise injection from adjacent I/O pins and PCB traces running close together in parallel for long distances. Simulate any suspicious traces using a PCB crosstalk/Signal Integrity simulation tool to determine if a particular layout needs to be improved.

It is common practice for designers to select pinouts for their system early in the design cycle. For the FPGA designer, this requires a detailed knowledge of the targeted FPGA device. Designers often use a spreadsheet program to initially capture the list of the design I/O. Lattice Semiconductor provides detailed pinout information that can be downloaded from the Lattice Semiconductor website in .csv format for designers to use as a resource to create pinout information. For example, by navigating to the pinout.csv file, you can gather the details for all the different package offerings of the device in the family, including I/O banking, differential pairing, Dual Function of the pins, and input and output details.

5.1. Series Termination Resistors

When using series termination resistors, start with a value of 0 Ω due to GPIOs having a relatively high output impedance.

5.2. Functional Blocks Rule-Based Pinout Considerations

The Avant family of devices supports many applications with high-speed interfaces. These include various rule-based pinouts that need to be understood prior to implementation of the PCB design on these high-speed interfaces. The pinout selection must be completed with an understanding of the interface building blocks implemented in the FPGA fabric. These include IOLOGIC blocks such as Soft MIPI, clock resource connectivity, and PLL usage. Refer to Lattice Avant High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02300) for rules pertaining to these interface types.

5.3. LVDS and MIPI Assignments

True LVDS and MIPI signaling inputs and outputs are available on I/O pins on the bottom side of the devices. Top side I/O banks do not support true LVDS and MIPI standard but can support emulated LVDS outputs. True LVDS and MIPI input pairing on bottom banks can be found under the High-Speed column in the pin-list .csv file.

Emulated LVDS output are available on pairs of all banks, but this requires external termination resistors. This is described in Lattice Avant sysI/O User Guide (FPGA-TN-02297).

Bank voltage must be set to 1.8 V to support LVDS.

Bank voltage must be set to 1.2 V to support MIPI.

5.4. HSUL and SSTL Pin Assignments

The HSUL and SSTL interfaces are referenced I/O standards that require an external reference voltage. HSUL and SSTL are supported on the device bottom banks only. The V_{REF} pin(s) should get high priority when assigning pins on the PCB. These pins can be found in the Dual Function column with V_{REF} label. Each bank includes a separate V_{REF} voltage. V_{REF} sets the threshold for the referenced input buffers. Each I/O is individually configurable based on the bank supply and reference voltages.

6. Pinout Considerations

The Avant device supports many applications with high-speed interfaces. These include various rule-based pinouts that need to be understood prior to implementation of the PCB design on these high-speed interfaces. The pinout selection must be completed with an understanding of the interface building blocks implemented in the FPGA fabric. These include IOLOGIC blocks such as DDR, clock resource connectivity, and PLL and DLL usage. Refer to Lattice Avant High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02300) for rules pertaining to these interface types.

6.1. LVDS Pin Assignments

True LVDS inputs and outputs are available on I/O pins on the device bottom banks 3 to 11 only. Top I/O banks do not support True LVDS standard, but can support emulated LVDS outputs. True LVDS input pairing on bottom banks can be found under the High-Speed column in the pinlist csv file.

Emulated LVDS output are available on pairs around all banks, but this requires external termination resistors. This is described in Lattice Avant sysI/O User Guide (FPGA-TN-02297).

6.2. HSUL, SSTL and LVSTL Pin Assignments

The HSUL, SSTL and LVSTL interfaces are referenced I/O standards require an external reference voltage. HSUL, SSTL and LVSTL are supported on the device bottom banks 3 TO 11 only. The V_{REF} pin(s) should get high priority when assigning pins on the PCB. These pins can be found in the Dual Function column with V_{REF} label. Each bank includes a separate V_{REF} voltage. V_{REF} sets the threshold for the referenced input buffers. Each I/O is individually configurable based on the bank supply and reference voltages.

7. Checklist

Table 7.1. Hardware Checklist

	Item	OK	NA
1	**FPGA Power Supplies**		
1.1	System Supplies		
1.1.1	V_{CC}, V_{CCCLK}, V_{CCHP}, V_{CCA_PLLx} @ 0.82 V ±3%		
1.1.2	Use a PCB plane for V_{CC} core with proper decoupling		
1.1.3	V_{CC} core sized to meet power requirement calculation from software		
1.1.4	V_{CCA_PLLx} Must be *quiet* and isolated from other switching noises.		
1.1.5	V_{CCAUX} and V_{CCAUXA} @ 1.8 V ±3%		
1.1.6	V_{CCAUX} and V_{CCAUXA} Must be *quiet* and isolated from other switching noises.		
1.1.7	V_{CCAUX} pins should be ganged together and a solid PCB plane is recommended.		
1.1.8	V_{CCAUXA} pins filtered separately from V_{CCAUX} pins.		
1.1.9	V_{CC_BAT} pin @ 1.5 V +3%/-33% if used, if not used leave pin open.		
1.2	I/O Supplies		
1.2.1	All *Wide Range* V_{CCIO} (Banks 0, 1, 2, 12, 13, and 14) V_{CCIOx} voltages: 1.2 V, 1.8 V, 2.5 V, or 3.3 V.		
1.2.2	All *High Performance* (Banks 3 – 11) V_{CCIOx} between 0.9 V, 1.0 V, 1.1 V, 1.2 V, 1.35 V, 1.5 V, or 1.8 V.		
2	**JTAG**		
2.1	CFGMODE pin pulled Low per Table 4.1.		
2.2	Keep JTAG_EN accessible on PCB to recover JTAG port, especially during development.		
2.3	Keep JTAG port pins accessible on PCB, especially during development.		
2.4	Pull-down on TCK per Table 4.1.		
2.5	Pull-up on TMS, TDI, and TDO per Table 4.1.		
3	**MSPI and SSPI Configuration**		
3.1	V_{CCIO1}, V_{CCIO2} bank voltage matches sysCONFIG peripheral devices (SPI Flash, External connections).		
3.2	10 kΩ pull-up to V_{CCIO2} for MSPI Configuration 10 kΩ pull-down to GND for SSPI Configuration		
3.3	Pull-ups or pull-downs on persisted configuration specific pins per Table 4.1 and Table 4.2		
4	**Special Pin Assignments**		
4.1	VREF assignments followed for single-ended SSTL inputs		
4.2	Properly decouple the VREF source		

	Item	OK	NA
5	**Critical Pinout Selection**		
5.1	Pinout is chosen to address FPGA resource connections to I/O logic and clock resources per Lattice Avant High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02300).		
5.2	Shared general purpose I/O are used as inputs for FPGA PLL and Clock inputs.		
5.3	The Differential clock input positive side must use a PCLKTx_y and negative side must use PCLKCx_y pins for the clock to be properly routed directly to the edge clock tree.		
6	**LPDDR3 and DDR3 Interface Requirements**		
6.1	DQ, DM, and DQS signals should be routed in a data group and should have similar routing and matched via counts. Using more than three vias is not recommended in the route between the FPGA controller and memory device.		
6.2	Maintain trace length matching to a maximum of ±20 mil between any DQ/DM and its associated DQS strobe within a DQ group. Use careful serpentine routing to meet this requirement.		
6.3	All data groups must reference a ground plane within the stack-up.		
6.4	DDR trace reference must be solid without slots or breaks. It should be continuous between the FPGA and the memory.		
6.5	Provide a separation of 3 W spacing between a data group and any other unrelated signals to avoid crosstalk issues. Use a minimum of 2 W spacing between all DDR traces excluding differential CK and DQS signals. (W is the minimum width of the signal trace allowed)		
6.6	Assigned FPGA I/O within a data group can be swapped to allow clean layout. Do not swap DQS assignments.		
6.7	Differential pair of DQS to DQS_N trace lengths should be matched to ±10 mil.		
6.8	Resistor terminations (DQ) placed in a fly-by fashion at the FPGA is highly recommended. Stub fashion terminations, if used, should not include a stub longer than 600 mil.		
6.9	LDQS/LDQS_N and UDQS/UDQS_N trace lengths should be matched within ±100 mil.		
6.10	Address/control signals and the associated CK and CK_N differential FPGA clock should be routed with a control trace matching ±100 mil.		
6.11	CK to CK_N trace lengths must be matched to within ±10 mil.		
6.12	Address and control signals can be referenced to a power plane if a ground plane is not available. Ground reference is preferred.		
6.13	Address and control signals should be kept on a different routing layer from DQ, DQS, and DM to isolate crosstalk between the signals.		
6.14	Differential terminations used by the CLK/CLKN pair must be located as close as possible to the memory.		
6.15	Address and control terminations placed after the memory component using a fly-by technique are highly recommended. Stub fashion terminations, if used, should not include a stub longer than 600 mils.		

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, please refer to the Lattice Answer Database at https://www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 0.80, December 2022

Section	Change Summary
All	Preliminary release.

www.latticesemi.com