CrossLink-NX-33 Hardware Checklist

Technical Note

FPGA-TN-02308-1.0

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
BGA	Ball Grid Array
FPGA	Field-Programmable Gate Array
HCSL	High Speed Current Steering Logic
LVDS	Low-Voltage Differential Signaling
MIPI	Mobile Industry Processor Interface
PCB	Printed Circuit Board

1. Introduction

When designing complex hardware using the CrossLink™-NX-33 device, you must pay special attention to critical hardware configuration requirements. This technical note steps through these critical hardware implementation items relative to the CrossLink-NX-33 device. The document does not provide detailed step-by-step instructions but gives a high-level summary checklist to assist in the design process.

The CrossLink-NX-33 device includes up to 33k Logic Cells. This technical note assumes that the reader is familiar with the CrossLink-NX-33 device features as described in CrossLink-NX-33 Data Sheet (FPGA-DS-02104). The data sheet includes the functional specification for the device. Topics covered in the data sheet include but are not limited to the following:

- High-level functional overview
- Pinouts and packaging information
- Signal descriptions
- Device-specific information about peripherals and registers
- Electrical specifications

Refer to CrossLink-NX-33 Data Sheet (FPGA-DS-02104) for details. The critical hardware areas covered in this technical note are:

- Power supplies as they relate to the CrossLink-NX-33 power supply rails and how to connect them to the PCB and the associated system
- Configuration mode selection for proper power-up behavior
- Device I/O interface and critical signals

Important: You should refer to the following documents for detailed recommendations.

- sysCONFIG Usage Guide for Nexus Platform (FPGA-TN-02099)
- sysI/O Usage Guide for Nexus Platform (FPGA-TN-02067)
- sysCLOCK PLL Design and Usage Guide for Nexus Platform (FPGA-TN-02095)
- Memory Usage Guide for Nexus Platform (FPGA-TN-02094)
- CrossLink-NX 33 High-Speed I/O Interface (FPGA-TN-02280)
- Thermal Management (FPGA-TN-02044)
- sysDSP Block Usage Guide for Nexus Platform (FPGA-TN-02096)
- Electrical Recommendations for Lattice SERDES (FPGA-TN-02077)
- High-Speed PCB Design Considerations (FPGA-TN-02148)
- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02150)
- CrossLink-NX LIFCL-33 Pinout (FPGA-SC-02042)

2. Power Supplies

The V_{CC}, V_{CCAUXA}, and V_{CCIOx} power supplies are monitored to determine the CrossLink-NX-33 internal Power Good condition during power-up. These supplies need to be at a valid and stable level before the device becomes operational. All other supplies are not monitored during power-up, but need to be at valid and stable level before the device configuration is complete and enters into User Mode.

Table 2.1 describes the power supplies and the appropriate voltage levels for each supply.

Table 2.1. Single-Ended I/O Standards

Supply	Voltage (Nominal Value)	Description
V_{CC}, V_{CCECLK}	1.0 V	FPGA core power supply. Required for Power Good condition.
V_{CCAUXA}	1.8 V	Auxiliary Supply Voltage for Core logic.
V_{CCAUX}	1.8 V	Auxiliary power supply voltage for internal analog circuitry Banks 0, 1, and 5. Required for Power Good condition
$V_{CCAUXH[4:2]}$	1.8 V	Auxiliary power supply voltage for internal analog circuitry Banks 2, 3, and 4.
$V_{CCIO[5:0]}$	Banks 0, 1, 5: 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V. Banks 2, 3, 4: 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V.	Bank I/O Driver Supply Voltage. Each bank has its own V_{CCIO} supply: V_{CCIO0} and V_{CCIO1} are used in conjunction with pins dedicated and shared with device configuration, and are required for Power Good condition.

The CrossLink-NX-33 FPGA device has a power-on-reset state machine that depends on V_{CC}, V_{CCAUX}, $V_{CCIO[1:0]}$ power supplies. These supplies should come up monotonically. Initialization of the device does not proceed until all monitored power supplies have reached their minimum operating voltages.

2.1. Power Noise

The power rail voltages of the FPGA allow for a worst-case normal operating tolerance of ±5% of these voltages. The 5% tolerance includes any noises.

2.2. Power Source

The recommendation is to design voltage regulators to be accurate to within 3% of the optimum voltage to allow power noise design margin.

When calculating the voltage regulator total tolerance, include:

- Regulator voltage reference tolerance
- Regulator line tolerance
- Regulator load tolerance
- Tolerances of any resistors connected to regulator's feedback pin which sets regulator's output voltage
- Expected voltage drops due to power filtering ferrite bead's ESR * expected current draw
- Expected voltage drops due to current measuring resistor's ESR * expected current draw

With 3% tolerance allocated to the voltage source, the design has a remaining 2% tolerance for noise and layout related issues. The 1.0 V rail is especially sensitive to noise as every 10 mV is 1% of the rail voltage. For PLLs, target less than 0.25% peak noise.

Supplies should be decoupled with adequate power filters. Bypass capacitors must be located close to the device package pins.

For the best jitter performance, especially with MIPI functionality, optimize pin assignment to keep noisy I/O pins away from sensitive functional pins. The leading causes of PCB related crosstalk to sensitive blocks is related to FPGA outputs located in close proximity to the sensitive power supplies. These supplies require cautious board layout to ensure noise immunity to the switching noise generated by FPGA outputs.

2.3. Recommended Power Filtering Groups and Components

Table 2.2. Recommended Power Filtering Groups and Components

Power Input	Recommended Filter	Notes
V_{CC}, V_{CCECLK}	10 µF x 3 + 100 nF per pin	Core logic. 1.0 V
V_{CCAUXA}	120 Ω FB + 10 µF + 100 nF per pin	Auxiliary power supply pin for Core logic. 1.8 V
V_{CCAUX} and $V_{CCAUXH[4:2]}$ Combined Together	120 Ω FB + 10 µF x 2 + 100 nF per pin	Auxiliary power supply pin for internal analog circuitry V_{CCAUX} Banks 0, 1, 5. $V_{CCAUXH[4:2]}$ Banks 2, 3, 4. 1.8 V
$V_{CCIO[5:0]}$	10 µF + 100 nF per pin	Bank I/O. Unused banks can use a single 100 nF. For banks with lots of outputs or large capacitive loading add one additional 10 µF (or can use a single 22 µF instead of two 10 µF.) Banks 0, 1, 5 = 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V. Banks 2, 3, 4 = 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V.

2.4. Unused Bank(s) V_{CCIOx}

Connect unused V_{CCIO}s to a power rail, do not leave them open.

Unused banks can use a single 100 nF bypass capacitor.

2.5. Ground Pins

All ground pins need to be connected to the board's ground plane.

2.6. Power Sequencing

There is no power-up sequence required for the CrossLink-NX-33 device.

2.7. Power Estimation

Once the CrossLink-NX-33 device density, package, and logic implementation is decided, power estimation for the system environment should be determined based on the Power Calculator provided as part of the Lattice Radiant® design tool. When estimating power, the designer should keep two goals in mind:

- Power supply budgeting should be based on the maximum of the power-up in-rush current, configuration current, and maximum DC and AC current for the given system environmental conditions.
- Thermal considerations are also important. The thermal design of the system environment and CrossLink-NX-33 device should be able to support operating at maximum operating junction temperature.

The above two criteria should be taken into consideration early in the design phase.

3. Component Selection

3.1. Ferrite Bead Selection

- Most designs work well using ferrite beads between 120 Ω @100 MHz and 240 Ω @100 MHz.
- Ferrite bead induced noise voltage from ESR * CURRENT should be < 1% of rail voltage for non-analog rails and < 0.25% for sensitive rails.
- Non-PLL rails should use ferrite beads with ESR between 0.025 Ω and 0.10 Ω depending on current load.
- PLL rails draw low current which allows ferrite beads with ESR <= 0.3 Ω.
- Small package size ferrite beads have higher ESR than large package size ferrite beads of same impedance.
- High impedance ferrite beads have higher ESR than low impedance ferrite beads in the same package size.

3.2. Capacitor Selection

When specifying components, choose good quality ceramic capacitors in small packages and place them close to the power oscillator supply pins with short low inductance connections. Good quality capacitors for bypassing generally meet the requirements discussed in the following sections.

3.2.1. Capacitor Dielectric

Use X5R, X7R, and similar dielectrics with good capacitance tolerance (<= ±20%) over temperature range. Avoid Y5V, Z5U, and similarly poor capacitance-controlled dielectrics.

3.2.2. Voltage Rating

Capacitor working capacitance decreases non-linearly with higher voltage bias. To maintain capacitance, the capacitor voltage rating should target at least 80% higher than the voltage rail (maximum). For example: 3.3 V rail bypass capacitors should use the commonly available 6.3 V rating as a minimum.

3.2.3. Size

Smaller body capacitors have lower inductance, work to higher frequencies, and improve board layout. For a given voltage rating, smaller body capacitors tend to cost more than larger body capacitors. Optimizing between market pricing and size related inductance, recommended capacitor sizes are in Table 3.1.

Table 3.1. Recommended Capacitor Sizes

Capacitance	Size Preferred	Size Next Best
0.1 µF	0201	0402
1.0 µF, 2.2 µF	0402	0201
4.7 µF	0402	0603
10 µF	0402	0603
22 µF	0805	0603

4. Clock Inputs

The CrossLink-NX-33 device provides certain pins for use as clock inputs in each I/O bank. These pins are shared and can alternately be used for General Purpose I/O.

When these pins are used for clocking purpose, the user needs to pay attention to minimize signal noise on these pins. Refer to CrossLink-NX-33 High-Speed I/O Interface (FPGA-TN-02280).

These shared clock input pins can be found under the Dual Function column of the pin-list .csv file.

High speed differential interfaces (such as MIPI) being received by the FPGA must route their differential clock pair into a pair of inputs that support differential clocking, labeled PCLKTx_y (+true) and PCLKCx_y (-complement).

When providing an external reference clock to the FPGA, ensure that the oscillator's output voltage to the FPGA does not exceed the bank's voltage. Good power supply decoupling of the clock oscillator is required to reduce clock jitter. A typical bypassing circuit is shown in Figure 4.1.

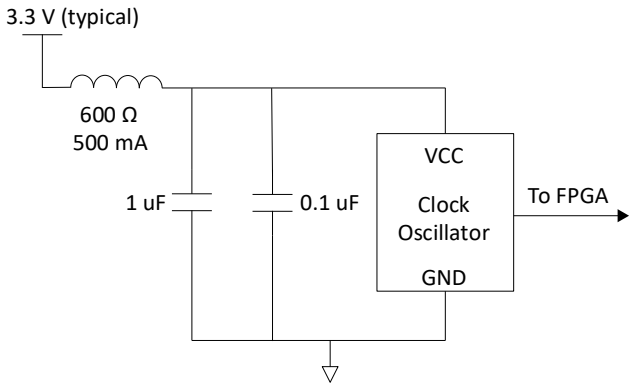

Figure 4.1. Clock Oscillator Bypassing

For differential clock inputs to banks with V_{CCIO} voltage of 1.5 V and lower it is recommended to use an HCSL oscillator to keep the clock voltage less than or equal to the bank's VCCIO. An LVDS oscillator can also be used if AC coupled and then DC biased at half the V_{CCIO} voltage. Example dual footprint design supporting HCSL and LVDS shown below in Figure 4.2.

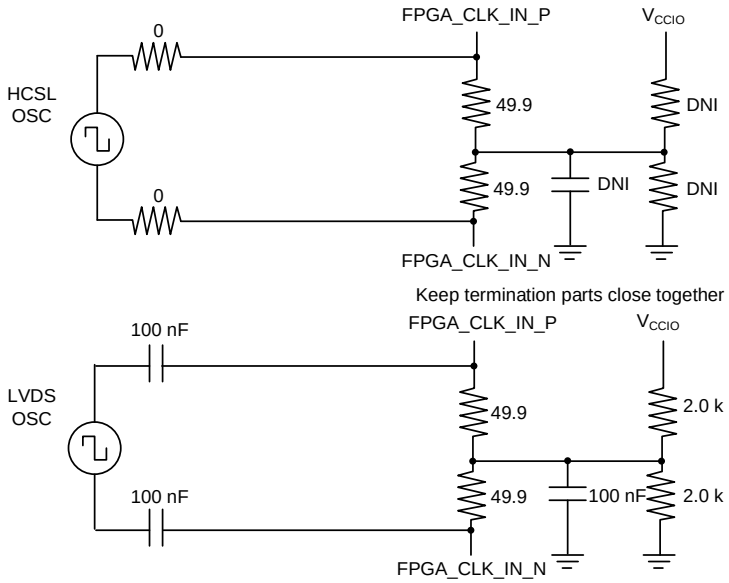

Figure 4.2. PCB Dual Footprint Supporting HCSL and LVDS Oscillators

5. Configuration Considerations

PCB layout design and breakout suggestions are outlined in PCB Layout Recommendations for BGA Packages (FPGA-TN-02024).

The CrossLink-NX-33 device includes provisions to configure the FPGA through the JTAG interface or several modes utilizing the sysCONFIG port.

5.1. JTAG

The JTAG port includes a JTAG Enable pin and a 4-pin interface, as shown in Table 5.1.

Table 5.1. JTAG Pin Recommendations

JTAG Pin	PCB Recommendation
JTAG_EN	4.7 kΩ pull-down to GND (JTAG port disabled) or 1.0 kΩ pull-up to V_{CCIO1} (JTAG port enabled)
TDI/SI	10 kΩ pull-up to V_{CCIO1}
TMS/SCSN	10 kΩ pull-up to V_{CCIO1}
TDO/SO	10 kΩ pull-up to V_{CCIO1}
TCK/SCLK	2.2 kΩ pull-down to GND

Every PCB is recommended to have easy access to FPGA JTAG pins, even if the primary configuration interface is not using the JTAG port. This JTAG port enables debugging in the final system. For best results, route the TCK, TMS, TDI, and TDO signals to a common test header along with V_{CCIO1} and ground.

5.2. Slave SPI and I2C Configuration

While the pins listed in Table 5.2 have internal weak pull resistors, pull-up resistors to the appropriate bank V_{CCIO} and pull-down to board ground for these pins should be used as indicated under PCB Connection.

Table 5.2. Pull-up/Pull-down Recommendations for Configuration Pins

Pin	PCB Connection
PROGRAMN	4.7 kΩ pull-up to V_{CCIO0}
INITN	10 kΩ pull-up to V_{CCIO0}
DONE	10 kΩ pull-up to V_{CCIO0}
JTAG_EN	4.7 kΩ pull-down to GND (JTAG port disabled) or 1.0 kΩ pull-up to V_{CCIO1} (JTAG port enabled)
MCLK	1.0 kΩ to GND (Not installed by default) 1.0 kΩ to Vccio1 (Not installed by default)
MCSN	10 kΩ pull-up to V_{CCIO0}
TMS/SCSN	10 kΩ pull-up to V_{CCIO1}
SCL/SDA	1.0 kΩ to 4.7 kΩ pull-up to V_{CCIO1}

5.3. Configuration Pins Per Programming Mode

Table 5.3 lists the signal pins required for each configuration-programming mode.

Table 5.3. Configuration Pins Needed per Programming Mode

Configuration Mode	Bank	Enablement	Clock		Bus Size	Pins
			Pin	I/O		
MSPI	0	(Default)	MCLK	Output	1	MCLK, MCSN, MOSI, MISO
					2	MCLK, MCSN, MD0, MD1
					4	MCLK, MCSN, MD0, MD1, MD2, MD3
JTAG	1	JTAG_EN pin[1]	TCLK	Input	1	TCK, TMS, TDI, TDO
SSPI	1	Activation key[1]	SCLK	Input	1	SCLK, SCSN, SI, SO
					2	SCLK, SCSN, SD0, SD1
					4	SCLK, SCSN, SD0, SD1, SD2, SD3
I^2C/I3C	1	Activation key	SCL	Input	1	SCL, SDA

Note:

1. JTAG and SSPI ports share pins. When JTAG_EN is asserted, the JTAG port takes precedence over SSPI.

6. I/O Pin Assignments

Crosstalk coupling is reduced in the device packages of CrossLink-NX-33 devices. The PCB board, however, can cause significant noise injection from adjacent I/O pins and PCB traces running close together in parallel for long distances. Simulate any suspicious traces using a PCB crosstalk/Signal Integrity simulation tool to determine if a particular layout needs to be improved.

It is common practice for designers to select pinouts for their system very early in the design cycle. For the FPGA designer, this requires a detailed knowledge of the targeted FPGA device. Designers often use a spreadsheet program to initially capture the list of the design I/O. Lattice Semiconductor provides detailed pinout information that can be downloaded from the Lattice Semiconductor website in .csv format for designers to use as a resource to create pinout information. For example, by navigating to the pinout.csv file, you can gather the pinout details for all the different package offerings of the device in the family, including I/O banking, differential pairing, Dual Function of the pins, and input and output details.

6.1. Series Termination Resistors

When using series termination resistors, start with a value of 0-Ω due to GPIOs having a relatively high output impedance.

6.2. Functional Blocks Rule-Based Pinout Considerations

The CrossLink-NX-33 device supports many applications with high-speed interfaces. These include various rule-based pinouts that need to be understood prior to implementation of the PCB design on these high-speed interfaces. The pinout selection must be completed with an understanding of the interface building blocks implemented in the FPGA fabric. These include IOLOGIC blocks such as MIPI, clock resource connectivity, and PLL and DLL usage. Refer to CrossLink-NX-33 High-Speed I/O Interface (FPGA-TN-02280) for rules pertaining to these interface types.

6.3. LVDS and MIPI Pin Assignments

True LVDS and MIPI signaling inputs and outputs are available on I/O pins on the bottom side of the devices. Top side I/O banks do not support true LVDS and MIPI standard, but can support emulated LVDS outputs. True LVDS and MIPI input pairing on bottom banks can be found under the High-Speed column in the pin-list .csv file.

Emulated LVDS output are available on pairs of all banks, but this requires external termination resistors. This is described in sysI/O Usage Guide for Nexus Platform (FPGA-TN-02067).

Bank voltage must be set to 1.8 V to support LVDS.

Bank voltage must be set to 1.2 V to support MIPI.

6.4. HSUL and SSTL Pin Assignments

The HSUL and SSTL interfaces are referenced I/O standards that require an external reference voltage. HSUL and SSTL are supported on the device bottom banks only. The V_{REF} pin(s) should get high priority when assigning pins on the PCB. These pins can be found in the Dual Function column with V_{REF} label. Each bank includes a separate V_{REF} voltage. V_{REF} sets the threshold for the referenced input buffers. Each I/O is individually configurable based on the bank supply and reference voltages.

7. Checklist

Table 7.1. Hardware Checklist

	Item	OK	NA
1	**FPGA Power Supplies**		
1.1	Core Supplies		
1.1.1	V_{CC}, V_{CCECLK} @ 1.0 V ±5%		
1.1.2	Use a PCB plane for V_{CC}, V_{CCECLK} with proper decoupling		
1.1.3	V_{CC} core sized to meet power requirement calculation from software		
1.1.4	V_{CCAUX}, V_{CCAUXA} and $V_{CCAUXH2/H3/H4}$ @ 1.8 V –3%/+5%		
1.1.5	Follow recommended power filtering groups and components in Table 2.2.		
1.1.6	V_{CCAUXA} and $V_{CCAUXH2/H3/H4}$ pins should be ganged together and a solid PCB plane is recommended. This plane should not couple into the V_{CC} core power plane.		
1.1.7	All ground pins need to be connected to the board's ground plane.		
1.2	I/O Supplies		
1.2.1	All *Wide Range* V_{CCIO} (Banks 0,1,5) are between 1.2 V to 3.3 V.		
1.2.2	All *High Performance* V_{CCIO} (Bank 2,3,4) are between 1.0 V to 1.8 V.		
1.2.3	Connect unused V_{CCIO}s to a power rail, do not leave them open. Unused banks can use a single 100 nF bypass capacitor.		
1.2.4	All Configuration V_{CCIO} (Banks 0,1), when used with configuration interfaces (for example, SPI Flash memory devices), need to match voltage specifications.		
1.2.5	$V_{CCIO[5:0]}$ used based on user design		
2	**JTAG**		
2.1	Pull-up on JTAG_EN to enable JTAG function, per Table 5.2.		
2.2	Keep JTAG_EN accessible on PCB to recover JTAG port, especially during development.		
2.3	Keep JTAG port pins accessible on PCB, especially during development.		
2.4	Pull-down on TCK per Table 5.1.		
2.5	Pull-up on TMS per Table 5.1.		
3	**Configuration**		
3.1	Pull-down on JTAG_EN to disable JTAG and enable shared pins used for configuration, per Table 5.2.		
3.2	Pull-ups or pull-downs on persisted configuration specific pins per Table 5.1 and Table 5.2.		
3.3	V_{CCIO0}, V_{CCIO1} bank voltage matches sysCONFIG peripheral devices such as SPI Flash.		
4	**Special Pin Assignments**		
4.1	V_{REF} assignments followed for single-ended SSTL inputs.		
4.2	Properly decouple the V_{REF} source.		
5	**Critical Pinout Selection**		
5.1	Pinout is chosen to address FPGA resource connections to I/O logic and clock resources per CrossLink-NX-33 High-Speed I/O Interface (FPGA-TN-02280).		
5.2	Shared general purpose I/O are used as inputs for FPGA PLL and Clock inputs.		
6	**Series Termination Resistors**		
6.1	When using series termination resistors start with a value of 0 Ω due to GPIOs having a relatively high output impedance.		

	Item	OK	NA
7	**MIPI Interface Requirements**		
7.1	Soft MIPI supported on bottom banks 2, 3, and 4.		
7.2	V_{CCIO} set to 1.2 V.		
7.3	MIPI differential pairs must reference a ground plane without slots or breaks. It should be continuous between the FPGA and destination/source		
7.4	Provide a separation of 3 W between positive and negative of a pair (diff-pair spacing). (W is the minimum width of the signal trace allowed.)		
7.5	Provide a separation of 6 W spacing around each differential pair (inter-pair spacing). (W is the minimum width of the signal trace allowed.)		
7.6	Length match clock and data lane pair traces within 0.1 mm.		
7.7	MIPI RX at FPGA should have clock differential pair routed to clock pins labeled PCLKTx_y (+true) and PCLKCx_y (-complement).		
8	**LVDS Interface Requirements**		
8.1	True LVDS supported on bottom banks 2, 3, and 4.		
8.2	V_{CCIO} set to 1.8 V.		
8.3	LVDS differential pairs must reference a ground plane without slots or breaks. It should be continuous between the FPGA and destination/source		
8.4	Provide a separation of 3 W between positive and negative of a pair (diff-pair spacing). (W is the minimum width of the signal trace allowed.)		
8.5	Provide a separation of 6 W spacing around each differential pair (inter-pair spacing). (W is the minimum width of the signal trace allowed.)		
8.6	Length match pair traces within 0.1 mm.		
8.7	LVDS RX at FPGA should have clock differential pair routed to clock pins labeled PCLKTx_y (+true) and PCLKCx_y (-complement).		

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, October 2022

Section	Change Summary
All	Initial release.

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