CrossLinkPlus sysI/O Usage Guide

Technical Note

FPGA-TN-02108-1.0

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
DRC	Design Rule Check
DDR	Double Data Rate
GPIO	General Purpose Input/Output
GUI	Graphical User Interface
HDL	Hardware Description Language
I^2C	Inter-Integrated Circuit
LSE	Lattice Synthesis Engine
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
LVTTL	Low Voltage Transistor-Transistor Logic
PIO	Programmable Input/Output
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit

1. Introduction

The Lattice Semiconductor CrossLinkPlus™ device family features programmable sysI/O™ buffers that support a wide range of interfaces. The sysI/O buffers enables you to easily interface with other devices using advanced system I/O standards.

This technical note describes available sysI/O standards and how they can be implemented using Lattice Diamond® design software.

2. sysI/O Buffer Overview

The key features of the sysI/O block are:

- Support for both differential and single-ended standards.
- Programmable weak pull-up on all banks.
- Support for on-chip programmable pull-up resistor for I^2C. 3.3 kΩ, 6.8 kΩ, and 10 kΩ in Bank 0.
- Support for on-chip dynamic differential input terminations on Bank 1 and Bank 2.
- Input Hysteresis on all LVCMOS33/LVTTL33, LVCMOS25, and LVCMOS18.
- Programmable Open Drain on all outputs.
- ckfBGA80 Package - Bank 1 and Bank 2 are in groups of 14 and 16 I/O respectively or 7 and 8 LVDS I/O pairs respectively that support True-LVDS output driver, differential input comparator, and differential termination resistor per I/O pair. Both single-ended and differential LVDS drivers can be tri-stated.
- ucfBGA64 Package - Bank 1 and Bank 2 are in groups of 10 and 12 I/O respectively or 5 and 6 LVDS I/O pairs respectively that support True-LVDS output driver, differential input comparator, and differential termination resistor per I/O pair. Both single-ended and differential LVDS drivers can be tri-stated.

3. Supported sysI/O Standards

The CrossLinkPlus sysI/O buffers support both single-ended and differential standards on Bank 1 and Bank 2. Bank 0 supports all the configuration pins and general purpose single-ended I/O. Table 3.1 lists the sysI/O standards supported in CrossLinkPlus devices.

Table 3.1. Single-Ended I/O Standards

Standard	V_{CCIO}	Input	Output	Bi-directional
LVTTL33	3.3	Yes	Yes	Yes
LVCMOS33	3.3	Yes	Yes	Yes
LVCMOS25	2.5	Yes	Yes	Yes
LVCMOS18	1.8	Yes	Yes	Yes
LVCMOS12	1.2	No	Yes*	No

***Note**: For Bank 1 and Bank 2 only.

Table 3.2. Differential I/O Standards

Standard	Input	Output	Bi-directional
LVDS	Yes	Yes	No
subLVDS	Yes	No	No
MIPI (D-PHY)	Yes (HS-RX, LP-RX)	No*	Yes (LP)
SLVS	Yes	No*	No
LVCMOS25D	Yes	Yes	Yes
LVCMOS33D	No	Yes	No
LVTTL33D	No	Yes	No

***Note**: These output standards are supported by the hard MIPI D-PHY blocks on CrossLinkPlus, but not the programmable I/O.

4. sysI/O Banking Scheme

CrossLinkPlus devices have three banks at the bottom and two MIPI® D-PHY banks at the top of the device as shown in Figure 4.1.

CrossLinkPlus supports single-ended buffers on all banks (0, 1, and 2.) Differential I/O are supported on Bank 1 and Bank 2. ctfBGA80 has 7 differential I/O pairs on Bank 1 and 8 differential I/O pairs on Bank 2, for a total of 15 pairs of differential I/O which are all True-LVDS. ucfBGA64 has 5 differential I/O pairs on Bank 1 and 6 differential I/O pairs on Bank 2, for a total of 11 pairs of differential I/O, which are all True-LVDS. All the configuration ports are located at Bank 0.

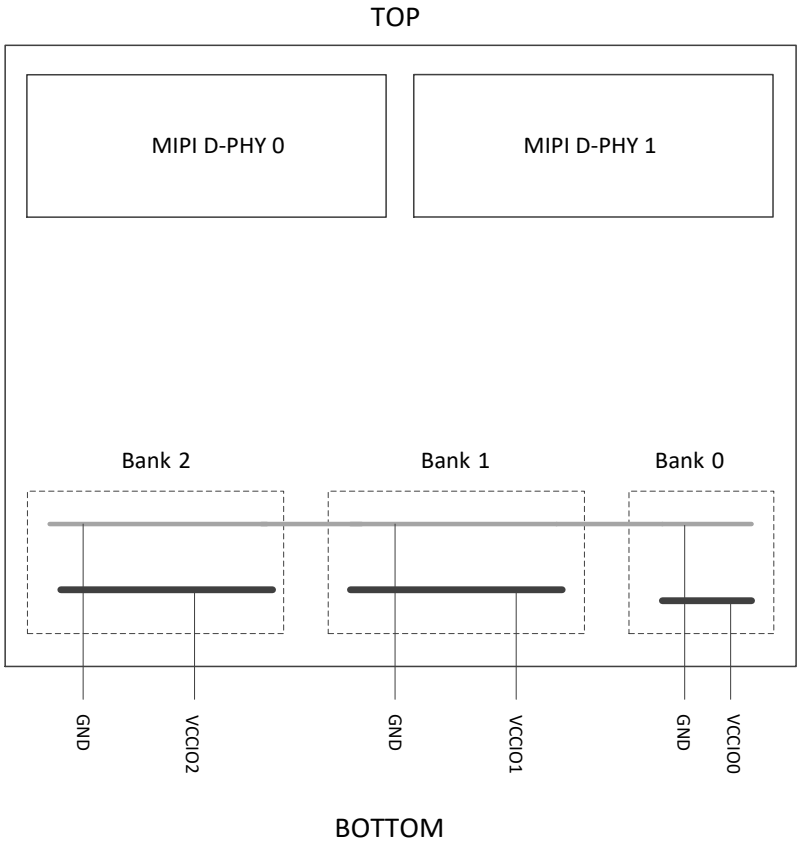

Figure 4.1. sysI/O Banking

4.1. V_{CC} (1.2 V)

CrossLinkPlus devices have V_{CC} core supply. This V_{CC} supply is also used to power the control logic of the sysI/O buffers. The control signals and data signals from the I/O logic are translated to the higher supply of the I/O buffers. When the internal V_{CC} core is powered down during sleep mode, V_{CC} is still powered ON in I/O to maintain I/O personality.

4.2. V_{CCIO} (1.2 V/1.8 V/2.5 V/3.3 V)

Each bank has a separate V_{CCIO} supply that powers the single-ended output drivers and the input buffers such as LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, and LVCMOS12 (output only). The V_{CCIO} voltage applied to the bank determines the input and output standards that can be supported in that bank. It is also used to power the differential output drivers. In addition, V_{CCIO} of Bank 0 is used to supply power to the sysCONFIG™ signals. When V_{CCIO} and V_{CCAUX} are set to the same supply, 2.5 V or 3.3 V, they should be tied together.

4.3. VCCAUX

In addition to the bank V_{CCIO} supplies and a V_{CC} core logic power supply, CrossLinkPlus devices have a V_{CCAUX} auxiliary supply that powers the differential and referenced input buffers. The V_{CCAUX} supply is used for differential receivers and 100 Ω termination blocks inside I/O.

4.4. D-PHY External Power Supplies (1.2 V)

V_{CC_DPHY}, V_{CCA_DPHY}, and V_{CCPLL_DPHY} are supplies used to power the D-PHY.

Table 4.1 shows a summary of all the required power supplies.

Table 4.1. CrossLinkPlus FPGA Power Supplies

Supply	Voltage (Nominal Value[2])	Description
V_{CC}	1.2 V	FPGA core power supply.
V_{CCGPLL}	1.2 V	General Purpose PLL Supply Voltage. Should be isolated from excessive noise.
V_{CCAUX}	2.5 V or 3.3 V	Auxiliary Supply Voltage for Bank 1, 2 and internal Flash programming.
V_{CCIO0}	1.8 V to 3.3 V	I/O Driver Supply Voltage for Bank 0. V_{CCIO0} is used in conjunction with pins dedicated and shared with device configuration.
$V_{CCIO[2, 1]}$	1.2 V to 3.3 V	I/O Driver Supply Voltage for Bank 1, or 2. Each bank has its own V_{CCIO} supply.
V_{CC_DPHYx}[1]	1.2 V	Digital Supply Voltage for D-PHY. Should be isolated from excessive noise.
V_{CCA_DPHYx}[1]	1.2 V	Analog Supply Voltage for D-PHY. Should be isolated and from excessive noise.
V_{CCPLL_DPHYx}[1]	1.2 V	PLL Supply voltage for D-PHY. Should be isolated and “clean” from excessive noise.

Notes:

1. X denotes bank number.
2. Refer to CrossLinkPlus Family Data Sheet (FPGA-DS-02054) for recommended minimum and maximum values.

Table 4.2 lists the I/O Standards that are available in each bank on the device.

Table 4.2. I/O Standards Supported by Various Banks

Description (Types of I/O Buffers)	Harden (Top Side) D-PHY Banks	Bottom Side Bank 0	Bottom Side Bank 1 and Bank 2
Single-ended Output Standards	—	LVTTL LVCMOS33 LVCMOS25 LVCMOS18	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS12
Differential Output Standards	MIPI D-PHY	—	LVDS LVTTL33D LVCMOS33D LVCMOS25D
Single-ended Input Standards	—	LVTTL LVCMOS33 LVCMOS25 LVCMOS18	LVTTL LVCMOS33 LVCMOS25 LVCMOS18
Differential Input Standards	MIPI D-PHY	—	LVDS SubLVDS SLVS LVCMOS25D
On Die Termination	Yes	No	Yes (only for LVDS)

5. sysI/O Buffer Configurations

This section describes the various sysI/O features available on the CrossLinkPlus device.

5.1. Programmable PULLMODE Settings

The CrossLinkPlus sysI/O buffers support programmable pull up resistors on banks. Each of the LVCMOS and LVTTL inputs has a programmable weak pull-up capability that can be enabled if required on Bank 0, Bank 1 and Bank 2. In addition, on Bank 0, the shared sysCONFIG bank, there are programmable I^2C resistors. The available options for Bank 0 are:

- 3P3K (3.3 kΩ)
- 6P8K (6.8 kΩ)
- 10K (10 kΩ)
- UP (100 kΩ)
- NONE

These are mostly used to support I^2C interface, but can also be used for other purposes.

5.2. Output Drive Strength

The CrossLinkPlus outputs have preset drive strengths and cannot be programmed by the user. Table 5.1 lists the available drive settings for each of the output standards.

Table 5.1. LVCMOS Drive Values

V_{CCIO}	Dependent I/O Type	Drive Strength (mA)
3.3	LVCMOS33	8
2.5	LVCMOS25	6
1.8	LVCMOS18	4
1.2	LVCMOS12	2

5.3. Open-Drain Control

All LVCMOS and LVTTL output buffers can be configured to function as open drain outputs. You can implement an open drain output by turning on the OPENDRAIN attribute in the software.

5.4. Differential I/O Support

CrossLinkPlus devices support true differential input buffers on each pair of IOs in the LVDS Bank 1 and Bank 2 with a DIFFDRIVE of 3.5 mA. The performance of the LVDS input buffer is 1.2 Gb/s for flip chip packages. Refer to CrossLinkPlus Data Sheet (FPGA-DS-02054) for more details about 1.2 Gb/s.

5.5. Complementary Outputs

The single-ended driver associated with the complementary pad can optionally be driven by the complement of the data that drives the single-ended driver associated with the true pad. CrossLinkPlus uses pads A and C as true pads and pads B and D as complement pads. This allows a pair of single-ended drivers to be used to drive complementary outputs with the lowest possible skew between the signals. Pads A and B form a Programmable Input/Output (PIO) pair and pads C and D form another PIO pair.

It can be used in conjunction with off-chip resistors to emulate LVDS output drivers. When this option is selected, the tristate control for the driver associated with the complement pad is driven by the same signal as the tristate control for the driver associated with the true pad. In CrossLinkPlus, this option is available for LVCMOS33 and LVCMOS25 outputs.

5.6. On-Chip Termination

Bank 0 in the CrossLinkPlus device is also called config/shared I/O bank. This I/O Bank only supports single-ended input and output. There are programmable I^2C resistors on this bank that can be configured to use one of the internal integrated pull-ups, the weak pull-up is OFF, and the following integrated pull-up values (or equivalent current source through the transition region) are available.

- 3.3 kΩ ± 20%
- 6.8 kΩ ± 20%
- 10 kΩ ± 20%

Bank 1 and Bank 2 support differential and MIPI D-PHY inputs. These banks support the on-chip 100 Ω input differential termination between all pairs of LVDS, SLVS, SubLVDS and MIPI D-PHY inputs. It is statically configured as ON and OFF for all differential input types except MIPI D-PHY.

When the I/O type is MIPI, the on-chip termination is enabled dynamically based on the HSSEL signal. See Table 5.2 for details. The tolerance of this input termination is ± 20% over the operating range of the device.

5.7. Programmable Input Delay

Each input can optionally be delayed before it is passed to the core logic or input registers. The primary use for the input delay is to achieve zero hold time for the input registers when using a direct drive primary clock. To arrive at zero hold time, the input delay stalls the data by at least as much as the primary clock injection delay.

5.8. Standby

The Standby mode is a way to dynamically power down the bank. It disables the differential receiver and True differential driver. The Standby modes are enabled on a bank-by-bank basis, with bit settings and each Bank has user-routed fabric input signals to enable the Standby (Dynamic power down) modes.

Refer to Power Management and Calculation for CrossLinkPlus Devices (FPGA-TN-02111) for more information about the Standby settings for the I/O banks.

5.9. MIPI D-PHY Support

The following primitive should be used when implementing MIPI D-PHY I/O CrossLinkPlus supports High Speed (HS) Rx, Low Power (LP) Rx and Low Power Tx mode. MIPI primitive is supported in Bank 1 and Bank 2.

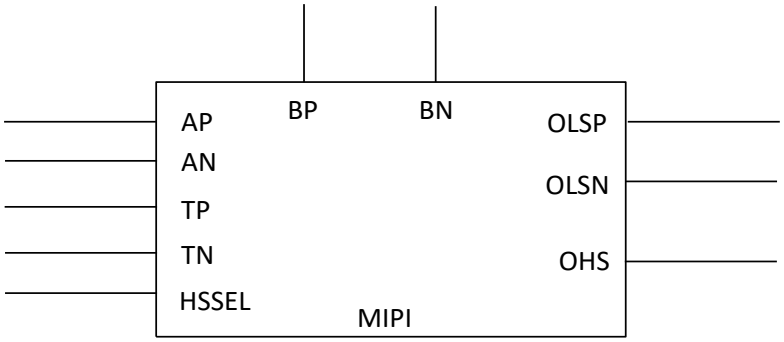

Figure 5.1. MIPI Primitive Symbol

Table 5.2. MIPI Port List

Port	I/O	Description
BP	I/O	Bidirectional PAD A, C used for DPHY Clock/Data HS and LP mode
BN	I/O	Bidirectional PAD B, D used for DPHY Clock/Data HS and LP mode
AP	I	Input from fabric to PAD A, C – used for LP Tx function only
AN	I	Input from fabric to PAD B, D – used for LP Tx function only
HSSEL	I	High Speed Select Signal. HSSEL=1: High Speed mode, 100 Ω differential termination is on. HSSEL=0: Low Speed mode, 100 Ω termination is turned off.
TP	I	Tristate for PAD A,C
TN	I	Tristate for PAD B,D
OLSP	O	LP Rx signal from BP
OLSN	O	LP Rx signal from BN
OHS	O	HS Rx signal from BP/BN differential

When IO_TYPE is MIPI, the MIPI primitive above should be instantiated in the design, otherwise the software Design Rule Check (DRC) errors out. The output from the MIPI D-PHY buffer can only be used with the Double Data Rate (DDR) registers. Refer to CrossLinkPlus High-Speed I/O Interface (FPGA-TN-02102) for details on building MIPI D-PHY interfaces.

6. Software sysI/O Attributes

The sysI/O attributes can be specified in the Hardware Description Language (HDL), using the Spreadsheet View or in the logical preference file (.lpf) file directly. Appendix A and Appendix B list examples of how these can be assigned using each of these methods mentioned above. This section describes in detail each of these attributes.

6.1. IO_TYPE

This is used to set the sysI/O standard for an I/O. The VCCIO required to set these I/O standards are embedded in the attribute names itself. There is no separate attribute to set the VCCIO requirements. Table 6.1 lists the available I/O types.

Table 6.1. IO_TYPE Attribute Values

sysI/O Signaling Standard	IO_TYPE
DEFAULT	LVCMOS25
LVTTL	LVTTL33
LVTTL Differential	LVTTL33D
3.3 V LVCMOS	LVCMOS33
3.3 V LVCMOS Differential	LVCMOS33D
2.5 V LVCMOS	LVCMOS25
2.5 V LVCMOS Differential	LVCMOS25D
1.8 V LVCMOS	LVCMOS18
1.2 V LVCMOS (Output)	LVCMOS12
LVDS 2.5 V	LVDS
SubLVDS	SUBLVDS
SLVS	SLVS
MIPI D-PHY	MIPI

6.2. PULLMODE

The PULLMODE attribute is available for all the LVTTL and LVCMOS inputs and bidirectional I/O. This attribute can be enabled for each I/O independently.

Table 6.2. PULLMODE Settings

Pull Options	PULLMODE VALUE
Weak Pull-up (Default)	UP
I^2C Pull-up Resistors	3P3K (3.3 kΩ), 6P8K (6.8 kΩ), 10K (10 kΩ)
Pull Off	NONE

Table 6.3. PULLMODE Settings

Buffer	Values	Default
Input	UP, NONE, 3P3K, 6P8K, 10K	UP
Output	NONE	NONE

6.3. OPENDRAIN

LVCMOS and LVTTL I/O standards can be set to Open Drain configuration by using the OPENDRAIN attribute.

Table 6.4. Open Drain Attribute Values

Attribute	Values	Default
OPENDRAIN	ON, OFF	OFF

6.4. DIFFRESISTOR

This attribute is used to set the on-chip differential termination on MIPI D-PHY HS, LVDS, SLVS, and SubLVDS inputs.

Table 6.5. DIFFRESISTOR Values

Attribute	Values	Default
DIFFRESISTOR	OFF, 100 (100 Ω)	100

6.5. HYSTERESIS

Hysteresis can be enabled for LVCMOS and LVTTL inputs.

Table 6.6. Hysteresis Attribute Values

Attribute	Values	Default
HYSTERESIS	ON, NA	ON

6.6. DIN/DOUT

This attribute can be used when an I/O register needs to be assigned. Using DIN asserts an input register and using DOUT attribute asserts an output register in the design. By default, the software tries to assign the I/O registers if applicable. You can turn this OFF by using synthesis attribute or using the preference editor of the software. These attributes can only be applied on registers.

6.7. LOC

This attribute can be used to make pin assignments to the I/O ports in the design. This attribute is only used when the pin assignments are made in HDL source. You can also assign pins directly using the Graphical User Interface (GUI) in the Spreadsheet View of the software.

7. Design Recommendations

This section discusses some of design rules and considerations that need to be taken into account when designing with the CrossLinkPlus sysI/O buffers.

7.1. Banking Rules

- If V_{CCIO} for any bank is set to the same voltage as V_{CCAUX} (2.5 V or 3.3 V), it is recommended to connect them to the same power supply to minimizing leakage.
- If V_{CCIO} for either bank 1 or bank 2 is set to 1.2 V, it is recommended to connect it to the same power supply as V_{CC} to minimizing leakage.
- The top of the device has two Hardened DPHY blocks. These blocks are not available for any other functions.
- Bank 0 on the bottom of the device is General Purpose Input/Output (GPIO) and sysConfig bank. Only single-ended I/O standards can be built into this bank.
- Bank 1 and Bank 2 on the bottom of the device support differential Inputs, differential Outputs and singled-ended I/O.
- DIFFRESISTOR can be turned on for each PIO. Only Bank 1 and Bank 2 have this feature.
- I^2C pull-up resistors are only available on Bank 0.
- Only one V_{CCIO} level is allowed in a given bank so all IO_TYPES of that bank should be compatible with that V_{CCIO} level.

Appendix A. HDL Attributes

Using these HDL attributes, you can assign the sysI/O attributes directly in your source. Use the attribute definition and syntax for your synthesis vendor. The sysI/O attributes syntax and examples for Synplify Pro® synthesis tool and Lattice Synthesis Engine (LSE) are listed here. This appendix only lists the sysI/O buffer attributes for these devices. Refer to the Synplify Pro user manual to see a complete list of synthesis attributes. These manuals are available through the Diamond Software Help.

VHDL Synplify Pro and LSE

This section lists syntax and examples for all the sysI/O attributes in VHSIC Hardware Description Language (VHDL) when using Synplify Pro synthesis tool and LSE.

Syntax

Table A.1. VHDL Attribute Syntax for Synplify

Attribute	Syntax
IO_TYPE	attribute IO_TYPE: string; attribute IO_TYPE of *Pinname*: signal is *"IO_TYPE Value"*;
PULLMODE	attribute PULLMODE: string; attribute PULLMODE of *Pinname*: signal is *"Pullmode Value"*;
OPENDRAIN	attribute OPENDRAIN: string; attribute OPENDRAIN of *Pinname*: signal is *"OpenDrain Value"*;
DIFFRESISTOR	attribute DIFFRESISTOR: string; attribute DIFFRESISTOR of *Pinname*: signal is *"DIFFRESISTOR Value"*;
HYSTERESIS	attribute HYSTERESIS: string; attribute HYSTERESIS of *Pinname*: signal is *"HYSTERESIS Value"*;
DIN	attribute DIN: string; attribute DIN of *Pinname*: signal is " ";
DOUT	attribute DOUT: string; attribute DOUT of *Pinname*: signal is " ";
LOC	attribute LOC: string; attribute LOC of *Pinname*: signal is "*pin_locations*";

Examples

IO_TYPE

--*Attribute Declaration***

ATTRIBUTE IO_TYPE: string;

--*IO_TYPE assignment for I/O Pin***

ATTRIBUTE IO_TYPE OF portA: SIGNAL IS "LVCMOS25";
ATTRIBUTE IO_TYPE OF portB: SIGNAL IS "LVCMOS33";
ATTRIBUTE IO_TYPE OF portC: SIGNAL IS "LVDS25";

PULLMODE

--*Attribute Declaration***

ATTRIBUTE PULLMODE: string;

--*PULLMODE assignment for I/O Pin***

ATTRIBUTE PULLMODE OF portB: SIGNAL IS "UP";

OPENDRAIN

--*Attribute Declaration*****

ATTRIBUTE OPENDRAIN: string;

--*Open Drain assignment for I/O Pin*****

ATTRIBUTE OPENDRAIN OF portB: SIGNAL IS "ON";

DIFFERESISTOR

--*Attribute Declaration*****

ATTRIBUTE DIFFRESISTOR: string;

--* DIFFRESISTOR assignment for I/O Pin*****

ATTRIBUTE DIFFRESISTOR OF portB: SIGNAL IS "100";

HYSTERESIS

--*Attribute Declaration*****

ATTRIBUTE HYSTERESIS: string;

--* DIFFRESISTOR assignment for I/O Pin*****

ATTRIBUTE HYSTERESIS OF portB: SIGNAL IS "ON";

DIN/DOUT

--*Attribute Declaration*****

ATTRIBUTE din: string;
ATTRIBUTE dout: string;

--* din/dout assignment for I/O Pin*****

ATTRIBUTE din OF input_vector: SIGNAL IS " ";
ATTRIBUTE dout OF output_vector: SIGNAL IS " ";

LOC

--*Attribute Declaration*****

ATTRIBUTE LOC: string;

--* LOC assignment for I/O Pin*****

ATTRIBUTE LOC OF input_vector: SIGNAL IS "E3,B3,C3 ";

Verilog Synplify Pro and LSE

This section lists syntax and examples for all the sysI/O attributes in Verilog using Synplify Pro synthesis tool.

Syntax

Table A.2. Verilog Synplify Attribute Syntax

Attribute	Syntax
IO_TYPE	*PinType PinName* /* synthesis IO_TYPE="*IO_Type Value*"*/;
PULLMODE	*PinType PinName /* synthesis PULLMODE="Pullmode Value"*/;*
OPENDRAIN	*PinType PinName /* synthesis OPENDRAIN ="OpenDrain Value"*/;*
DIFFRESISTOR	*PinType PinName* /* synthesis DIFFRESISTOR =" *DIFFRESISTOR Value*"*/;
HYSTERESIS	*PinType PinName /* synthesis HYSTERESIS ="Hysteresis Value"*/;*
DIN	*PinType PinName* /* synthesis DIN=" "*/;
DOUT	*PinType PinName* /* synthesis DOUT=" "*/;
LOC	*PinType PinName* /* synthesis LOC="*pin_locations*"*/;

Examples

//IO_TYPE and PULLMODE assignment

```
output portB /*synthesis IO_TYPE="LVCMOS33" PULLMODE ="UP"*/;
output portC /*synthesis IO_TYPE="LVDS" */;
```

//**PULLMODE**

```
output [4:0] portA /* synthesis IO_TYPE="LVCMOS33" PULLMODE = "NONE" */;
```

//OPENDRAIN

```
output portA /*synthesis OPENDRAIN ="ON"*/;
```

//DIFFRESISTOR

```
input portB /*synthesis IO_TYPE="LVDS" DIFFRESITOR="100" */;
```

//HYSTERESIS

```
input portB /*synthesis HYSTERESIS="ON" */;
```

//DIN (Place the flip-flops near the load input)

```
input load /* synthesis din="" */;
```

//DOUT (Place the flip-flops near the load output)

```
output load /* synthesis dout="" */;
```

//LOC (I/O pin location)/input [3:0] DATA0 /* synthesis loc="E3,B1,F3"*/;

Appendix B. sysI/O Attributes Using Spreadsheet View User Interface

The sysI/O buffer attributes can be assigned using the Spreadsheet View in Lattice Diamond design software. The **Port Assignments** sheet lists all the ports in a design and all the available sysI/O attributes in multiple columns. Click on each of these cells for a list of all valid I/O preferences for that port.

Each column takes precedence over the next. Therefore, when you choose a particular IO_TYPE, the columns for the PULLMODE, DRIVE, SLEWRATE, and other attributes only list the valid entries for that IO_TYPE.

Pin locations can be locked using the **Pin** column of the **Port Assignments** sheet or using the **Pin Assignments** sheet. You can right-click on a cell in the **Pin** column and click **Assign Pins** to see the list of available pins. In Spreadsheet View, go to **Design**, then **Preference PIO DRC** to look for incorrect pin assignments.

You can enter the DIN/DOUT preferences using the **Cell Mapping** tab. All the preferences assigned using the Spreadsheet View are written into the logical preference file (.lpf).

Figure B.1 shows the **Port Assignments** sheet of the Spreadsheet View. For further information on how to use the Spreadsheet View, refer to the Diamond Help documentation, available in the Help menu option of the software.

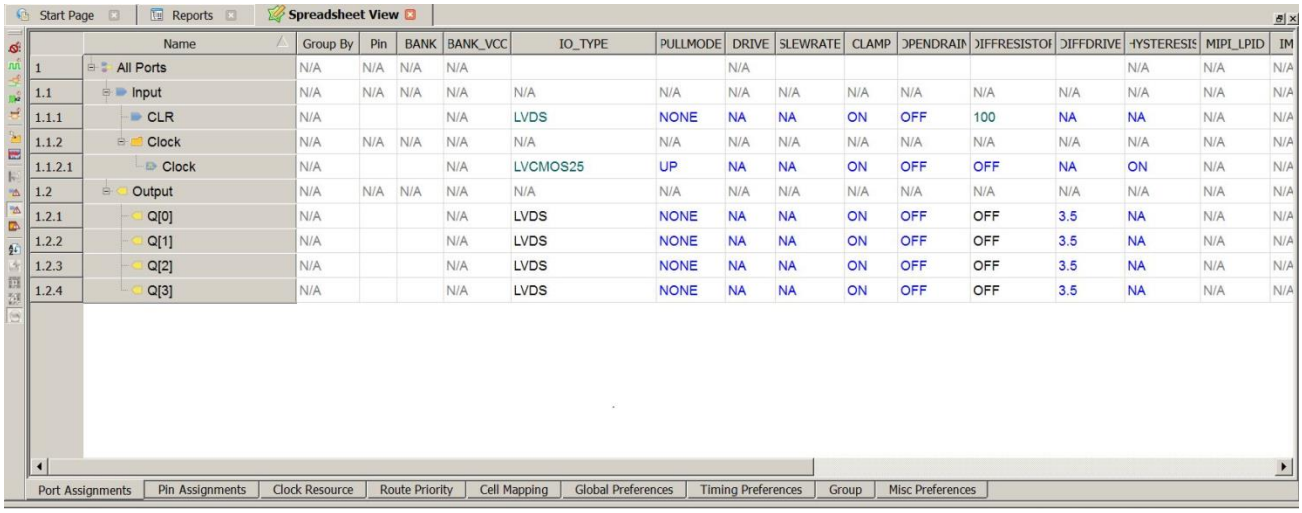

Figure B.1. Port Attributes Tab of Spreadsheet View

References

For more information, refer to the following documents:

- CrossLinkPlus Family Data Sheet (FPGA-DS-02054)
- CrossLinkPlus High-Speed I/O Interface (FPGA-TN-02102)
- CrossLinkPlus Hardware Checklist (FPGA-TN-02105)
- CrossLinkPlus Programming and Configuration Usage Guide (FPGA-TN-02103)
- CrossLinkPlus sysCLOCK PLL/DLL Design and Usage Guide (FPGA-TN-02109)
- CrossLinkPlus Memory Usage Guide (FPGA-TN-02110)
- Power Management and Calculation for CrossLinkPlus Devices (FPGA-TN-02111)
- CrossLinkPlus I2C Hardened IP Usage Guide (FPGA-TN-02112)
- Advanced CrossLinkPlus I2C Hardened IP Reference Guide (FPGA-TN-02135)

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, August 2019

Section	Change Summary
All	Production release

www.latticesemi.com