



Reducing Cost and Power in Consumer Applications Using PLDs

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Lattice Semiconductor
5555 Northeast Moore Ct.
Hillsboro, Oregon 97124 USA
Telephone: (503) 268-8000
www.latticesemi.com

Introduction

The need to respond to changing market standards in a compressed time to market window has led to the widespread use of programmable logic devices (PLDs) in a broad range of consumer applications. While development of application specific integrated circuits (ASICs) and application specific standard parts (ASSPs) requires high non-recurring engineering charges, PLDs are standard off-the-shelf parts that can be customized for different applications using flexible software tools. Unlike ASICs and ASSPs, PLDs do not require long lead times: their functionality can be changed at any time to accommodate a change in product requirements. In many market segments, such as handheld devices, PLDs have found acceptance due to new product architectures that reduce power consumption, feature new packaging options and lower unit cost.

Consumer Applications – Trends and Challenges

Reducing Cost

According to forecasts from iSuppli, revenue from sales of consumer electronics equipment in 2010 is projected to reach \$259 billion, marking an end to the market contraction of prior years. And in an ongoing sign of strength, revenue will continue to rise in the coming years, increasing by 6.7 percent in 2011 and by 7 percent in 2012. The increase in revenue is fuelled by sales of high volume products such as blue ray DVD players, LCD TVs, set-top-boxes, digital cameras, smart phones and GPS devices. In line with this, new equipment will be designed to address the needs of emerging markets at substantially lower price points as consumers look for more value and features in their purchases. As a result, designers are faced with continual pressure to deliver lower cost products with higher levels of system integration.

Reducing the Power Budget

Reducing static power has been an ongoing challenge for designers of consumer applications. For many battery powered applications such as smart phones, GPS devices, mobile computing and digital cameras, prolonged battery life is one of the most important differentiating features. Low power is also becoming important for many electronic appliances that are powered through wall sockets, as designers seek to comply with the latest EnergyStar and EC Code of Conduct regulations.

Shrinking Product Life Cycle

The consumer electronics market is rapidly evolving, as indicated by the continuous emergence of new standards that improve the quality and affordability of consumer electronics products. Two trends - proliferation of broadband access for both wired and wireless devices, and convergence of media and data - are driving the development of these new standards.

Manufacturers are under tremendous competitive pressure to be the first-to-market with differentiated products. However, a successful product quickly attracts competitive copycats, leading to rapid price erosion. To stay ahead of the competition, consumer manufacturers are forced to constantly enhance their products or support emerging technologies. For these reasons, there is a dramatic reduction in the consumer product life cycle.

PLD Usage in Consumer Applications

With improved architectures that reduce power consumption, new packages for smaller form factors, lower cost per unit and a high level of product differentiation, PLDs are increasingly being used in consumer applications. In many consumer systems, PLDs can extend the usage of the current generation of the applications processor or CPU by providing advanced bus interfacing and bridging functions. These bus interfacing and bridging functions usually do not

have very high performance requirements. Figure 1 shows an example of such an application.

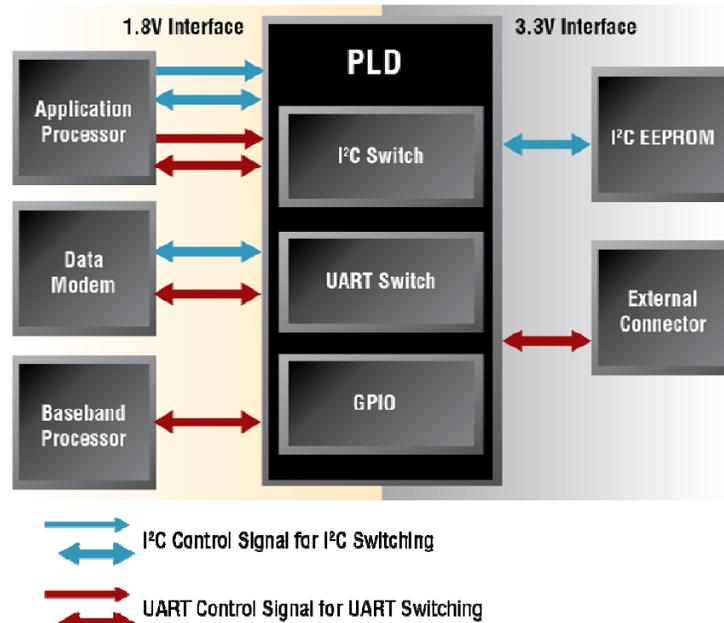


Figure 1: PLD Usage in Mobile Phones

PLDs are also routinely used to implement human machine interface controllers, display controllers, external memory interface controllers and PWM controllers. Table 2 shows some common PLD applications in the consumer space. Sometimes two or more functions are combined to address a particular requirement; an example of one such application is shown in Figure 2.

PLD Function	Example Application
Human Machine Interface Controller	Keyboard Matrix Decoder, Digital Touchscreen Control, Interrupt Manager.
Display Controller	Image Rotation, Image Scaling, LCD Control, Display Interface Multiplexing/Demultiplexing
External Memory Interface Controller	Controllers for Secure Digital (SD) Memory, Compact Flash (CF) Memory, Memory Stick, DDR/DDR2/LPDDR Memory
PWM Controller	LCD Backlight Control, Stepper Motor Control
Bus Interfacing and Bridging	I ² C, SPI, UART, I ² S, USB, SDIO

Table 1: Common PLD Functions in Consumer Applications

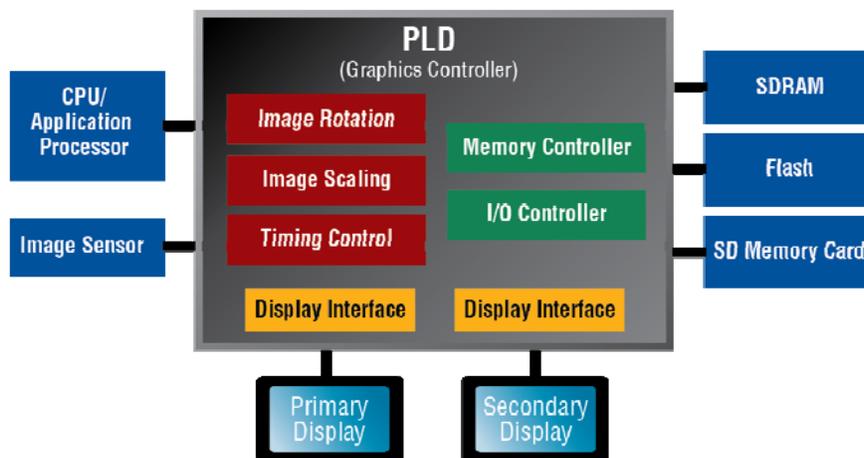


Figure 2: PLD Example Application in Digital Cameras

Like high end FPGAs, low density PLDs now have advanced I/O capabilities, including support for different I/O standards, multiple I/O banks, and multiple voltages. These features allow the PLD to be used to implement interconnect logic between ASICs/ASSPs, memories, processors and other devices that often have mismatched voltages and I/O standards.

As shown in Figure 3, a Graphics Multiplexer is an ideal example of low-cost, low density PLDs used for advanced interconnects logic. The latest trend in laptops and portable power management is the Intel Switchable Graphics Initiative. The Graphics Multiplexer selects a graphics controller based on application requirements. The low-power integrated GPU is used for routine applications such as word processing, e-mail and Internet browsing. The high-performance discrete GPU is used for high performance applications such as gaming, video editing and playing HD video. Support for low-swing differential I/O standards and built-in gear boxes and PLLs enables the PLD to interface with graphics processors, implement intelligent multiplexer algorithms to minimize or eliminate visual artifacts in switching and directly drive the LCD screens.

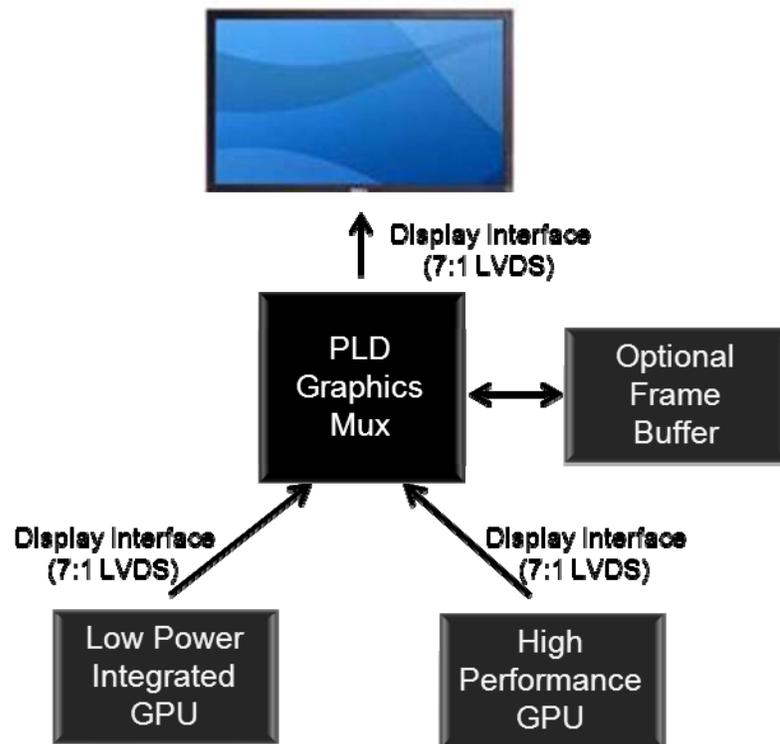


Figure 3: PLD-Based Graphics Multiplexer

Lattice's MachXO2 PLD family is an ideal fit for the functions used in the consumer applications described above. Combining optimized lookup table (LUT) architecture with 65-nm embedded Flash process technology, MachXO2 devices provide a flexible “Do-it- All” solution for consumer designs.

Lowering Costs with MachXO2 Devices

Pad Limited Design

Historically for high-volume, price-sensitive applications, PLDs were not the lowest-cost solution. However, this changed as both ASICs and PLDs started becoming pad limited. In pad-limited designs, the die size is determined solely by the number of required I/O pads and not by the amount of logic in the core. Price is ultimately dictated by die size – when devices become pad limited, the pricing difference between a custom and programmable product begins to narrow. MachXO2 devices are designed to be pad limited. The I/O pads are laid out in double or triple staggered I/O rings depending on device density, minimizing the die size for a given number of IOs.

Low Cost Packages

MachXO2 devices are available in a broad range of low cost, halogen-free packages. Available package options include low cost BGAs and TQFP, as well as advanced wafer level chip scale packages and micro chip scale packages. The BGA package includes the fewest possible signal routing layers to reduce total package cost. These packages are designed such that all the I/O and power supply connections breakout in two to four layers of PCB routing. Doing so avoids the use of higher cost manufacturing techniques such as buried or blind vias and laser drilled vias. I/O assignment on MachXO2 packages was done to enable density migration within the same package. This helps in leveraging the same board through the possible design changes, requiring a larger or smaller MachXO2 device.

Functional Integration

Designers are often faced with the challenge of supporting a high level of functionality to reduce total cost. Discrete devices increase cost, board real estate requirements and the total power budget of the system. Discrete devices are also associated with lower board reliability. All of these attributes make higher functional integration more desirable for consumer applications.

MachXO2 devices enable a high level of system integration including a single chip solution that does not require an external configuration memory, external user Flash memory or EEPROMs and oscillator resulting in reduced board area, component count and total system cost.

Figure 4 shows a single MachXO2 device integrating discrete logic such as I/O expanders, voltage level and bus bridging translators, voltage regulator, clock sources and configuration devices, all in a single device.

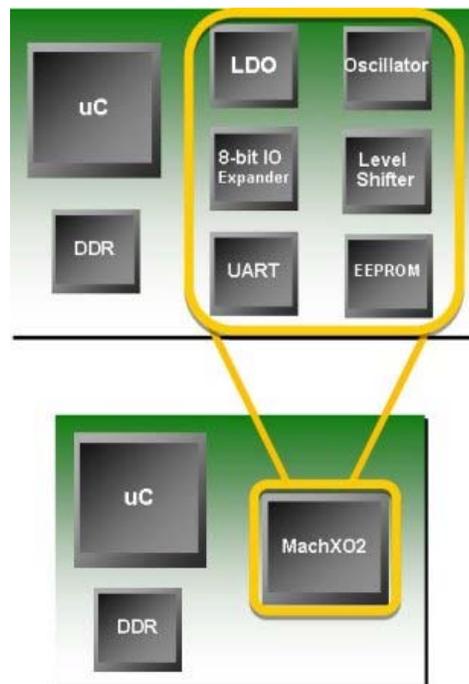


Figure 4: MachXO2 functional integration

Integrate External Non-volatile Memory

MachXO2 devices include up to 256Kbits of embedded Flash memory. This on-chip User Flash Memory (UFM), enables the MachXO2 devices to integrate the external non-volatile memory, and can be used for a variety of applications, including storing a portion of the configuration image, storing PROM data or, as a general purpose User Flash Memory.

Reduce Number of Oscillators

MachXO2 devices have an internal oscillator with a nominal accuracy of +/- 5% that can be used as a clock source in a design, eliminating the need for an external oscillator.

Hardened SPI, I²C, Timer/Counter

SPI and I²C controllers and timer/counters are among the most commonly implemented functions in consumer designs. Designers often implement SPI or I²C bus expansion in PLDs. Timer/Counters are also frequently used to generate status signals. All MachXO2 devices include hardened implementations of these commonly used functions. With hardened I²C, SPI and timer/counter functions, designers can save up to 600 LUTs for additional logic implementation in their designs. Table 2 shows the savings logic requirements that can be realized by hardening commonly used control functions.

Function	Typical LUTs required in PLDs	Typical LUTs required in MachXO2 Devices
SPI Master	115	0
I ² C Master	234	0
Timer/Counter	50-80	0

Table 2: Typical Logic Requirement Saving by Using Hardening I²C, SPI and timer/counter functions

Lowering Power Budget with MachXO2 Devices

Static and Dynamic Power

Total power in a PLD is the sum of two main components: static power and dynamic power. Static power results primarily from transistor leakage current in the device. Leakage current is the small current that "leaks," either from source-to-drain or through the gate oxide, even when the transistor is logically "off."

Dynamic power is the power consumed during switching events in the core or I/O of the device and it is, therefore, frequency and user dependent.

Static power depends on the design of the PLD itself and cannot be controlled by the design. MachXO2 PLDs have been designed to minimize static power through innovative techniques at the process, circuit design and architecture levels. These include the use of a low power 65-nm process, variable channel lengths, optimized transistor selection and improved routing defaults and algorithms, resulting in standby power as low as 19uW for 256 LUTs. Figure 5 shows a comparison of static power between 65-nm MachXO2 and 130-nm MachXO devices.

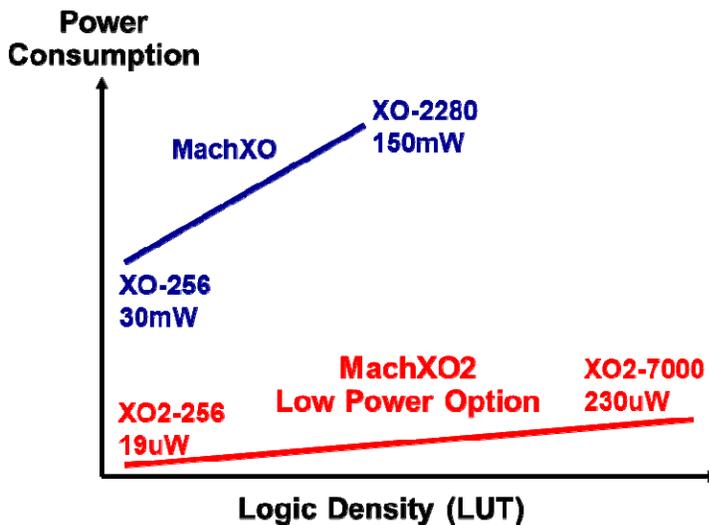


Figure 5: Static Power Comparison between MachXO2 and MachXO PLDs

Since dynamic power depends on the number of nodes switching at a time, it is more design dependent. Designers can use various techniques to reduce dynamic power. For example, enabling the clock at the source of the clock tree rather than at individual end points minimizes clock transitions in the system. I/Os also contribute significantly to dynamic power. Using LVTTTL/LVCMOS standards and lower I/O voltages helps reduce power. Use of lower swing differential signaling also reduces dynamic power. MachXO2 devices provide a number of architectural features to reduce dynamic power consumption, such as power controller, I/O bank controller, dynamic clock enable, power guard and programmable low-swing differential signaling.

Lower Power Due to Non-Volatility

In addition to static and dynamic power there is an additional component of power related to inrush and configuration. This is the power consumed during power-up and configuration, before the PLD/FPGA enters user mode. Power dissipated is proportional to the time required to enter user mode. Board

designers must account for this additional power while determining power requirements. Many consumer systems are designed such that the FPGA or PLD frequent On/Off cycles. This system behavior worsens this additional power dissipation due to frequent On/Off cycles. Due to their inherent nature (i.e. PLD with on-chip configuration memory), MachXO2 devices can configure themselves in microseconds, minimizing power dissipation during inrush and configuration. Figure 6 shows a comparison between the time required to enter user mode for MachXO2 PLDs and SRAM-based FPGAs.

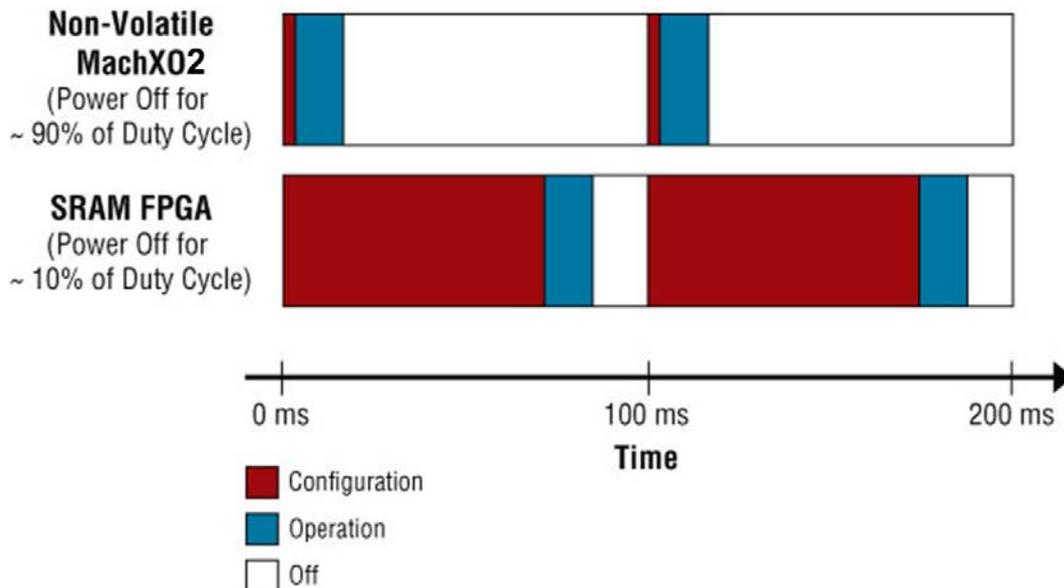


Figure 6: MachXO2 Low Power Cycling

Rapid Innovation with Free Design Tools

Designers can start designing with MachXO2 devices using the Lattice Diamond v1.1 software, which can be downloaded for free from the Lattice website. Alternatively, they can also use the free ispLEVER® v8.1 SP1 Starter software with an installed control pack that can be downloaded from the Lattice website.

A comprehensive suite of reference designs optimized for consumer applications can be downloaded for free from the Lattice Website. These include (list a few consumer ref designs). The reference design source, including HDL and Firmware, can be modified depending on application requirements. For more information on the reference designs visit <http://www.latticesemi.com/ip>

Conclusion

PLDs are a good choice for implementing functions in consumer applications because they overcome the limitations of ASICs and ASSPs by providing a cost-effective, low power and flexible solution. The MachXO2 PLD family is designed for low cost, low power consumer applications and offers designers the benefits of lower cost, reduced power consumption, and increased system integration in a small footprint. In addition, MachXO2 devices include hardened implementations of some of the most popular functions used in consumer applications, such as User Flash Memory (UFM), I²C, SPI and timer/counter.