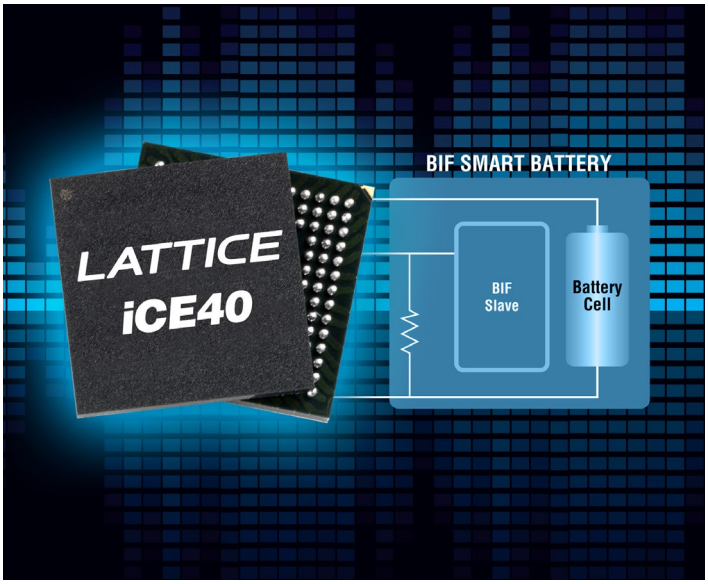
Battery Interface using iCE40

Low Cost Solution for MIPI Battery Interface in Mobile Devices

The mobile handheld industry has witnessed explosive growth in recent years. Smart phones, tablets and other battery powered devices available today have evolved to become personal internet devices with rich features that are always connected. The use of dual-core and quad-core processors is becoming mainstream in many such devices to create a more compelling user experience. The increase in power consumption has downstream effects on power delivery, battery life and longevity. One of the challenges faced by mobile system designers is balancing between optimal battery capacity, chemistry, power delivery, safety and form factor.

The MIPI Battery Interface (BIF) is a comprehensive battery communication interface standard for mobile devices. The communication protocol established by BIF provides a method for system designers to read parameters on demand to optimize power consumption during device use and to optimize battery charging. It also provides a method to authenticate batteries for systems that need to ensure user safety. BIF is a single wire interface that supports the use of one or more smart batteries and/or low cost batteries in the same system.

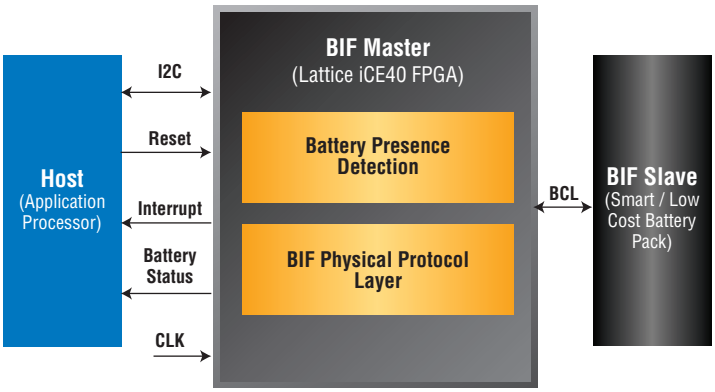
The block diagram below illustrates the implementation of MIPI BIF Master using the Lattice iCE40 ultra low densityFPGA. Communication over the BIF battery communication line (BCL) is enabled using the Lattice CMD solution. The Lattice CMD is connected to the host application processor using the I2C protocol. A simple protocol is defined on top of the I2C standard to communicate between the host and CMD. The host interface can be easily customized using the Lattice solution. In addition, any further customization of the BIF interface / protocol can be achieved using the Lattice CMD solution. The Lattice solution utilizes <<1K LUTs providing the flexibility for the customer to even integrate other system functions within the same Lattice FPGA device. The Lattice MIPI BIF solution will be made available as a standard Intellectual Property (IP) though Lattice iCEcube2™ software suite.



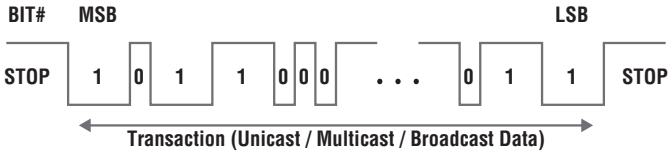
Key Features and Benefits

- **Host Connectivity**
  - Customizable interface to host such as I2C, SPI, etc.
- **Ultra-Low Power**
  - Power as low as 100µA static
- **Low Cost**
  - Utilizes <1K LUTs
- **Broad Package Portfolio**
  - Footprints as small as 2.5 x 2.5 mm
  - 0.4 mm BGA pitch suited for Smartphones and tablet applications
- **Proven interoperability with multiple slaves**

MIPI BIF Master Implementation



Conceptual Diagram of the BIF Protocol



Communication is achieved using time distance coding and supports the use of broadcast words (master to all slaves), Multicast words (master to selected slaves) and Unicast words (selected slave to master).

Lattice iCE40 FPGA Family

Lattice's iCE40 FPGA family is designed for connectivity, video and imaging, sensor management, and memory/storage expansion applications.

Fabricated on a 40nm low-power, standard CMOS process, the iCE40 family has been optimized for applications requiring ultra low power and low cost, such as smartphones, tablets, digital still camera, e-books readers, and portable navigation devices. The iCE40 family comes in two power/performance variants.

Development Tools

Lattice's iCEcube2 development software is a feature-rich development platform that supports the development with Lattice's iCE40 FPGA devices. The iCEcube2 development software integrates Synopsys' Synplify Pro® synthesis tool with Lattice's physical design tools (placement & routing).

The iCEcube2 design environment includes key features and functions that help facilitate design for mobile applications. They include a project navigator, constraint editor, floorplanner, package viewer, power estimator, and static timing analyzer.

iCE40 Device Selection Guide

	LP-Series Optimized for ultra-low power applications (1.0 Volt and 1.2 Volt Operation)				HX-Series Optimized for display, memory and SERDES applications (1.2 Volt Operation)		
Feature	**LP384**	**LP1K**	**LP4K**	**LP8K**	**HX1K**	**HX4K**	**HX8K**
Logic Cells	384	1280	3520	7680	1280	3520	7680
Embedded RAM Bits	0	64K	80K	128K	64K	80K	128K
Phase-Locked Loops	0	1	2	2	1	2	2
Core Icc @ 0KHz[1]	21µA	100µA	360µA	360µA	267µA	667µA	1100µA
Package	**Programmable I/O: Max I/O (LVDS Channels)**						
32-pin QFN (5 x 5 mm)	21 (4)						
36-ball ucBGA (2.5 x 2.5 mm)	25 (3)	25 (3)[2]					
49-ball ucBGA (3 x 3 mm)	37 (6)	35 (5)					
81-ball ucBGA (4 x 4 mm)	55 (3)	63 (8)	63 (9)[2]				
81-ball csBGA (5 x 5 mm)		62 (8)					
84-pin QFNS[2] (7 x 7 mm)		67 (7)					
100-pin TQFP/VQFP (14 x 14 mm)					72 (9)[2]		
121-ball ucBGA (5 x 5 mm)		95 (12)	93 (13)	93 (13)			
121-ball csBGA (6 x 6 mm)		92 (12)					
132-ball csBGA (8 x 8 mm)					95 (11)	95 (12)	95 (12)
144-pin TQFP (20 x 20 mm)					96 (12)	107 (14)	
225-ball ucBGA (7 x 7 mm)			167 (20)	178 (23)			178 (23)
256-ball caBGA (14 x 14 mm)							206 (26)

1. At 1.2V Vcc
2. No PLL Available
3. Only 1 PLL Available

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March 2013
Order #: I0224B