LatticeXP Family

Instant-On, Single-Chip FPGA with High Security

LatticeXP devices bring together the "instant-on" and non-volatility of Flash with the reconfigurability of SRAM – all in a single low-cost chip. No other FPGA vendor offers the benefits of non-volatility and infinite reconfigurability in a low-cost FPGA architecture, delivering complete density migration.

The LatticeXP family utilizes the same proven FPGA fabric as Lattice’s popular LatticeECP™ and LatticeEC™ FPGA families. This highly efficient FPGA fabric is optimized to deliver the best balance of features for cost-sensitive high-volume applications. The LatticeXP family offers flexible I/O capabilities, distributed memory, embedded memory, high-performance logic and superior routing.

A non-volatile Flash cell array distributed within the LatticeXP device stores the device configuration. By eliminating the external configuration bitstream and by providing a security scheme that prevents program readback, the LatticeXP family delivers secure FPGA solutions. LatticeXP devices are ideal for low cost, instant-on, security-sensitive systems.

LatticeXP – A Superior FPGA Solution

**INSTANT-ON**
- Self-configuration in less than 1mS
- Ideal for critical system "heartbeat" control logic
- Supports fast configuration "scrubbing"

**HIGH SECURITY**
- LatticeXP devices include security circuitry to prevent readback
- No external bitstream – secure from bitstream "snooping"
- Excellent solution for security sensitive applications

**SINGLE CHIP SOLUTION**
- Perfect for space-constrained applications
- Save boot PROM costs
- Simplify design

**SRAM + FLASH**
- Real time reprogramming of device during operation

**Key Features and Benefits**

- **Non-Volatile, Infinitely Reconfigurable**
  - Reconfigurable SRAM-based logic combined with Flash non-volatile memory
  - SRAM and non-volatile memory programmable through system configuration and JTAG ports
  - Dedicated security circuitry

- **TransFR™ Technology Allows Simple Field Upgrades**

- **Extensive Density and Package Options**
  - 3.1K to 19.7K Look-up Tables (LUTs)
  - TQFP, PQFP and lpBGA packages
  - 62 to 340 I/Os
  - Density migration supported

- **Embedded and Distributed Memory**
  - 54 Kbits to 396 Kbits sysMEM™ Embedded Block RAM
  - Up to 79 Kbits distributed RAM

- **Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTL
    - SSTL 18 Class I
    - SSTL 3/2 Class I, II
    - HSTL15 Class I, III
    - HSTL 18 Class I, II, III
    - PCI
    - LVDS, Bus-LVDS, LVPECL, RSDS

- **Dedicated DDR Memory Support**
  - Implements interfaces up to DDR333 (166MHz)

- **sysCLOCK™ PLLs**
  - Up to 4 analog PLLs per device
  - Clock multiply, divide and phase shifting

- **Sleep Mode Reduces Standby Power to <100µA**

- **System Level Support**
  - IEEE Standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer capability
  - Onboard oscillator for configuration
  - Operate with 3.3V, 2.5V, 1.8V or 1.2V power supply
LatticeXP Architecture

Architecture Overview
LatticeXP FPGAs are designed to offer exceptional functionality, performance and value. Built with an extremely efficient architecture, these low-cost, non-volatile, infinitely reconfigurable FPGAs deliver high performance sysMEM embedded RAM blocks, distributed memory, sysCLOCK PLLs, DDR memory interface, sysIO buffers, and more.

ispXP Technology
ispXP™ technology gives FPGA device designers a superior programmable solution. LatticeXP devices provide logic availability within microseconds of power-up / reconfiguration, reprogrammability and high security ... all in one chip. Significant savings accrue in board space, system design effort, inventory costs, handling costs, and manufacturing costs. With LatticeXP devices, designers will improve time-to-market and lower costs.

ispXP PROGRAMMING AND CONFIGURATION

Instant-On – Fast SRAM configuration via on-chip Flash memory.

Programmable Function Unit Blocks (PFU)
The core of LatticeXP devices consists of Programmable Functional Units (PFU) and PFUs without RAM (PFF). The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions.

- Four Slices per PFU
- Each Slice Individually Programmable
- Slices can be Concatenated for Longer Functions
- PFUs can be Concatenated for Complex Functions

PFU BLOCK DIAGRAM

SLEEP MODE REDUCES POWER BY A FACTOR OF 1000X!

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Normal Mode</th>
<th>Off</th>
<th>Sleep Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLEEPN Pin</td>
<td>High</td>
<td>–</td>
<td>Low</td>
</tr>
<tr>
<td>Static ( I_{CC} )</td>
<td>Typically &lt;100mA</td>
<td>0</td>
<td>Typically &lt;100µA</td>
</tr>
<tr>
<td>Power Supplies</td>
<td>Normal Range</td>
<td>Off</td>
<td>Normal Range</td>
</tr>
<tr>
<td>Logic Operation</td>
<td>User Defined</td>
<td>Non Operational</td>
<td>Non Operational</td>
</tr>
<tr>
<td>I/O Operation</td>
<td>User Defined</td>
<td>Tri-State</td>
<td>Tri-State</td>
</tr>
</tbody>
</table>

LatticeXP Block Diagram

ispXP Capability offers instant-on start-up and security from bitstream snooping. On-chip Flash memory configures SRAM in microseconds.

Mixed Voltage Support
LatticeXP devices are offered in two versions, a version that operates with a 1.2V core power supply, and another version that can operate with 1.8, 2.5 and 3.3V core power supplies. Both versions have independent I/O banks that support 1.2, 1.5, 1.8, 2.5 and 3.3V I/O supply voltages and, with external resistors, can interface with 5V I/O legacy systems.
**LatticeXP Capability**

- Offers instant-on start-up and security from bitstream snooping.
- On-chip Flash memory configures SRAM in microseconds.

**sysCONFIG™ Port**

- Supports serial and parallel configuration.

**sysCLOCK PLLs**

- For clock management.

**sysMEM Embedded Block RAM (EBR)**

- Provides 9kbit true dual port RAM at up to 250MHz.

**DDR Interface Support**

LatticeXP devices provide designers with dedicated DDR interfaces to easily connect LatticeXP FPGAs to external DDR memory:
- Precision DQS Delay Control
- Dedicated DDR Registers (For Mux/Demuxing)
- Automatic DQS to System Clock Domain Transfer
- Half Clock Transfer
- High Performance (DDR333/166 MHz)

**sysMEM Embedded Block RAM (EBR)**

LatticeXP FPGAs include flexible sysMEM EBR blocks. sysMEM EBR blocks provide on-chip memory resources to support a broad range of features:
- 54K Bits to 396K Bits sysMEM Embedded Block RAM (EBR)
- 250MHz Operation
- Multiple Blocks per Device
- Configurable Width and Depth
- Single-Port, Dual-Port and Pseudo-Dual-Port
- Bus Size Matching
- RAM Initialization and ROM Operation
- Memory Cascading

**sysIO Buffer Supports High-Bandwidth I/O Standards**

With Lattice's sysIO interfaces, LatticeXP devices can easily communicate with a variety of devices, supporting many single-ended and differential I/O standards:
- sysIO Interfaces Support
  - LVCMOS / LVTTL
    - Hotsocketing capable
    - Programmable slew rate
    - Programmable drive strength
    - Programmable pull-up, pull-down, bus friendly
    - Programmable open drain
  - PCI, LVDS, SSTL, HSTL, Differential HSTL, Differential SSTL, LVPECL, BLVDS, RSDS
  - 700Mbps+ I/O buffers
  - 333Mbps DDR memory interfaces
- Eight I/O Banks Per Device
## TransFR – Easy Field Updates

LatticeXP devices include Lattice's exclusive Transparent Field Reconfiguration (TransFR) technology. TransFR technology allows logic to be updated in the field without interrupting system operation.

Thanks to its dual SRAM and Flash configuration space architecture, LatticeXP devices require less than 2mS to reconfigure, an order of magnitude lower than competing solutions. To change the logic configuration, simply program the Flash in the background while the logic functions normally. In a single command, Lattice's ispVM® software locks the I/Os, copies Flash to SRAM, allows the data state to be initialized and unlocks the pins. Your logic is upgraded instantly!

### ispLEVER Design Tools

Lattice's ispLEVER® software is a comprehensive design environment for the LatticeXP architecture. The ispLEVER tools include everything you need for design entry, synthesis, map, place & route, floorplanning, simulation, project management, device programming and more. Synthesis and simulation tools from industry leaders Mentor Graphics and Synplicity are included with ispLEVER.

### ispLeverCORE™ Intellectual Property

Lattice offers an expanding portfolio of IP cores to support the easy integration of commonly used functions, including:
- PCI Master/Target and Target 64-bit and 32-bit
- DDR Memory Controllers
- SDRAM Memory Controllers
- DMA Controllers
- 10/100/1G Ethernet MAC
- I²C Controller
- and more...

For additional IP cores, go to www.latticesemi.com/ip. Lattice’s ispLeverCORE Connections partners also offer a wide range of IP for the LatticeXP family.

## Device Selection Guide

### Parameter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>LFXP3</th>
<th>LFXP6</th>
<th>LFXP10</th>
<th>LFXP15</th>
<th>LFXP20</th>
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<tbody>
<tr>
<td>PFU/PFF Rows</td>
<td>16</td>
<td>24</td>
<td>32</td>
<td>40</td>
<td>44</td>
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<tr>
<td>PFU/PFF Columns</td>
<td>24</td>
<td>30</td>
<td>38</td>
<td>48</td>
<td>56</td>
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<tr>
<td>Number of PFUs/PFFs</td>
<td>384</td>
<td>720</td>
<td>1216</td>
<td>1932</td>
<td>2464</td>
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<tr>
<td>LUTs (K)</td>
<td>3.1</td>
<td>5.8</td>
<td>9.7</td>
<td>15.4</td>
<td>19.7</td>
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<tr>
<td>Distributed RAM (K bits)</td>
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<td>39</td>
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<tr>
<td>EBR Block SRAM (K bits)</td>
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<td>Number of EBR SRAM Rows</td>
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<tr>
<td>Number of EBR SRAM Blocks</td>
<td>6</td>
<td>8</td>
<td>24</td>
<td>36</td>
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<tr>
<td>$V_{CC}$ Voltage (V) Options</td>
<td>1.2/1.8/2.5/3.3V</td>
<td>1.2/1.8/2.5/3.3V</td>
<td>1.2/1.8/2.5/3.3V</td>
<td>1.2/1.8/2.5/3.3V</td>
<td>1.2/1.8/2.5/3.3V</td>
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<td>Number of PLLs</td>
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<td>Maximum Number of I/Os</td>
<td>136</td>
<td>188</td>
<td>244</td>
<td>300</td>
<td>340</td>
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</table>

### Packages & I/O Combinations

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<th>LFXP10</th>
<th>LFXP15</th>
<th>LFXP20</th>
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</thead>
<tbody>
<tr>
<td>100-pin TQFP (14 x 14 mm)</td>
<td>62</td>
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<tr>
<td>144-pin TQFP (20 x 20 mm)</td>
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<td>208-pin PQFP (28 x 28 mm)</td>
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<td>256-ball fpBGA (17 x 17 mm)</td>
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<tr>
<td>388-ball fpBGA (23 x 23 mm)</td>
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<tr>
<td>484-ball fpBGA (23 x 23 mm)</td>
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