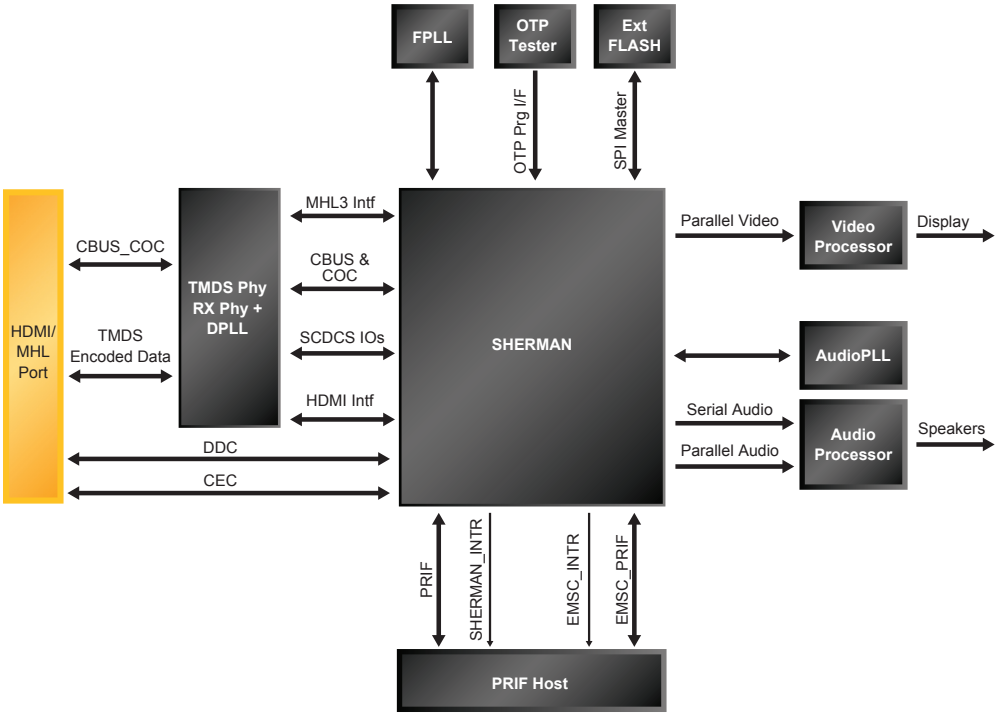
Lattice Semiconductor HDMI® 2.0 Receiver IP

Lattice HDMI 2.0 receiver controller IP is an HDMI 2.0 and HDMI 1.x digital RX IP core. The digital logic supports HDMI 2.0 and HDMI 1.x specifications, 600MHz, HDCP 2.2 RX, CEA-861F, video color space conversion and audio extraction. It is backward compatible with DVI 1.0 and supports the HDCP 2.2 algorithm for decryption of encrypted digital data. Additional features include: controller to access HDCP key ROM, HDCP repeater, 1-bit audio, high bitrate audio (HBR) support, Sony/Philips digital interface (SPDIF) and support for 32 channels of I²S audio.

SoC With HDMI 2.0 Receiver Interface IP



Key Features

HDMI 2.0 Controller

- Backward compatible with HDMI 1.4
- Supports dynamic DDC read requests for any SCDC status updates
- Supports CEA-861-F video resolutions
- Supports ITU-BT-2020 video formats
- Supports 4:2:0 pixel encoding with Deep Color support
- 4Kx2K, 60 Hz, 4:4:4 video formats support
- HDMI 2.0 HBR audio support up to 1536 kHz
- Parallel audio interface to enable implementation of added HDMI 2.0 audio extensions
  - 3D audio supports 10.2, 22.2, and 30.2 speaker placement
  - Multi-stream audio to support multiple video streams or multi-view video streaming
  - New audio packets to support additional audio extensions

HDCP 2.2

- Compliant with HDCP 2.2 specification for HDMI 2.0 and HDCP 1.4 specification for HDMI 1.4b
- Integrated Lattice IP HDCP 2.2 Encoder with embedded 8051
- Embedded OTP ROM with BIST controller

HDMI 2.0 PHY

- Compliant with HDMI 1.4/2.0 and DVI 1.0 standards
- Easy integration into customer's SoC with a corresponding HDMI Rx Digital IP core
- Supports 25~600MHz link clock and 8/10/12 bit color mode
- Supports both DC and AC coupled transmitter
- Long cable support (using HDMI cable and connector)
  - >10m at 75MHz, > 5m at 225MHz
  - Preset adaptive equalization
  - Preset adaptive PLL bandwidth control

Controller Interface

Video Interface

- 10 bpp/12 bpp Deep Color for RGB or YCbCr 4:4:4
- 16/20/24-bit YCbCr 4:2:2
- 10-bit or 12-bit YCbCr 4:2:0 for 4Kx2K
- Multi-colorspace converter: Programmable 3x3 matrix operator, plus 64 pre-defined sets of coefficients for standard color space
- Up-/down-sampling between 4:4:4 and 4:2:2, 4:2:2 and 4:2:0
- Dithering

Audio Interface

- 8-channel I²S
- 8-channel DSD
- S/PDIF (PCM, Dolby Digital, DTS) Packetized Parallel Audio Interface (PAI) for 3D and multi-stream audio

PHY Interface

- IP is designed to interface with Lattice HDMI 2.0 PHY

Misc. Interface

- I²C slave for register access
- SPI slave for HDCP 2.2 PRAM fast access
- Parallel Register Interface (PRIF) for easy integration to SoC for register access

Deliverables

Controller Deliverables

- **Licensed Core Deliverable:**
  - Synthesizable and un-encrypted Verilog RTL for HDMI 2.0 RX digital supporting HDCP 2.2
- **Licensed Core Scripts and Environment:**
  - Synopsys synthesis example scripts and constraint files
  - Prime Time pre-layout scripts
  - Conformal LEC formal verification example scripts
  - Simulation Environment in System Verilog
  - Test bench to verify IP
  - Regression test suite
  - Test invoking scripts
- **Licensed Core Documentation:**
  - Integration guidelines document
  - Design overview, I/O description document
  - Test bench description and regression list document
  - Programming registers spreadsheet with description
  - Digital design datasheet
- **Software Deliverable:**
  - Reference software in source code for configuration and control of licensed core
  - Software documentation

PHY Deliverables

- **GDS for the HDMI PHY IP hard macro and glue logic as RTL**
- **.lib timing views (slow, typical, fast)**
- **LVS netlist**
- **LVS/DRC log file**
- **Integration guidelines document**
- **Data sheet**
- **Silicon characterization report**
- **PHY model**

Applications Support
www.latticesemi.com/support

March 2017
Order #: I0257 Rev. 0