Receiver IP Core Incorporating HDMI® Specification Version 1.4a Features

Supporting features such as 3D over HDMI, HDMI Ethernet Channel, and Audio Return Channel in addition to HDMI 1.3 feature set

Lattice Semiconductor designs, tests and licenses transmitter and receiver IP cores that incorporate features of the HDMI specification version 1.4a. The IP cores support 3D over HDMI, HDMI Ethernet Channel, as well as Audio Return Channel capabilities to offer an enhanced entertainment experience that brings 3D functionality to the home theater and simplifies device connectivity. Lattice is one of the founders of the HDMI standard and operates HDMI Authorized Testing Centers worldwide.

Applications

- 3D Video from Movies, Games and Broadcast
- Digital TV & 3D TV
- A/V Receivers & Home
- Theater
- Deep Color Displays

Key Features

- 1080p/60Hz
- HDMI Ethernet Channel
- Audio Return Channel
- 48-bit Deep Color Video
- 3D over HDMI
- CEC

The HDMI 1.4a specification consolidates the transmission of HD video, audio, data and control into a single cable by enabling high-speed, bidirectional communication through the HDMI cable. Lattice's RX IP core supports both HDMI 1.3 and HDMI 1.4a features, such as HDMI Ethernet Channel and Audio Return Channel.

An HDMI Ethernet Channel-enabled device can send and receive data via 100 Mbps Ethernet over an HDMI cable utilizing the IP core and the customer's own Ethernet transceiver. The Audio Return Channel allows the TV tuner to send audio streams from the TV to an HDMI-attached A/V receiver for audio processing to improve sound quality.

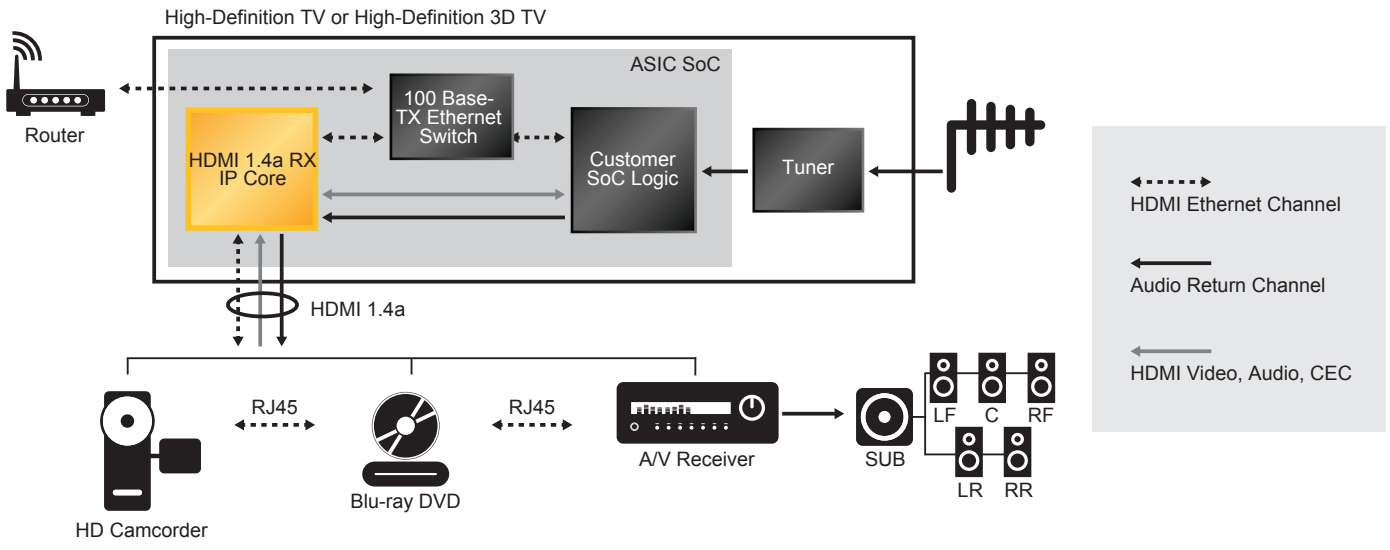
All mandatory and many optional 3D video formats defined in the HDMI 1.4a specification support up to 1080p frame size.

Lattice's RX IP core supports all relevant audio formats, while its colorspace converter allows convenient interfacing with most video interfaces. The Receiver RX IP core is configurable, providing the SoC designer access to multiple internal interfaces and hardware blocks, potentially reducing integration time and gate count. Lattice's ASSPs also include High-bandwidth Digital Content Protection (HDCP).

In addition to market leading HDMI 1.4a features, the IP cores offer key advantages to SoC manufacturers, including reduced bill of materials cost. Lattice's industry leadership and unparalleled expertise helps its IP customers accelerate time-to-market through shorter design cycles and faster compliance testing with the assurance of compatibility with hundreds of millions of HDMI-enabled digital TVs worldwide.

Lattice offers the broadest range of silicon proven TX and RX IP solutions, incorporating HDMI features for use numerous consumer electronics applications.

Receiver Application Incorporating HDMI 1.4a Feature



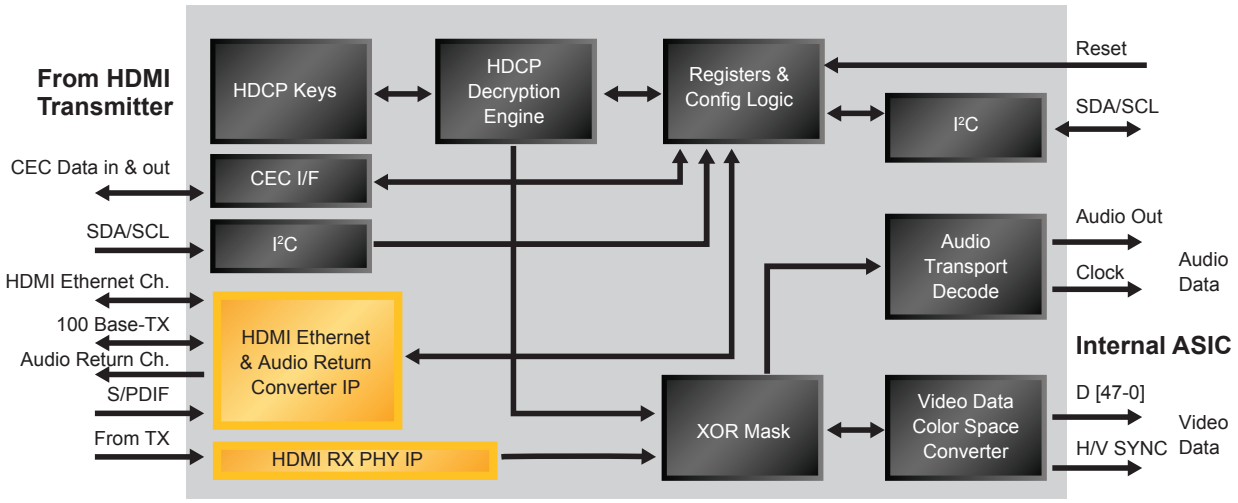
General Features

- **Digital Video Inputs**
  - 24/30/36/48-bit RGB/YCbCr 4:4:4 (Deep Color)
  - x.v.Color
  - 16/20/24-bit YCbCr 4:2:2
  - 8/10/12-bit YCbCr 4:2:2 (ITU 601 and 656)
  - 12/15/18/24-bit DMO (Digital Multimedia Output) RGB/YCbCr 4:4:4
  - Separate and embedded syncs
- **Video Processing**
  - HDMI: Resolutions up to 16-bit 1080p30 and 12-bit 1080p60
  - Color-space conversion
  - Support of all mandatory and many optional HDMI 1.4a 3D video formats up to 1080p
  - 4:2:2-to-4:4:4 and 4:4:4-to-4:2:2 conversion
- **Digital Audio Inputs**
  - Industry standard S/PDIF and I²S output
  - Direct Stream Digital (DSD) for Super Audio CD
  - Dolby® TrueHD and DTS-HD Master Audio™ high bit rate support up to 24Mbit/s
  - 2/8 Channel Dolby Digital®, DTS, DVD-Audio and PCM support up to 192 kHz
  - IEC 60958 and IEC 61937 compatible
- **System Operation**
  - Automatic configuration supported
  - Parallel and Slave I²C I/F, Slave I²C (HDCP)
  - Interrupt pin and registers
  - Monitor detection (hot plug & transmitter detect)
  - HDCP cipher engine decrypts video/audio
  - Programmable Data Enable (DE)
  - CEC (Consumer Electronics Control)
  - Home Network Support and Audio Uplink
  - 100Base-T Ethernet (100Mbps) <=> HDMI Ethernet Channel
  - S/PDIF in => Audio Return Channel
- **Compliance**
  - HDMI 1.1, 1.2, 1.3 and 1.4a
  - HDCP 1.4
  - EIA/CEA-861D
  - DVI 1.0

Deliverables

- **Digital IP Core**
  - Unencrypted, commented RTL
  - Interface to analog TMDS RX PHY and HDMI
  - Ethernet & Audio Return Converter IP Core
  - Development kit and firmware for CEC (option)
- **Analog IP Core**
  - TMDS RX PHY - .lef, .lib, GDSII
  - HDMI Ethernet & Audio Return Converter - .lef, .lib, GDSII
  - LVS Netlist
- **NC-Verilog Test Bench**
  - Test bench
  - I²C verification modules
  - Audio/video stimulus and monitors
  - HDMI transmitter encrypted model
  - Regression test suite
  - Test-invoking scripts
- **Scripts and Documentation**
  - Synopsys synthesis scripts & constraint files
  - Primetime static timing scripts
  - ATPG example scripts
  - Logic-equivalency scripts - RTL2Gates
  - Programming and Integration guidelines
  - Design overview and I/O description
  - Design datasheet

HDMI 1.4a Receiver IP Core Data Flow



Applications Support
www.latticesemi.com/support

March 2017
Order #: I0259 Rev. 0