Consumer Solutions
Your Idea In Our Silicon

Lattice Semiconductor’s low cost and low power FPGAs allow new handsets with new and proprietary ideas and features to be developed without waiting for next-generation chipsets.

Enable Innovative Solutions
Ultra-Low Density FPGAs Enable Differentiation

Ultra-low density FPGAs from Lattice serve as companion chips to standard Application Processors (APs), enabling consumer mobile designers to quickly and easily bring new features and capabilities to market.

- Quickly meet new customer demand
- Stay ahead of the competition
- Create proprietary solutions
- Innovate now!

For New Opportunities
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Eliminating “Sensor Choke” in Smartphones (EBI2 to I²C Bridging)

Too many I²C devices

- Smartphones now have as many as 15 to 20 sensors.
- All are trying to talk to the processor through a slow I²C port.
- This chokes the application processor and kills system performance.

Bridge slow I²C devices to a high-speed bus

- Lattice ultra-low density FPGAs can implement multiple buffered I²C controllers.
- Connect them to the application processor through a high-speed parallel bus, (such as EBI2) and high-speed serial bus (such as SPI).
Smart Sensor Management for Smartphones
(Interrupt Aggregation)

Multiple sensor interrupts slow down smartphone responses

Multi-touch screens can generate very heavy interrupts at a given time.
This tremendously increases processor overhead and potentially affects other tasks.

Interrupt aggregator offloads processor and improves performance

Lattice ultra-low density FPGAs can aggregate multiple sensor interrupts into efficient summaries to offload the processor.
The interface to the processor (red dotted box) can be customized to any available interface such as SPI or a processor local bus’ offering extra flexibility in terms of design integration.
Smart Sensor Management for Smartphones
(Auto-Polling)

Sensor polling increases processor overhead

Some “chatty sensors”, such as gyroscopes, require constant polling from the processor. This is very troublesome for the processor and often prevents the processor from entering into the sleep state.

Offload processor with built-in auto-polling and data filtering

Lattice ultra-low density FPGAs can incorporate auto-polling as a feature to offload the processor. It can further be used to filter out unnecessary data to increase interrupt efficiency.
Sensor Expansion and Management via SLIMbus
(SLIMbus to Multiple I²C Interfaces)

Increasing sensors, but no good way to connect to processor

Smartphones have increasing demand for sensors.
Most of these use slow I²C interfaces.
This creates an application processor I²C bottleneck.

Connect multiple sensors through MIPI-SLIMbus

Lattice ultra-low density FPGAs can implement a SLIMbus to multiple I²C adapters.
This allows the application processor to use the SLIMbus to manage the sensors.
Increasing SPI Performance to Allow Additional SPI Peripherals (SPI Port Expansion)

Many SPI peripherals on single port

Adding additional SPI based peripherals can enrich your product. But what if the SPI port doesn’t have enough performance?

SPI port expansion

Lattice ultra-low density FPGAs can implement a high-speed SPI controller and interface it to your application processor’s high-speed parallel bus.
Enabling “Always-On” Applications in Smartphones
(Always-On Pedometer)

Sensor Management chips are too power hungry

Smartphones now have several sensors.
Sensor management chips consume too much power to be used in “always on” modes - e.g. Pedometer.

Enable “Always-On” applications

Lattice ultra-low density FPGAs can be used to create low power “always-on” solutions using the accelerometer.

Implementation multiple I2C masters to completely isolate low & high power sensors.
Wake up high power sensors only after determining an event using only the low power accelerometer.
Enabling Universal Remote in Smartphones
(Infrared LED Tx / Rx)

Processor can’t support timing critical functions

In multi-tasking operating systems, application processors need to be ready to service interrupts all the time. This makes it challenging to manage tasks that require precision timing control.

Timing Critical Processor Offload

Ultra-Low Density FPGA

Lattice ultra-low density FPGAs can be used to offload timing critical tasks from the Application Processors.
Enabling “E-Commerce” Applications in Smartphones (Barcode Emulation)

LCD Glass too reflective for 1-D barcode readers

1-D barcodes displayed on the LCD screens are not readable by traditional barcode scanners. Reflections from 1-D barcodes can be emulated using a LED. This requires time critical control of LEDs.

In multi-tasking operating systems, it is not efficient for application processors to control LEDs for barcode emulation.

Timing Critical Processor Offload

Lattice ultra-low density FPGAs can be used to offload the timing critical barcode emulation function from the application processor.
Tunable Antenna
(RFFE Bridge)

Processor can’t control tunable IC within a guaranteed response time

Connectivity Processor  \( \rightarrow \)  Tunable Digital Capacitor

How to guarantee the response time?

The tunable IC is controlled via the SPI interface, but the processor can’t guarantee the response time through SPI interface.

Guaranteed response time with flexibility for tuning

Ultra-Low Density FPGA

MDM9290/MSM8960  SPI  Tunable parameters in ROM

MDM9290/MSM8960  RFFE  Tunable Digital Capacitor

Lattice ultra-low density FPGAs can implement the needed parameters using internal block RAM for tunable IC management.

In addition, tunable parameters can be updated in the future when needed.
LVDS panel is serial (LVDS), but processor is parallel (RGB)

Many of the large, high-quality displays popular in today’s tablets use serial LVDS inputs, while most application processors output parallel RGB video.

In addition, tablets often need to connect to external VGA displays such as projectors.

Parallel (RGB) to Serial (LVDS) conversion

Lattice ultra-low density FPGAs can implement a 7:1 SERDES to match the application processor’s parallel video output to the serial video input on the display.

In addition, the Ultra-low density FPGA can downscale the high resolution video to VGA output.
Enabling HDMI Output from Smartphones
(Video Upscaling)

Processor only supports low-resolution

Smartphones can output 720p/1080p have a competitive advantage.
But what if application processors can only output the lower resolutions?

Upscale low resolution to high resolution

Lattice ultra-low density FPGAs can upscale the application processor’s 480p/720p video output to match the HDMI 720p/1080p input.
Enabling TV Output from a Feature Phone

(Video XY Swapping)

Processor can’t support Video XY swapping

Adding an inexpensive TV encoder chip is a fast way to increase the value of your feature phone.

But most TV encoders input the image in landscape mode, while most baseband processors output the image in portrait mode.

XY swapping using an ultra-low density FPGA with external SRAM

Lattice ultra-low density FPGAs can perform an video XY swap on the baseband processor’s video output with an external frame buffer.
720p Wireless Video Streaming from a Smartphone (Image Mirroring and Downscaling)

Processor does not support dual displays

Can’t connect your smartphone to your home TV.
Low-cost application processors only provide one video output. How can you drive your internal display and an external display simultaneously?

Downscale to create two resolutions

The external display’s larger video resolution can be routed to a Lattice ultra-low density FPGA.
The Lattice FPGA can downscale it to match the smaller video resolution of the smartphone.
Allows both displays to be active at the same time.
3D Video and Imaging
(Autostereoscopic 3D Panel Timing Controller)

Processors can’t directly drive autostereoscopic 3D panels

Drive autostereoscopic 3D panel with built-in TCON

Lattice ultra-low density FPGAs implement a 3D panel timing controller and drive to an autostereoscopic.

Directly connects to an autostereoscopic 3D display for handset / mobile based products.
Universal 3D Shutter Glasses
(Customized Pattern Detector for Multiple TVs)

Different TV brands and glasses are often incompatible

Different TV brands and glasses are often incompatible because TV makers define their own IR transmission standard. This creates incompatibility for different glasses and TVs. Users have to abandon their glasses when changing to different TV brands.

Universal shutter glass with pre-defined pattern detection

Lattice ultra-low density FPGAs can implement pattern detection circuits with preloaded patterns to support major TV brands. In addition, IR noise filtering can be added to offer better quality viewing experience.
Managing Differing Video Requirements for Tablets
(Color Space Conversion and Timing Controller)

Processor can’t convert color space

Successful tablets must be able to receive video input from multiple sources and display it on multiple devices. However, this can be challenging for many application processors.

Use an ultra-low density FPGA for color space conversion and display timing control

Lattice ultra-low density FPGAs can implement:
- Color Space Conversion
- Display Timing Controllers
- Image scaling
Dual Camera Video for Smartphones and Tablets
(Displaying Video-in-Video Images)

Processor lacks multi-camera support

Dual cameras are becoming common in smartphones and tablets.

A popular application is to use two cameras to produce a video in video display.

Multi-camera support using an ultra-low density FPGA with external SRAM

Lattice ultra-low density FPGAs can:
  • Convert the camera data to RGB
  • Use an external frame buffer to build the video in video image
  • Interface the video image to the application processor
Enabling Dual Display Cameras
(Image Resolution Conversion)

DSPs only supports one resolution

Many Imaging DSP chips have the capability to drive a display in only one resolution.

Some applications require images to be displayed in multiple LCD screens.

Downscale high resolution to low resolution

Lattice ultra-low density FPGAs can downscale the DSP’s high resolution output to match the low resolution display’s requirement.
Adopting Managed NAND for Mobile Devices (Built-in eMMC Controller)

Incompatible or lacking eMMC controller

- Some processors have no built-in eMMC controller, unable to take advantage of existing managed NANDs.
- Many processors offer eMMC controllers through SDIO ports. However SDIO ports may already be used to connect to other peripherals.

Additional eMMC controller to lower system cost

- Implement an eMMC host controller inside a Lattice ultra-low density FPGA to take advantage of low cost managed NAND.
- An eMMC controller can be customized to a x8 interface for higher performance.
Fast Addition of Wi-Fi or CMMB Modules

(SDIO to High-Speed Parallel Bus Bridge)

Module has two ports, but neither is free

Bridge SD card to AP bus, to free up SD port for Wi-Fi module

A fast way to enhance your product’s feature set is to use readily available modules, such as Wi-Fi or CMMB.

Most of these modules provide SDIO and SPI interfaces.

But what if neither of these interfaces are available?

A Lattice ultra-low density FPGA can implement an SD Host Controller and bridge it to the application processor’s high-speed parallel bus.

This allows the Wi-Fi module to be placed on the SD/SDIO port.

Lattice also provides reference driver code to enable rapid system integration.
Smart Frame Buffer for Notebooks
(Offloads CPU and GPU for Power Optimization)

Power consumption is high during period of inactivity

A manufacturer of ultrabooks wanted to reduce power consumption and increase battery life while still delivering the same performance of the display subsystem. The manufacturer needed a companion chip to manage the outputs of the GPU and CPU while reducing total system power.

Smart Frame Buffer offloads processor and enhances battery life

The Lattice Smart Frame Buffer ultra-low density FPGA solution enables ultrabook / notebook suppliers to increase battery life by shutting down the GPU and or CPU subsystems during periods of inactivity. The smart frame buffer manages and refreshes the display while the power-hungry CPU/GPU subsystem goes into standby.
USB Keyboard Docking for Tablets
(Full Keyboard Docking Solutions)

Designers are searching for Low-cost, flexible keyboard docking

Consumers are demanding a keyboard docking station for tablets offering a notebook-like feel.
Must be low-cost, low-power and customizable.

Implement low-cost, flexible keyboard docking with an ultra-low density FPGA

Lattice ultra-low density FPGAs are ideal for low-cost, low-power, flexible docking solutions.
Based on the USB1.1 interface, Program ROM for the keyboard can be customized to fit designer needs.
Optional touchpad and security algorithm can be implemented to offer extra authentication features and flexibility.
Media Docking for Smartphones
(Image Upscaling and Audio Muxing)

Two audio sources must share one speaker and upscaling one

The speaker is shared between built-in radio and smartphone audio output.

Need to output 720p to TV, but the phone only offers 480p.

Muxing multiple audio sources and upscale to HDMI

Lattice’s media docking solution provides an easy way to connect all the audio and video sources from the media devices (radio/smartphone/tablet) to the external world.

The video scaling portion of the design takes video input source from the media device; upscales it and then sends to the external HDMI connector.

In addition, authentication security algorithms, such as SHA-2 can be implemented to guarantee use of vendor-approved parts.
4G LTE Expansion for Tablets
(Additional USB2.0 Host Controller for LTE Modem)

Processor lacks USB host for LTE modem connection

![Diagram](image)

- Processor's native USB host controllers are already occupied.
- Need additional USB host controller to support latest 4G LTE modem.
- Must guarantee 4G bandwidth of 100 Mbps downlink and 50 Mbps uplink.

USB2.0 host controller for LTE connectivity

![Diagram](image)

- Lattice ultra-low density FPGAs can implement a USB2.0 host controller with high-speed processor interface to connect to a LTE modem.
- The processor interface can be customized to be either a 16-bit or 32-bit bus to boost performance.
- In addition, a DMA engine can be added to give even higher bandwidth.
Adding High-End Headsets to Smartphones
(Nokia ECI Implementation)

Processor does not support high-end audio feature

How to Interface to High End Headsets?

Application Processor

One role of smartphones is to function as a media player. Most media players interface to a high end headset, which includes media control functions. How can this capability be added to a smartphone?

Implement Nokia’s proprietary ECI for superior audio experience

A Lattice ultra-low density FPGA to implement Nokia’s ECI. Nokia’s Enhanced Control Interface (ECI) is similar to Apple’s Earphones with remote and microphone. This lets smartphone designers quickly add a high-end audio device interface.
Dual SIM Phones
(Inter-processor Communication)

How to allow inter-processor communication

One way to implement a dual SIM phone is by using two baseband processors. How can the two processors communicate with each other?

Create an Inter-Processor Communication Unit (IPCU)

Lattice ultra-low density FPGAs can use any available port on either processor for implementing the inter-processor communication unit (IPCU).

Example interfaces for two processor using a pair of SPI slaves.
Dual SIM Phones
(SIM Card Switching)

Single baseband can’t support two SIM cards

Often dual SIM phones are implemented with a single baseband processor. SIM switching logic is required to make it happen.

Implement SIM switching logic to enable dual SIM application

Lattice ultra-low density FPGAs can implement the SIM switching logic allowing one baseband processor to support two SIM interfaces.
High-End Camera Phone with Camera DSP Module
(Multiple Hosts Sharing Same Client)

One client, but two hosts

A high-end camera phone can be built by using an actual camera DSP module.

How does the camera DSP communicate with the application processor?

How do two SD hosts share one SD client?

How are other resources shared between two processors? (e.g., LCD, buttons and touch.)

Mux single client between two hosts

Lattice ultra-low density FPGAs can implement the necessary flags, registers, etc. to enable the inter-processor communication.

In addition, a, ultra-low density FPGA can be used to mux the single resources between two hosts.
Adding High-end Features to Low Cost Phones
(UART Expansion via the SPI Port)

Adding additional features to a low-cost feature phone can make a big impact on your market share.

But the application processors in low cost phones usually have limited interfacing capacity.

Lattice ultra-low density FPGAs can implement multiple UART controllers and interface them to the application processor’s high-speed SPI port.
Processors have implemented SLIMbus to replace traditional audio interfaces like I²S inside the handset. However, the audio codecs are slow in adopting the SLIMbus interface, causing an interface mismatch.

Lattice ultra-low density FPGAs can implement a SLIMbus to I²S to solve this interface mismatch problem.

Reversely, an I²S to SLIMbus host controller can be implemented to support the connectivity processor (such as MDM9200) with the SLIMbus interface to hook up to the AP supports only I²S.
MIPI-BIF (Battery Interface) for Smartphones (Accelerates Smart Battery Adoption)

Can't connect to smart batteries using MIPI-BIF interface

A smart battery interface with security features can offer strong protection against the use of counterfeit batteries, providing a safer solution for end users. However, most existing mobile processors don’t support the MIPI-BIF smart battery interface.

Implement MIPI-BIF for smart battery connectivity

Lattice ultra-low density FPGAs can implement a complete MIPI-BIF host controller to interface to smart batteries. This allows the mobile developer to adopting the latest battery interface standard using their existing applications processor.
Multiprocessor systems

(Custom Interface for Inter-processor Communication)

Sharing critical parameters between two processors

Dual port RAMs are popular in multiprocessor systems where data needs to be shared between two processors.

However, DPRAMs require high number of I/Os and are not ideal for space constrained applications.

Custom inter-processor communication unit

Lattice ultra-low density FPGAs can used to implement I/O optimized custom interfaces to share critical parameters between two processors.

Lattice ultra low density FPGAs are offered in several small packages that meet the requirements of space constrained applications such as Smartphones.
## Mobile Application Targeted IP

### Connectivity
- 1-to-4 UART Expander
- CMOS Camera Interface
- PWM (16x3)
- I2C Master / Slave Controller
- SPI Master / Slave Controller
- USB 2.0 Host Controller
- USB 2.0 Device Controller
- USB 2.0 OTG Controller
- USB 2.0 Hub Controller
- I2C Master / Slave Controller
- PCI Master / Target Controller

### Sensor Management
- I2C Master Controller
- SPI Master Controller
- SLIMbus Client Controller
- UART
- Expansion Memory Interface
- Touchscreen Controller
- PWM (16x3)
- Keypad Scanner
- IrDA Fast Tx/Rx

### Memory and Storage
- Cellular RAM Controller
- MDDR Controller
- CF+Controller
- MS Pro Interface
- NAND Flash Interface
- SLC2MLC Interface
- MMC Host Controller
- SD Host Controller
- SDIO Host Controller
- MMC Client – MMC Mode Using FPGA RAMs as Memory
- SD Client – SD Mode Using NAND Flash as Memory
- NOR Flash Controller
- Flash Controller with Wear Leveling
- LPC Bus Controller
- DDR/DDR2/LPDDR Memory Controllers
- SDRAM Controller

### Video and Imaging
- Dual Display Controller
- Graphics LCD Controller
- LCD Controller (16x2 Character)
- Touch Screen Controller
- XGA to WVGA LANCZOS2 Scaler
- XGA to WVGA Nearest Neighborhood Scaler
- RGB565 to YCbCr 8bit (Color Space Conversion)
- RGB666 to YCbCr 8bit (Color Space Conversion)
- RGB888 to YCbCr 8bit (Color Space Conversion)
- YCbCr 10bit to RGB666 (Color Space Conversion)
- YCbCr 10bit to RGB888 (Color Space Conversion)
- YCbCr 8bit to RGB666 (Color Space Conversion)
- YCbCr 8bit to RGB888 (Color Space Conversion)
- YCbCr 10bit to RGB666 (Color Space Conversion)
- YCbCr 10bit to RGB888 (Color Space Conversion)
- YCbCr 8bit to RGB666 (Color Space Conversion)
- YCbCr 8bit to RGB888 (Color Space Conversion)
- YCbCr 10bit to RGB666 (Color Space Conversion)
- I2C Based Video Switching
- Image Blending – Multiple Images and Text Overlay
- Image Enhancements – Brightness and Contrast Controller
- LVDS Transmitter/Receiver
- LVDS Serializer/De-Serializer
- DVI Receiver Controller
- MIPI DSI Receiver / Transmitter Controller
- MIPI CSI-2 Receiver / Transmitter Controller
- Dual-LVDS Transmitter (after LVDS Serializer)

### Other
- Sigma-Delta ADC
- Mico8 Microcontroller
- LED/OLED Driver
- Power Management Bus Controller
- CRC (Cyclic Redundancy Checker)
- AES Encryption / Decryption
- RC4-based pseudo-random sequence generator
- MIPI Battery Interface (BIF)
Design Services

In addition to the Application Examples, Lattice offers a wide range of IP focusing in the areas of Sensor Management, Video and Imaging, Memory and Storage, and Connectivity. Lattice also offers custom design services.
## Device Selection Guide

### iCE40

<table>
<thead>
<tr>
<th>Feature</th>
<th>LP384</th>
<th>LP1K</th>
<th>LP4K</th>
<th>LP8K</th>
<th>HX1K</th>
<th>HX4K</th>
<th>HX8K</th>
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<td>128K</td>
<td>64K</td>
<td>80K</td>
<td>128K</td>
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<td>Phase-Locked Loops</td>
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<td>2</td>
<td>1</td>
<td>2</td>
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<td>Core icc @ 0KHz</td>
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<td>100µA</td>
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### MachXO2

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<th>256</th>
<th>640/U</th>
<th>1200/U</th>
<th>2000/U</th>
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<td>Memory Standards</td>
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### Package

<table>
<thead>
<tr>
<th>Package</th>
<th>Programmable I/O: Max I/O (LVDS Channels)</th>
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<tbody>
<tr>
<td>25-ball WLCSP (2.5 x 2.5 mm)³</td>
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<tr>
<td>32-pin QFN (5 x 5 mm)</td>
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</tr>
<tr>
<td>36-ball ucBGA (2.5 x 2.5 mm)</td>
<td>25 (3)</td>
</tr>
<tr>
<td>49-ball ucBGA (3 x 3 mm)</td>
<td>37 (6)</td>
</tr>
<tr>
<td>64-ball ucBGA (4 x 4 mm)</td>
<td>55 (3)</td>
</tr>
<tr>
<td>81-ball ucBGA (4 x 4 mm)</td>
<td>62 (8)</td>
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<tr>
<td>84-pin QFN³ (7 x 7 mm)</td>
<td>67 (7)</td>
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<tr>
<td>100-pin TQFP/VQFP (14 x 14 mm)</td>
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<td>121-ball ucBGA (5 x 5 mm)</td>
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<tr>
<td>121-ball csBGA (6 x 6 mm)</td>
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<tr>
<td>144-pin TQFP (20 x 20 mm)</td>
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<td>184-ball csBGA (8 x 8 mm)⁴</td>
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<td>225-ball ucBGA (7 x 7 mm)</td>
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<tr>
<td>256-ball fbBGA (17 x 17 mm)</td>
<td>206 (4)</td>
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<tr>
<td>332-ball csBGA (17 x 17 mm)</td>
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<tr>
<td>484-ball fpBGA (23 x 23 mm)</td>
<td>278 (4)</td>
</tr>
</tbody>
</table>

1. MachXO2 (ZE option) measured at 1.2V Vcc
2. No PLL available in this package
3. Only 1 PLL available
4. Ultra high I/O count devices are supported for XO2-HC/HE options
5. WLCSP package available for ZE option only
6. Contact Lattice sales representative regarding this package, available for HE option only
Packages Designed for Mobile Applications

iCE40 Packages

- **84 QFNS**: 0.5 mm pitch, 7X7 mm
- **225 ucBGA**: 0.4 mm pitch, 7X7 mm
- **121 csBGA**: 0.5 mm pitch, 6X6 mm
- **81 csBGA**: 0.5 mm pitch, 5X5 mm
- **32 QFN**: 0.5 mm pitch, 5X5 mm
- **121 ucBGA**: 0.4 mm pitch, 5X5 mm
- **81 ucBGA**: 0.4 mm pitch, 4X4 mm
- **49 ucBGA**: 0.4 mm pitch, 3 X 3 mm
- **36 ucBGA**: 0.4 mm pitch, 2.5 X 2.5 mm

MachXO2 Packages

- **484 fpBGA**: 1.0 mm pitch, 23x23 mm
- **144 TQFP**: 0.5 mm pitch, 20x20 mm
- **100 VQFP**: 0.5 mm pitch, 14x14 mm
- **256 caBGA**: 0.8 mm pitch, 14x14 mm
- **132 csBGA**: 0.5 mm pitch, 8x8 mm
- **225 ucBGA**: 0.4 mm pitch, 7X7 mm
- **484 fpBGA**: 1.0 mm pitch, 23x23 mm