LEARN HOW TO:
» Reduce Power Management Costs
» Increase System Reliability
» Reduce the Risk of Circuit Board Respins
Power 2 You

A Guide to Power Supply Management and Control

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Introduction

1.1 Power 2 You

This book provides technical details and design considerations for implementing the common circuit board power management functions shown as 3-D blocks in Figure 1-1 and Figure 1-2. This book also provides generalized cost effective solutions for each of these functions that can be customized to meet a circuit board’s specific voltage, current and control environment.

For readers viewing this document in .pdf format, the 3-D blocks in Figure 1-1 and Figure 1-2 are hyperlinked to the appropriate section of Chapter 2, where multiple circuit options are provided for that particular power management function. Each of the circuit options hyperlink to a detailed description in the relevant chapters.

If you are already familiar with Lattice Semiconductor Power Manager II devices and need to find a solution for a power management function:

1. Click on the required power management block in Figure 1-1.
2. You will automatically navigate to the section of Chapter 2 that provides multiple circuit options for the selected power management function.
3. Click on the relevant circuit option.
4. You will automatically navigate to the detailed description of that circuit diagram.

If you wish to read about the general board power management blocks, the design criteria and circuit options, read this chapter. After reading this chapter, you can skip Chapter 2 - “Solutions Summary” on page 2-1 and continue with Chapter 3 - “Reset Generators & Supervisors” on page 3-1.

What is Power Management?

Every circuit board is powered from one or more sources called the input, or primary, power supplies. And, every circuit board performs one or more functions using a number of ICs, such as ASICs, CPUs, FPGAs, and so on. These ICs are called the payload ICs. The circuit board generates multiple power rails from the input supplies to power these payload ICs, using board
mounted supplies called primary and secondary supplies. The term ‘Power Management’ in this book includes all power rail control functions implemented in a circuit board. Typically, input power rails are controlled by power management functions such as hot-swap control and redundant power rail control. On the payload side, power management functions include sequencing, monitoring, supervisory signal generation, trimming and margining.

**Typical Board Power Supply Architectures**

Circuit boards can be broadly classified into two types:

1. Boards that derive input power supply from a backplane with its power always on and the boards plugged into or extracted from the backplane without turning the power off – these are called hot-swappable boards, shown in Figure 1-1.

2. Boards that derive power from an external power supply that is turned on after the board is connected and is turned off before the board is disconnected – these are called non hot-swappable boards.

There are solutions to implement all of the critical power supply control functions. Advanced power supply designers can click on any of the hyperlinked functions to see the solution. To learn the background of all these functions, continue reading this chapter.

*Figure 1-1. Power Management in a Hot-Swappable Circuit Board. (If viewing this document in .pdf format, click on any of the 3-D blocks to jump to implementation details.)*

Figure 1-1 illustrates the power supply architecture of a circuit board with the common power management blocks shown in 3-D. A hot-swappable board derives its power from one or more supplies from the backplane. There can be more than one set of supplies sourced from the backplane, so these boards are operational even when one of the supplies fails. The backplane supplies in Figure 1-1 are also called the primary supplies.

In systems that require high availability, such as telecom / datacom systems, backplanes provide redundant supplies called on-line and standby power. The **Power Supply OR’ing Controller, also called the redundant power supply controller**, selects between the online and standby supplies to derive the power to the board. (Refer to “2.4 Redundant Supply Management” on page 2-14.)

In order to extract and reinsert the boards from the backplane without disturbing the other boards plugged into the same backplane, a **hot-swap controller** function is implemented on each of these circuit boards.
Introduction

In some cases, the supply rail output from the hot-swap controller feeds one or more DC-DC converters, shown in Figure 1-1 as ‘DC-DC Primary’ supplies. Primary supplies are used to derive one or more main payload supply rails, which are also called secondary supply rails and are shown in Figure 1-1 as the ‘DC-DC Secondary’ supplies. These secondary supplies may have to be sequenced either through the DC-DC converter enable signals or through MOSFETs. Sequencing of these supplies is controlled by the sequence controller. After all supplies are sequenced, the reset generator starts the board’s normal operation by releasing the reset signal to the CPU. In addition, monitoring these lower voltages for faults should take into consideration, and compensate for, other error sources such as the ground voltage difference between the supply and the monitoring device. For example, the fault level of 1.2V is 1.2V * 5% = ±60mV. The ground voltage difference between different points in the circuit board can be as much as 20mV to 30mV. To compensate for the error, differential sensing, as shown in Figure 3-9 on page 9, is used.

Modern ICs require lower core voltages (1.2V or lower) with high current capacity (10A or higher) with reduced voltage tolerance. To meet these stringent supply requirements, a power supply trimming controller is often required. For quality assurance purposes, four-corner testing of boards (voltage and temperature) frequently requires margining of supplies. These boards use margining controllers. In some applications, such as GSM basestation boards, microwave boards and boards supporting hot-pluggable mezzanine cards, it may be necessary to power an external unit, such as a remote radio head or an outdoor antenna, or supply power to an AMC. To support these functions, the power feed controller is required.

Figure 1-2 shows the power management requirements in a non hot-swappable circuit board. These boards require primary and secondary power management controllers, as shown in Figure 1-2. The only primary power management function that is not relevant in these non-hot-swappable boards is the hot-swap controller. Systems that typically require non-hot-swappable boards include routers in “pizza-box” form factor, personal computers and medical ultrasound systems.
Typical Power Management Implementations and Their Drawbacks

The power rails in a board currently are managed by simple, single function integrated circuits (ICs) on both the primary and secondary sides. On the input side, each function shown in Figure 1-1 requires different ICs, depending on the rail voltage, board power and other control specifications.

Modern circuit boards with complex payload ICs typically require five or more secondary power rails. Monitoring, sequencing and the generation of resets in these boards require multiple single function ICs.

Together, the power management section requires multiple types of single function power management ICs in a given system. This results in a larger bill of materials (BOM), higher cost of inventory and assembly, as well as reduced reliability.

The cost of the power management portion in a circuit board increases with the number of rails, and the number of power management functions. Lower cost single function power management ICs are usually less accurate in monitoring for faults, resulting in reduced board reliability.

In order to reduce the number of secondary power management ICs, some designs use microcontrollers with an Analog-to-Digital (ADC) converter to monitor power supplies and use software to adapt to board-specific requirements. These microcontrollers are too slow to respond to power supply faults (5 to 10ms) and are unreliable, as they use hundreds of lines of code to perform power management functions and require a watchdog timer to monitor software flow. Microcontrollers are also used because the changes to power management can be met simply by changing software, as opposed to modifying the circuit board layout. However, modifications to software are almost always avoided, as most companies have strict control over software releases.

The ideal power management solution is the one that has the following characteristics:

1. Lower cost and reduced bill of material, and flexibility to meet individual board power management needs.
2. Increased board reliability through increased supply fault monitoring accuracy.
3. Reduced risk of circuit board re-layout to board power management through programmability.

This book details how a Lattice Power Manager II device can integrate all of these functions. Because these devices are in-system programmable, each device can be programmed to meet a wide variety of circuit board functions.

1.2 Lattice Power Manager II IC Family

There are five members in the Power Manager II family of devices: ispPAC®-POWR1220AT8, ispPAC-POWR1014A, ispPAC-POWR1014, ispPAC-POWR607 and ProcessorPM™-POWR605.

Figure 1-3 shows the part numbering convention of the Lattice Power Manager II product family.

**Figure 1-3. Lattice Power Manager II Family Part Numbers Indicate I/O Resources**

![Part Number Diagram]

While the largest device, the ispPAC-POWR1220AT8, can be used to implement complex power management functions, the smallest device, the ProcessorPM-POWR605, can be used to implement power management functions for a wide variety of microprocessors and DSPs. All Power Manager II devices can be programmed in-system through the JTAG interface. The power management algorithm can be designed using the PAC-Designer® software tool that can be downloaded from the Lattice website free of charge.

Figure 1-4 shows the architecture of the largest member of the family, the ispPAC-POWR1220AT8.

**Figure 1-4. ispPAC-POWR1220AT8 Device Block Diagram**

![Device Block Diagram]

This device can manage up to 12 supply rails and generate 20 outputs (including four programmable MOSFET drive outputs) using its on-chip 48-macrocell ruggedized CPLD. All supply voltages can be measured using the on-chip 10-bit ADC device via the I²C interface. This device also supports trimming and margining of up to eight DC-DC converters. Various time delays used in the power management algorithm can be realized by four on-chip programmable hardware timers.

The ispPAC-POWR1220AT8 device can integrate the following power management functions:

- Power supply OR’ing
- Positive rail power feed to external system
- Hot-swap controller for positive voltage rail
- Sequencing
- Voltage and current monitoring
- Reset generation
- Trimming and margining
- Watchdog timer

Figure 1-5 is a block diagram of the next members of the Lattice Power Manager II family, the ispPAC-POWR1014 and ispPAC-POWR1014A.

Figure 1-5. Block Diagram of ispPAC-POWR1014 & ispPAC-POWR1014A Devices

These devices can monitor up to 10 supply rails and generate 14 power management control outputs (including two programmable MOSFET drivers) using an on-chip 24-macrocell PLD block. The ispPAC-POWR1014A device provides a 10-bit ADC and an I²C interface to measure all supply voltages. Various time delays used in the power management algorithm can be realized by four on-chip programmable hardware timers.

The ispPAC-POWR1014/A devices can integrate the following power management functions:
Introduction

- Power Supply OR’ing
- Hot-swap controller for positive voltage rail
- Positive or negative power feed controller
- Sequencing
- Voltage and current monitoring
- Reset generation, sequencing
- Watchdog timer

The ispPAC-POWR607 device shown in Figure 1-6 can monitor up to six supplies and supports seven outputs (including two MOSFET drivers) that are controlled by the on-chip 16-macrocell PLD. Various time delays used in the power management algorithm can be realized by four on-chip programmable hardware timers.

**Figure 1-6. Block Diagram of an ispPAC-POWR607 Device**

This device can be powered down using a digital signal. The ispPAC-POWR607 device can be used for the following functions:

- Power Supply OR’ing
- Hot-swap controller for positive voltage rail
- Hot-swap controller for negative voltage rail
- Positive or negative power feed controller sequencing
- Reset generation
- Watchdog timer

**Figure 1-7** shows the ProcessorPM-POWR605 device, which is ideal for implementing power management functions for any processor or DSP. This device can monitor up to six supplies and generate five outputs that are controlled by the on-chip 16-macrocell PLD. Various time delays used in the power management algorithm can be realized by four on-chip programmable hardware timers.
The ProcessorPM-POWR605 device can be used to integrate the following functions:

- Voltage supervision
- Reset generation
- Watchdog timer

### 1.3 PAC-Designer Software

Board-specific power management is implemented using the PAC-Designer software: an intuitive, user-friendly software tool set. The PAC-Designer software enables the following:

1. Configure voltage monitoring thresholds for a given voltage rail.
2. Configure MOSFET driver characteristics to meet turn on and off ramp rates.
3. Implement power management functions such as hot-swap controller, sequencer, reset generator through LogiBuilder (simple configurable sequencer steps and logic equations).
4. Simulate the power management algorithm using either high-end tools such as Aldec® Active-HDL™ or Mentor Graphics® ModelSim™, or use the waveform simulator built into the software.
5. Calculate the resistor values to be connected between the Power Manager II devices and the DC-DC converters for implementing Trimming and Margining functions.
6. Generate JEDEC files and SVF files for programming the device using standard programming methods.

### 1.4 Summary of Chapters

This book has nine chapters. Chapter 3 to Chapter 8 each cover a power management function in detail.

Chapter 1 - “Introduction” on page 1-1 – summarizes the power management functions, explains drawbacks of traditional power management solutions, and provides a brief introduction to Lattice Power Manager II products.
Chapter 2 - “Solutions Summary” on page 2-1 – is a summary of all of the solutions provided for each of the power management functions shown in Figure 1-1.

Chapter 3 - “Reset Generators & Supervisors” on page 3-1 – describes reset generator supervisor and watchdog timer and identifies some of the common pitfalls to avoid in voltage supervision and reset generation in circuit boards with multiple power supplies.

Chapter 4 - “Power Supply Sequencing” on page 4-1 – shows how a flexible power supply sequencing arrangement provides a solution. This section also describes software-based sequencing methodology.

Chapter 5 - “Hot-Swap Controllers” on page 5-1 – describes design considerations for implementing hot-swap controllers and selecting MOSFETs. This chapter also provides hot-swap controller solutions for positive rail, negative rail, and multiple backplane rails.

Chapter 6 - “Power Supply OR’ing Controllers” on page 6-1 – describes the design considerations and provides N-rail positive and negative rail OR’ing solutions.

Chapter 7 - “Power Feed Controllers” on page 7-1 – provides design considerations for implementing power feed controllers and selecting MOSFETs. N-supply positive and negative rail power feed, and MicroTCA power module design, are also discussed.

Chapter 8 - “Margining and Trimming” on page 8-1 – describes the need for trimming and margining of supplies, provides trimming and margining solutions, and describes how to implement these designs using software.

Chapter 9 - “Design Tools for Power Manager II” on page 9-1 – describes the software flow, provides a description of each of the steps, and describes software implementation of complex power management designs.
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Solutions Summary

2.1 N-Supply Supervisor, Reset Generator and Watchdog Timer

Features of Supervisor, Reset Generator and Watchdog Timer in a Power Manager II Device

- Monitors up to 12 rails for over-voltage / under-voltage faults
- Precision (0.2% typ.) programmable monitoring threshold from 0.67V to 5.8V
- Differential voltage sensing for monitoring low voltage, high current supplies
- Fast fault detection with glitch filtering – up to 64μs
- Reset generation with programmable pulse stretch of up to hundreds of milliseconds
- Low voltage interrupt generation
- Manual reset input with programmable de-bounce period
- Watchdog timer with programmable time delay from hundreds of milliseconds to minutes
- Flexible watchdog timer interrupt / reset signal combinations
- All features can be changed after assembly through in-system programming
- Over-voltage protection and under-voltage lock-out
- Integrates additional functions such as sequencing, hot-swap, trimming and margining
- Measures voltage and current through I2C. (A detailed circuit description of a design using ProcessorPM-POWR605 device is provided in “3.2 N-Supply Supervisor, Reset Generator and Watchdog Timer” on page 3-10.)
**Figure 2-1. ProcessorPM-POWR605 Integrating 6-Supply Supervisor, Reset Generator and Watchdog Timer**

Advantages of Supervisor, Reset Generator and Watchdog Timer in a Power Manager II Device

- Lowers cost compared to multiple supervisor and reset ICs
- Reduces number of components – No resistors to set threshold, no capacitors to set time delay
- Increases functional reliability – Very fast fault detection, higher monitoring precision, fewer components
- Reduces spurious supply fault interrupts due to supervisor monitoring threshold accuracy and filtering supply glitches
- Reduces risk – Accommodates changes to specs through programmability
- Reduces part types – Single chip can be used across a wide range of applications
- Protects board against over-voltage faults by initiating shut-down. (A detailed circuit description of a design using ProcessorPM-POWR605 device is provided in “3.2 N-Supply Supervisor, Reset Generator and Watchdog Timer” on page 3-10.)
2.2 Power Supply Sequencing

Flexible N-Supply Sequencing

Features of Sequencer Implementation in a Power Manager II Device

- Programmable power up and power down sequencing
- Shutdown can be initiated through supply fault or an external input
- Allows user to change supply turn-on sequence or fine-tune sequence timing in software
- Supports multiple types of supply turn-on/off sequencing algorithms
- Closed loop sequencing / time-based open loop sequencing / complete sequencing within a given period
- Integrates additional functions such as supervision reset generation, watchdog timer, hot-swap, trimming and margining
- Measures voltage and current through through I²C
- Sequencing of supplies can be changed after assembly through in-system programming through JTAG. (A detailed circuit description is provided in “4.2 Flexible N-Supply Sequencing Using Power Manager II II Devices” on page 4-3.)

Figure 2-2. Flexible N-Supply Sequencing Using the ispPAC-POWR1014A Device

Advantages of Integrating Sequencer into a Power Manager II Device

- Reduces cost by integrating the sequencing function along with other board power management functions
- Minimizes the risk of board re-spin due to change of sequencing algorithm – Can adjust sequencing
algorithm after board assembly
• Reduces first prototype board bring-up time – By providing additional debug flags such as sequence incomplete, supply turn-on timeout, etc.
• Increases board reliability by reducing the number of components – Does not require resistors or capacitors for timing or sequencing threshold adjustment
• Reduces the number of ICs required for power management, including sequencing, by meeting the sequencing requirements of a wide variety of boards. (A detailed circuit description is provided in “4.2 Flexible N-Supply Sequencing Using Power Manager II II Devices” on page 4-3.)

Sequencing with MOSFETs and DC-DC Enables

Features of Sequencer Implementation in a Power Manager II Device
• Integrates multiple charge pumps to control high-side N-Channel MOSFETs
• Has unified sequencing algorithm using MOSFETs and DC-DC converter enables
• Programmable power-up and power-down sequencing
• Shutdown can be initiated through supply fault or an external input
• Allows user to change supply turn-on sequence or fine-tune sequence timing in software
• Supports multiple types of supply turn-on/off sequencing algorithms:
  • Closed loop sequencing / time-based open-loop sequencing / complete sequencing within a given period
  • Integrates additional functions such as supervision reset generation, watchdog timer, hot-swap, trimming and margining
• Sequencing of supplies can be changed after assembly through in-system programming via JTAG
• Measures voltage and current through I²C. (A detailed circuit description is provided in “4.3 Sequencing With MOSFETs and DC-DC Converter Enables” on page 4-9.)
Advantages of Integrating Sequencer into a Power Manager II Device

- Lowers cost by reducing the number of DC-DC converters as well as integrating sequencing function along with other board power management functions
- Minimizes the risk of board re-spin due to change of sequencing algorithm – Adjust sequencing algorithm after board assembly
- Reduces board bring-up time by providing additional debug flags such as sequence incomplete and supply turn-on timeout
- Increases board reliability by reducing the number of components – Does not require resistors or capacitors for timing or sequencing threshold adjustment
- Reduces the number of ICs required for power management, including sequencing by meeting the sequencing requirements of a wide variety of boards. (A detailed circuit description is provided in “4.3 Sequencing With MOSFETs and DC-DC Converter Enables” on page 4-9.)
2.3 Hot-Swap Controllers

Hot-Swap Controller Using Soft-Start Mechanism

Features of Hot-Swap Controller Implementation in a Power Manager II Device

- Allows safe insertion into backplane – Programmable contact de-bounce delay
- Over-voltage protection and under-voltage lockout
- Controls inrush current through programmable soft-start rate feature
- Retry on fault with programmable retry period
- Backplane voltage status flag to secondary side
- Isolates board from backplane due to faults on board. Ramp time can be customized to meet board turn-on power requirements.
- Backplane voltage range 3V to 5V
- Integrate other board management functions such as sequencing, reset generation, supervision, watchdog timer, trimming and margining
- Measure backplane voltage in addition to other board voltages and currents through I2C
- Management of supplies can be changed after assembly through in-system programming via JTAG
- Hot-swap controller can be programmed independently of other ICs on the board. (A detailed circuit description is provided in “5.2 Implementing a Positive Supply Hot-Swap Controller Using Power Manager II Devices” on page 5-2.)

Figure 2-4. Hot-Swap Control Implemented Through MOSFET Ramp Rate Control

Advantages of Integrating Hot-Swap Controller into a Power Manager II Device

- Lowers cost by integrating other board management functions and reducing the number of power management ICs
- Minimizes fault propagation to other boards in the system due to a fault on a circuit board
- Increases shut-down reliability – Ensures safe board shutdown through early warning to the secondary side
• Reduces the number of power management ICs – Integrates the remaining power management functions into the Power Manager II devices. (A detailed circuit description is provided in “5.2 Implementing a Positive Supply Hot-Swap Controller Using Power Manager II Devices” on page 5-2.)

Hot-Swap Controller with Hysteretic Current Limit Mechanism

Features of Hot-Swap Controller Implementation in a Power Manager II Device

• Limits the backplane current to a value during a current inrush event, minimizing power supply dip on the backplane
• Two programmable over-current limits: hot-swap event and board operation
• Programmable contact de-bounce delay
• Over-voltage, over-current protection and under-voltage lockout
• Short circuit protection response < 1μs
• Programmable retry period
• Retry on hot-swap fault / secondary supply fault
• Early warning about the backplane voltage status to secondary side
• Isolates board from backplane due to faults on board
• Integrates other board management functions such as sequencing, reset generation, supervision, watchdog timer, trimming and margining
• Measures backplane voltage in addition to other board voltages and currents through I2C
• Management of supplies can be changed after assembly through in-system programming via JTAG
• Hot-swap controller can be programmed independently of other ICs on the board. (A detailed circuit description is provided in “5.2 Implementing a Positive Supply Hot-Swap Controller Using Power Manager II Devices” on page 5-2.)

Figure 2-5. Hot-Swap Controller with Hysteretic Current Limit
Advantages of Hot-Swap Controller Integrated into a Power Manager II Device

- Reduces board cost by integrating other secondary board power management functions into Power Manager II
- Reduces board space taken up by the hot-swap controller by using a smaller hold-off capacitor
- Increases system reliability by reducing the peak current during the hot-swap event and during board fault
- Minimizes fault propagation to other boards in the system due to a fault on a circuit board
- Increases shut-down reliability – Ensures safe board shutdown through early warning to the secondary side
- Reduces the number of power management ICs – Integrates the remaining power management functions into the Power Manager II device. (A detailed circuit description is provided in “5.2 Implementing a Positive Supply Hot-Swap Controller Using Power Manager II Devices” on page 5-2.)

12V/24V Hot-Swap Controller

Features of Hot-Swap Controller Integrated into a Power Manager II Device

- Wide operating voltage range – 6V to 24V
- Can be used across a wide range of board power – 10W to 200W
- Limit the backplane current to a value during current inrush event to meet the safe operating area (SOA) specifications of a MOSFET
- Programmable inrush and operating over-current limits independently
- Programmable contact de-bounce delay
- Over-voltage, over-current protection and under-voltage lockout
- Short circuit protection response < 1μs
- Programmable retry period
- Retry on hot-swap fault/ secondary supply fault
- Backplane fault early warning
- Isolates board from backplane due to faults on board
- Integrates other board management functions such as sequencing, reset generation, supervision, watchdog timer, trimming and margining.
- Measures backplane voltage in addition to other board voltages and currents through I²C
- Management of supplies can be changed after assembly through in-system programming via JTAG
- Hot-swap controller can be programmed independently of other ICs on the board. (A detailed circuit description is provided in “5.2 Implementing a Positive Supply Hot-Swap Controller Using Power Manager II Devices” on page 5-2.)
Advantages of Hot-Swap Controller Integrated Into a Power Manager II Device

• Reduces board cost by integrating other secondary board power management functions into Power Manager II, lower cost MOSFET and smaller hold-off capacitor

• Reduces board space due to smaller hold-off capacitor

• Increases system reliability by reducing the peak current during the hot-swap event as during board fault

• Minimizes fault propagation to other boards in the system due to a fault on a circuit board

• Increases shut-down reliability – Ensures safe board shutdown through early warning to the secondary side

• Reduces the number of power management ICs – Integrates the remaining power management functions into the Power Manager II device. (A detailed circuit description is provided in “5.2 Implementing a Positive Supply Hot-Swap Controller Using Power Manager II Devices” on page 5-2.)

Negative Supply Hot-Swap Controller

Features of the Negative Supply Hot-Swap Controller Implementation

• Wide operating voltage range: -35V to -80V

• Supports wide range of board power: 10W to 200W

• Deterministic current level during hot-swap to meet the SOA specifications of a MOSFET

• Programmable inrush current limit

• Programmable over-current limit

• Short circuit protection response time < 1µs
• Programmable contact de-bounce delay
• Over-voltage protection and under-voltage lockout
• Enables load after the hot-swap event, further minimizing inrush current
• Programmable retry period
• Control of hot-swap from the secondary side.
• Early fault warning to secondary side
• Immune to 100V glitches. (A detailed circuit description is provided in “5.3 Implementing a Negative Supply Hot-Swap Controller” on page 5-13.)

**Figure 2-7. Hot-Swap Controller Circuit Using an ispPAC-POWR607 Device**

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### Advantages of Hot-Swap Controller Integrated into a Power Manager II Device

Increases system reliability by:

- Limiting inrush current to the programmed value
- Limiting current due to secondary side faults to the programmed value
- Reducing current glitches on the backplane
- Reducing power stress on the MOSFET
- Minimizes fault propagation through the system from a faulty card
- Reducing overall system cost
• Reducing board space due to smaller hold-off capacitor
• Reducing the number of hot-swap controller types across multiple projects. (A detailed circuit description is provided in “5.3 Implementing a Negative Supply Hot-Swap Controller” on page 5-13.)

CompactPCI Board Management

Features of CompactPCI Board Management Controller Integrated into a Power Manager II Device

• Hot-swap for 3.3V, 5V, ±12V (CompactPCI hot-swap and board controller)
• Can be used across a wide range of board power – 10W to 200W
• Programmable inrush current per individual rail
• Programmable contact de-bounce delay on all supply inputs
• Over-voltage, over-current protection and under-voltage lockout
• Short circuit protection response < 1μs
• Programmable retry period – Retry on hot-swap fault / secondary supply fault
• Backplane fault early warning
• Isolates board from backplane due to faults on board
• Integrate other board management functions such as sequencing, reset generation, supervision, watchdog timer, trimming and margining.
• Measures backplane voltages in addition to other board voltages and currents through I²C
• Management of supplies can be changed after assembly through in-system programming via JTAG. (A detailed circuit description is provided in “5.4 CompactPCI Board Management” on page 5-16.)
Figure 2-8. An *ispPAC-POWR1220AT8* Device – Complete CompactPCI Board Management

Advantages of CompactPCI Board Management Integrated into a Power Manager II Device

- Reduces board cost by integrating other secondary board power management functions into Power Manager II, lower cost MOSFET and smaller hold-off capacitor
- Increases system reliability by reducing the peak current during the hot-swap event as well as during board fault
- Minimizes fault propagation to other boards in the system due to a fault on a circuit board
- Increases shut-down reliability – Ensures safe board shutdown through early warning to the secondary side
- Reduces the number of power management ICs – Integrates the remaining power management functions into the Power Manager II device. (A detailed circuit description is provided in “5.4 CompactPCI Board Management” on page 5-16.)

CompactPCI Express Board Management

Advantages of CompactPCI Express Board Management

- Hot-swap for 3.3V, 5V, +12V (CompactPCI Express, VME system board controller)
- Can be used across a wide range of board power – 10W to 200W
- Programmable inrush current per individual rail
- Programmable contact de-bounce delay on all supply inputs
• Over-voltage, over-current protection and under-voltage lockout
• Short circuit protection response $< 1\mu s$
• Programmable retry period – Retry on hot-swap fault / secondary supply fault
• Backplane fault early warning
• Isolates board from backplane due to faults on board
• Integrates other board management functions such as sequencing, reset generation, supervision, watchdog timer, trimming and margining.
• Measures backplane voltages in addition to other board voltages and currents through I²C
• Management of supplies can be changed after assembly through in-system programming via JTAG. (A detailed circuit description is provided in “5.4 CompactPCI Board Management” on page 5-16.)

**Figure 2-9. Complete CompactPCI Express Board Power Management**

**Advantages of CompactPCI Express Board Management Implementation**

• Reduces board cost by integrating other secondary board power management functions into Power Manager II, lower cost MOSFET and smaller hold-off capacitor
• Increases system reliability by reducing the peak current during the hot-swap event as well as during board fault
• Minimizes fault propagation to other boards in the system due to a fault on a circuit board
• Increases shut-down reliability – Ensures safe board shutdown through early warning to the secondary side
• Reduces the number of power management ICs – Integrates the remaining power management functions into the Power Manager II device. (A detailed circuit description is provided in “5.4 CompactPCI Board Management” on page 5-16.)
2.4 Redundant Supply Management

Two Rail 5V Power Supply OR’ing (Using MOSFETs)

Features of Power Manager II-Based Implementation

- Low power loss replacement for diode
- Uses N-Channel MOSFET
- Proactive reverse current protection
- Under-voltage and over-voltage protection
- Individual branch current and voltage measurement through I²C
- Integrates other board management functions such as hot-swap, supply sequencing, voltage supervision, reset generation, watchdog timer, trimming and margining. (A detailed circuit description is provided in “6.3 +5v Power Supply OR’ing (Using MOSFETs) Circuit” on page 6-3.)

Figure 2-10. An ispPAC-POWR1014A Device Implementing Two-Rail 5V OR’ing Control

Advantages of Integrating Power OR’ing Control into a Power Manager II Device

- Increases board reliability through proactive reverse current protection
• Lowers power management cost through integrating multiple power management functions into a single device

• Reduces the number of ICs required to implement the Power OR’ing feature. (A detailed circuit description is provided in “6.3 +5v Power Supply OR’ing (Using MOSFETs) Circuit” on page 6-3.)

**Power Supply OR’ing of N-Rails Using MOSFETS**

**Features of Power Manager II-Based Implementation**

• Single Power Manager II chip implements OR’ing up to six channels

• Low power loss replacement for diode

• Uses N-Channel MOSFET

• Proactive reverse current protection

• Under-voltage and over-voltage protection

• Individual branch current and voltage measurement through I²C

• Integrate other board management functions such as hot-swap, supply sequencing, voltage supervision, reset generation, watchdog timer, trimming and margining. (A detailed circuit description is provided in “6.4 Power Supply OR’ing of Three or More 5V Supply Rails Using MOSFETS” on page 6-5.)
Advantages of Integrating Power OR’ing Control into a Power Manager II Device

- Increases board reliability through proactive reverse current protection
- Lowers power management cost through integrating multiple power management functions into a single device
- Reduces number of ICs required to implement Power OR’ing feature. (A detailed circuit description is provided in “6.4 Power Supply OR’ing of Three or More 5V Supply Rails Using MOSFETS” on page 6-5.)

N-rail (12V/24V) OR’ing

Features of Power Manager II-Based Implementation

- Wide operating voltage range: 6V to 24V
- Single Power Manager II chip implements OR’ing up to six channels
- Low power loss replacement for diode
- Uses N-Channel MOSFET

• Proactive reverse current protection
• Under-voltage and over-voltage protection
• Individual branch current and voltage measurement through I²C
• Integrates other board management functions such as hot-swap, supply sequencing, voltage supervision, reset generation, watchdog timer, trimming and margining. (A detailed circuit description is provided in “6.5 N-rail (12V/24V) OR’ing” on page 6-7.)

Figure 2-12. N- 12V Rail OR’ing Through MOSFET Using an ispPAC-POWR1014A Device

Advantages of Integrating Power OR’ing Control into a Power Manager II Device
• Increases board reliability through proactive reverse current protection
• Lowers power management cost through integrating multiple power management functions into a single device
• Reduces number of ICs required to implement the Power OR’ing feature. (A detailed circuit description is provided in “6.5 N-rail (12V/24V) OR’ing” on page 6-7.)

-48V Supply OR’ing Through MOSFETS
Features of Power Manager II-Based Implementation
• Wide operating voltage range: -30V to -80V
• Low power loss replacement for diode
• Uses N-Channel MOSFET
• Hot-swappable
• Proactive reverse current protection
• Under-voltage and over-voltage protection
• Fuse fault detection
• Controls hot-swap controller. (A detailed circuit description is provided in “6.6 -48V Supply OR’ing Through MOSFETS” on page 6-10.)

*Figure 2-13. Dual -48V MOSFET OR’ing Circuit Using an ispPAC-POWR607 Device*

**Advantages of Integrating Power OR’ing Control into a Power Manager II Device**

• Increases board reliability through proactive reverse current protection
• Lowers power management cost through integrating power OR’ing along with voltage monitoring and contact de-bouncing
• Reduces number of ICs required to implement the Power OR’ing feature. (A detailed circuit description is provided in “6.6 -48V Supply OR’ing Through MOSFETS” on page 6-10.)
2.5 Power Feed Controllers

Dual Rail -48V Power Feed Controller

Features of Power Manager II-Based Implementation

- Wide operating voltage range: -30V to -80V
- Safe MOSFETs operation (SOA)
- Individual channel current limiting
- Individual channel short circuit protection - < 1μs response time
- No-current and over-current flags per output branch
- Individual channel enables
- Retry upon fault detection
- Filters out short period over-current glitches. (A detailed circuit description is provided in “7.2 Dual Rail -48V Supply Feed” on page 7-1.)

Figure 2-14. An ispPAC-POWR607 Implements a Two-Channel -48V Power Feed Circuit

Advantages of Integrating 2-Channel -48V Power Feed into a Power Manager II

- Lowers cost by integrating two-channel power feed into a single chip
- Increases board reliability through current limiting and short circuit protection on a per-channel basis
- Reduces the number of ICs by being able to be customized across a wide range of power feed and protection requirements. (A detailed circuit description is provided in “7.2 Dual Rail -48V Supply Feed” on page 7-1.)
Three-Channels of a 6V-24V Power Feed System

Features of Power Manager II-Based implementation

- Wide operating voltage range: 6V to 24V
- Expandable up to four channels of power feed control
- Safe MOSFET operation (SOA)
- Individual channel current limiting
- Individual channel short circuit protection - < 1μs response time
- No-current and over-current flags per output branch
- Individual channel enables
- Retry upon fault detection
- Filters out short period over-current glitches
- Individual channel current and voltage measurement through I²C
- Integrates other board power management functions. (A detailed circuit description is provided in “7.3 Three Channels of a +12V Power Feed System” on page 7-4.)

Figure 2-15. Three-Channel 12V Power Feed Circuit

Advantages of Integrating Multiple Channel Power Feed into a Power Manager II Device

- Reduces cost of implementation by reducing the number of ICs required for the entire power feed circuit
- Reduced number of power feed ICs – Customizable to meet power feed characteristics across a wide variety of applications
• Increased reliability of the board by integrating other board management functions such as sequencing, reset generation, etc. (A detailed circuit description is provided in “7.3 Three Channels of a +12V Power Feed System” on page 7-4.)

Two-Channel +12V & 3.3V Power Feed With Diode OR’ing

Features of the Power Feed Solution Integrated into Power Manager II

• Designed for use in MicroTCA Power Module – Two channels
• Feeds 3.3V and 12V with OR’ing support using MOSFET
• Turns off 12V power feed within 50µs of AMC card extraction
• Programmable over-current protection
• MOSFET operates in safe operating area
• Supports OR’ing of payload power supply rails (+12V)
• Proactive reverse current protection
• Measures voltage and current through I²C
• Monitors input 12V supply for over- and under-voltage conditions
• Expand up to four channels of power feed as well as trimming of 12V supply for power supply OR’ing function. (A detailed circuit description is provided in “7.4 2-Channel +12V & 3.3V Power Feed With MOSFET OR’ing” on page 7-8.)
Advantages of Two-Channel MicroTCA Power Feed Circuit Using a Power Manager Device:

• Lowers cost of implementation
• Increased reliability through high precision voltage monitoring
• Integrates more channels of power feed circuitry along with trimming features. (A detailed circuit description is provided in “7.4 2-Channel +12V & 3.3V Power Feed With MOSFET OR‘ing” on page 7-8.)
2.6 Trimming and Margining

(A detailed circuit description is provided in “8.4 Trimming and Margining – Principle of Operation” on page 8-3.)

Features of Closed Loop Trimming and Margining Implemented in a Power Manager II Device

- Ideally suited for trimming any low voltage (<1.2V) and high current analog DC-DC converter
- Output voltage accuracy = Set pin voltage ±10mV
- Single chip supports up to eight channels of trimming and margining
- Voltage margining support
- Differential voltage sensing
- Voltage scaling
- VID support through simple PLD
- Integrates trimming and margining along with voltage supervision, sequencing, reset generation and hot-swap controller functions.

Figure 2-17. Low Cost Trimming and Margining Solution Using Power Manager II

Advantages of Implementing Trimming and Margining Using a Power Manager II Device

- Lowers cost of a DC-DC converter - No need for Digital DC-DC converter to support margining and trimming
- Increases functional reliability through DC-DC converter precision output voltage control
- Reduces operating power through voltage scaling
- Reduces debug time by automated margining tests
Reset Generators & Supervisors

3.1 Introduction

One of the most important peripheral ICs required for a microprocessor is a reset generator and a watchdog timer.

The functions of a reset generator are:

1. Hold the processor in a reset condition for an extended period of time during a power turn-on event.
2. If any supply is faulty, activate the reset to prevent it from mis-executing instructions and/or risk Flash memory corruption.

The functions of a watchdog timer are:

1. A monitor for software execution using the trigger generated by the software.
2. If the processor skips a trigger, activate an interrupt or reset the CPU to initiate a recovery process.

Traditional reset generators monitor just one input supply to generate the reset signal. However, most modern processors operate using many supplies, as shown in Figure 3-1. Because a fault on any of the supplies could result in the processor mis-executing instructions, reset generators that monitor only one supply are not adequate. Instead, reset generators are required that monitor all the relevant supplies for faults in order to generate the CPU reset. Figure 3-1 illustrates this. In the example shown it is not clear which of the five supplies should be chosen for reset.
In **Figure 3-1**, the processor requires 1.2V for its core, 1.8V and 0.9V for communicating with DDRII memory and 3.3V for communicating with Flash memory and other peripherals. The processor operates reliably only if all of its supply rails are within the datasheet-specified voltage limits; for example, the acceptable tolerance for: 3.3V (±5%), 1.8V (±5%), 1.2V (±3%), and 0.9V (±5%). One common behavior of a microprocessor when operating at a core voltage less than its specified low voltage level is the misinterpretation of instructions. When the instructions are misinterpreted (also called mis-executed), the program execution becomes unpredictable and the program can hang (not perform the intended task).

If the I/O voltage drops below the specified signaling threshold level, the instruction/data transferred between the memory and the processor can be corrupted.

The misinterpretation of instructions, or proper execution of corrupted instructions, by a microprocessor results in unpredictable behavior; in some cases, the microprocessor could overwrite the on-board Flash memory, resulting in a failed circuit board. Imagine the circuit board failing just because it was extracted from its sub-rack slot!

Unpredictable behavior under low voltage conditions is limited not only to microprocessors, but is also true for any ASIC / FPGA on the board. For example, if the power supply voltage drops below the limit for a networking ASIC, it might send a garbled packet. In some cases it might lose an internally buffered acknowledged packet, resulting in a corrupt message.

**Reliable Reset Generation by Monitoring All Supply Rails**

To prevent the processor from operating when any of its supplies is faulty, one has to monitor all supplies. Monitoring all the supplies for faults is known as supply supervision. Supervisor ICs are used to monitor multiple supplies simultaneously. The following functions are typically performed by one or multiple supervisor ICs:

1. Accurately monitor multiple supply rails for faults and quickly generate an interrupt

2. If the processor core or memory supplies fail, reset the processor
Voltage Supervision Reliability Is Determined By the Supervisor IC’s Fault Detection Accuracy As Well As Its Fault Detection Speed

Figure 3-2 shows the ProcessorPM-POWR605 supervisor and reset IC (replacing the reset IC in Figure 3-1) to monitor all supplies on the circuit board and prevent Flash corruption due to supply faults.

Figure 3-2. The Most Reliable Reset Generator ICs Monitor All Supplies (Supervisor IC)

Parts of a Supervisor IC

Figure 3-3 shows a simple, single supply, voltage monitoring circuit.

Figure 3-3. Single Power Supply Voltage Monitoring Circuit

This circuit uses a voltage comparator to monitor the supply voltage. One limb of the comparator is held at a constant reference voltage through the bandgap voltage reference. The monitored power supply voltage is attenuated using a resistor network such that the attenuated voltage is greater than the bandgap reference voltage as long as the supply voltage is above the fault level.

For example, the bandgap voltage is 2V, and the power supply should be monitored for 3.3V - 5% (= 3.135V). The attenuator is selected such that the output of the attenuator is greater than 2V as long as the monitored supply voltage is greater than 3.135V. The comparator output toggles when the monitored voltage drops below 3.135V. reset generators, supervisors and voltage detectors use circuits similar to the one shown in Figure 3-3.

Figure 3-4 shows the architecture of a device to monitor multiple power supply voltages. These devices contain multiple comparators with individual attenuators to facilitate the simultaneous monitoring of dif-
Different power supply voltages. The outputs of these comparators are logically combined to provide a single logic output to interrupt or reset the processor.

*Figure 3-4. Block Diagram of a Three Power Supply Supervisor IC*

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**Effect of Monitoring Accuracy on System Functionality**

In the circuit shown in Figure 3-3, suppose we use an ideal bandgap reference source (output voltage is always 2V), ideal attenuator (its output voltage is exactly 2V when the input voltage is 3.135V), and an ideal comparator: then, the output of the comparator always toggles exactly when the monitored voltage is 3.135V. But in reality, the bandgap reference voltage changes with temperature, the output voltage of the attenuator varies from device to device and there are inaccuracies with the comparator. All these result in a slight variation of the threshold voltages for each device and across temperature and voltage. The accuracy of a supervisor is a measure of the variation of threshold with respect to the intended threshold.

Many off-the-shelf supervisory ICs detect power faults with an accuracy of ±2%. This means that the actual threshold can vary by as much as 2% of the threshold value across voltage and temperature, and from device to device. Let’s examine the effect of this accuracy on system functionality and fault detection threshold selection.

Refer to Figure 3-5. If the device is specified at a threshold of 3.3V - 5% (3.135V) with a 2% accuracy, that device can declare the power supply as faulty anywhere between 3.135 + 2% and 3.135 - 2% (3.2V to 3.072V), shown by points A and B.
As can be seen, the supervisor can sometimes declare the power supply faulty when it is healthy, or declare it healthy when it is faulty. The latter is a more serious error, because at lower than the desired threshold voltage the processor can be mis-executing instructions, which defeats the purpose of using a supervisor IC.

To avoid such problems, the supervisor threshold should be set such that the entire power supply fault detect range lies within the operating voltage range of the processor. In this case, if the supervisor threshold is set at 3.2V, then the voltage range in which the supervisor can declare the power supply faulty is between 3.14V to 3.26V, thus avoiding the condition under which the processor is operating at a voltage less than its threshold (3.3V - 5%).

In the example shown in Figure 3-6, the threshold value of the supervisor was set at 3.2V. The 3.2V threshold value was actually calculated using the following equation:

\[ V_{TSup} = V_{in} \times \left(1-V_{inTol}/100\right)/\left(1-A_{sup}/100\right) \]

Where \( V_{TSup} \) - Supervisor Threshold

\( V_{in} \) - Power Supply Nominal Voltage

\( V_{inTol} \) - Input Power Supply Tolerance
In this example, $V_{\text{in}}$ at 3.3V, $V_{\text{inTol}}$ - 5%, $A_{\text{sup}}$ - 2%. Substituting these values into the equation above, $V_{\text{TSup}} = 3.3 \times (1 - (5/100)) / (1 - (2/100)) = 3.2V$.

By selecting the Supervisor IC with the threshold at 3.2V or above, the processor is guaranteed to be held in reset when the power supply voltage is less than or equal to 3.3V - 5%.

**Reduced Accuracy Results in Reducing the Power Supply Tolerance Headroom**

Power supply tolerance headroom is the maximum voltage swing allowed for the power supply, across load and operating temperatures, before being declared faulty as shown in Figure 3-6.

Consider the power supply headroom while using a supervisor IC with an accuracy of 2%. According to Figure 3-6, the power supply voltage variation should be higher than 3.26V (the highest voltage at which the supervisor would declare the supply faulty) all the time, or a power supply head room of 1.1%! Typically, power supplies have an output tolerance of about 3% across load and temperature, or the power supply voltage can swing from 3.2V to 3.4V. Clearly the choice for the user is either to use a more expensive supply with a power supply voltage variation of 1%, or use a supervisor with better accuracy.

**Using a Supervisor IC With an Accuracy Of 1%**

From the equation for the same system described above, but using an error of 1%, the supervisor selected should have a threshold of 3.17V. The upper limit of the fault detect range is 3.19V and is still less than the lowest output voltage of the power supply, -3.2V, and a power supply with a voltage variation of 3% can be used.

The board can be operated reliably with a lower cost power supply with larger output voltage tolerance by using a more accurate supervisor. The ispPAC-POWR1220AT8 device offers an accuracy of 0.2% (typical) and 0.7% (maximum).

**Effects of Fault Detection Delay**

Fault detection delay is the duration from the time the power supply voltage drops below the threshold of the supervisor (with very high accuracy), to the time the output of the supervisor toggles, indicating the fault.
In Figure 3-7, the 3.3V supply starts to fail. The power supply supervisor detects the power supply failure and signals the processor. As can be seen from Figure 3-7, the longer the supervisor takes to report the fault, the lower will be the power supply voltage.

For example, the power supply voltage is decaying at a rate of 1V per millisecond. The supervisor precision is very high, which allows the effects of the accuracy described above to be ignored and is set at the threshold of 3.3V - 5%. Let us examine two cases: Fault detection delay is 1ms and 50µs.

**If the Fault Detection Delay is 1ms:**
Because the power supply output voltage continues to drop, by the time the processor is reset its power supply voltage would be much less than the low voltage threshold (about 2V), which means that the processor was executing code until the supply reached 2V! Most likely the processor was mis-executing instructions or locked up. The purpose of the supervisor IC is defeated.

**If the Fault Detection Delay is 50µs:**
By the time the supervisor output is active, the processor voltage would have been reduced by about 50mV from its threshold of 3.3V-5%. Again, the processor operation is not guaranteed at this voltage.

Now, if the threshold was set 50mV above the 3.3V-5% level, the processor would be reset by the time the power supply crossed the operational threshold.

As can be seen, in this application the fault detection delay of 1ms is unacceptable. But a fault detection delay of about 50µs requires the threshold to be set 50mV above the minimum operating power supply voltage threshold.

The supervisor threshold for reliable operation should consider both the accuracy as well as the fault detection delay. Many applications use over-voltage monitoring; that is, if the power supply voltage reaches above the operating voltage range, either the faulty power supply itself is turned off, or a “crow-bar” mechanism is turned on by shorting that power supply output voltage to ground, protecting the devices on the circuit board. Speed of over-voltage detection, in this case, is even more important than the under-voltage fault detection.
The previous example considered only one power supply voltage and used a very accurate supervisor IC. In reality, the number of power supplies that the supervisor should monitor is more than one. The supervisor should be able to monitor all supplies simultaneously for fault and should be able to detect power supply faults with minimum fault detection delay.

Fault detection delay of 1ms or higher is typically seen in circuits that use a microcontroller to monitor voltages using their on-chip ADC.

**Supervisors Built Using ADC and a Microcontroller are Slow**

Some applications use a microcontroller to monitor all the power supplies using an on-chip Analog to Digital Converter and an analog multiplexer. The monitoring algorithm, which typically is initiated by an interrupt once every 5 or 10ms, digitizes each power supply voltage, one supply at a time in a round robin format. The ADC sample is compared with the internally stored threshold. If the ADC read value is lower than the threshold, an output port pin (reset or interrupt pin) is toggled to indicate the power supply fault.

Because the voltage monitoring algorithm is activated by the real time interrupt, the speed of fault detection is also determined by the delay between interrupts (5ms to 10ms). This is too slow for power supply fault detection. The only perceived advantage of a microcontroller is that it offers a flexible interface that lets designers change the power management algorithm after the board is assembled. However, designers typically avoid changing the microcontroller code. Because there are no software simulators available, any change in the code requires extensive circuit board testing. Consequently, the perceived advantage of flexibility is not real.

In order to meet the reliability needs, which include supply fault detection accuracy as well as speed of fault detection, it is advisable to use hardware supervisors instead of microcontrollers. To meet the flexibility needs, the Lattice Power Manager II devices offer programmable analog and programmable digital functions, while providing superior accuracy and fault detection speed. For example, the ispPAC-POWR1220AT8 device monitors 12 power supplies simultaneously and has a fault detection delay of 16µs.

**Other Factors Contributing to Increased Reliability**

The other factors to be considered for reliable power supply fault detection are:

**Glitch filter** – Power supplies are usually fairly noisy during the circuit board operation. The noise can be due to power supply output ripple or to transient currents in the system due to device operation, etc. This noise can result in a randomly toggling supervisor output. To prevent this, supervisors have a glitch filter that generates a clean input to the threshold comparators. Power Manager II devices support a 64µs glitch filter for each input.

**Hysteresis** – A small amount of hysteresis is added to the threshold comparators to prevent the outputs from toggling multiple times, due to power supply noise, when the power supply voltage is at its threshold. In Power Manager II devices, the hysteresis is set to 1% of the threshold voltage. The hysteresis does not affect the accuracy of the threshold because the hysteresis transition requirement is applied after the voltage crosses the threshold.

**Differential Voltage Sensing on a Circuit Board** – When monitoring voltage levels of 1.2V and below, one has to use differential voltage sensing to meet the fault detection accuracy needs of the circuit board.
Newer fabrication processes with smaller transistor geometries stipulate reduced core supply voltage and range such as 1V with a ±50 mV range. If these voltage rails are monitored from a central location, one should consider the ground voltage difference between the monitored node and the supervisor IC. For example, in Figure 3-8, if the ground voltage difference between the CPU and the voltage monitoring device using a single ended sensing method is about 20mV, and if the actual voltage as seen by the CPU is 30mV, the supervisor IC sees a 30mV + 20mV = 50mV rise from the target value, which is a fault, and interrupts the processor or holds the processor in reset even when it could operate.

If the ground voltage difference between the supervisor IC and the CPU is -20mV, the monitor IC does not see a fault even when the supply voltage is lower than its minimum operating threshold level. This results in an unreliable fault detection circuitry.
The safest solution is to use differential voltage sensing (Figure 3-9). Here the ground voltage difference between the CPU and supervisor IC becomes a common mode voltage at the supervisor and its input difference amplifier cancels the common mode voltage before feeding it to the comparator.

Ensuring Deterministic Behavior Under Fault Conditions Through Simulation – The response of a circuit board depends on the power supply failure. As a result, the supervisor is expected to perform different functions depending on the supply that failed. For example, if the core voltage of a CPU failed, the supervisor has to activate the reset signal and start the board power shutdown. However, if one of the redundant supplies failed, the supervisor has to interrupt the processor. To guarantee functional reliability, one should ensure that the design implemented in the Supervisor IC responds to the supply faults correctly. The easiest method is to simulate the design with different types of faults using software, rather than conduct the hardware regression tests.

3.2 N-Supply Supervisor, Reset Generator and Watchdog Timer

The ProcessorPM-POWR605 device provides six precision programmable threshold comparators, five I/Os, two digital inputs, four programmable timers and a 16-macrocell CPLD. This device is used to integrate the supervisor, the reset generator and a watchdog timer function. The ProcessorPM-POWR605 devices monitor supply rails with an accuracy of 0.7% and can identify faults within 12μs.

Figure 3-10. ProcessorPM-POWR605 Integrating Six-Supply Supervisor, Reset Generator & Watchdog Timer

Circuit Operation
The ProcessorPM-POWR605 in the circuit diagram in Figure 3-10 monitors six supplies directly by configuring each of the monitoring comparator inputs to the fault threshold. Two digital outputs of the ProcessorPM-POWR605 device are configured as CPU_Reset and WDT_Int. The CPU_Reset signal supports programmable pulse stretching up to 2 seconds. For example, if the programmable delay is set to 200ms, the CPU_Reset signal will remain active for a period of 200ms after all supplies are above their respective threshold levels. The CPU_Reset signal also gets activated if any of the supplies drops below their respective threshold levels. The WDT_Int signal is activated if the WDT_Trig input is not toggled before the watchdog timer expires. The watchdog timer delay can be programmed from 32μs to 2.5 minutes. The reset_in input is used to activate the CPU_Reset signal from an external input such as a manual reset input signal.
**Reset Generator, Supervisor and Watchdog Timer Algorithm**

1. Activate Reset signal, deactivate WDT_Int signals and wait for all supply levels to reach a value above their respective thresholds.

2. Wait for 200ms (time delay programmable).


4. Wait for any supply to fail. If any supply fails, activate the reset signal and jump to step 1.

**Parallel Equations of the Algorithm**

1. Timer equation waits for WDT trig. If the negative edge of the WDT_Trig signal is not received before the timer expires, activate WDT_Int signal.

2. If Reset_In signal is activated and remains active beyond the 50ms (programmable) de-bounce period, activate the CPU_Reset signal.

**Programmable Features**

- The monitoring threshold for each of the 6 supplies can be individually set to monitor any supply voltage rail from 0.67V to 5.8V.
- Reset pulse stretch duration can be programmed from 32μs to 2 seconds.
- Watchdog timer delay – Watchdog timer delay can be set from 32μs to hours.
- The input reset switch de-bounce delay can be programmed from 32μs to 2 seconds.

**Additional Features That Can be Added to ProcessorPM-POWR605**

- Three of the remaining I/O pins can be used to implement other input monitor features such as warm reset input, software reset input, FPGA Done, etc., or output control features such as DC-DC enables for sequencing, reset distribution to three other devices at different time intervals, etc.
- Over-voltage protection – any of the comparator thresholds can be set to monitor for over-voltage. This configuration can be used to provide over-voltage protection.

**Relevant Power Manager II ICs**

Devices such as the ispPAC-POWR1014/A can be used to monitor up to 10 rails. These devices support dual programmable threshold comparators for each of the inputs that enables them to monitor for both over and under-voltages at the same time. The ispPAC-POWR1220AT8 device can be used to monitor up to 12 rails. These devices also support differential sense inputs that can be used to monitor lower voltage supply rails on a larger board more accurately.
Power Supply Sequencing

4.1 Introduction

The number of power supplies (DC-DC Converters, LDOs, Voltage References) in a circuit board is determined by the number of multi-voltage devices used in its payload section. These devices also determine power supply sequencing. Power supply sequencing indicates that all supplies on the board should not be turned on arbitrarily at any time, but instead should be turned on or off in a prescribed sequence.

For example, on a circuit board a device with 3 supplies of 3.3V, 1.8V and 1.2V, usually the lowest voltage rail should be turned on first, followed by the larger voltages. The turn on sequence is 1.2V, 1.8V and finally 3.3V. Turning these supplies on in this sequence can be implemented easily by connecting the power good signal from the 1.2V supply to the enable signal of the 1.8V supply, and finally connecting the 1.8V power good signal to the enable signal of the 3.3V supply. However, when there are multiple devices, each with its own sequencing requirements, the logic required for sequencing can become complex.

Sequencing Power Supplies with Conflicting Sequencing Requirements

What if there is a second device on that same board with supplies of 3.3V, 2.5V and 1.2V, but the supplies must be turned on starting with the highest voltage? This is further complicated by the fact that 3.3V is the main input supply. Now the designer is required to implement sequencing using the fewest possible supplies.

In such cases, MOSFETs are used to gate the supplies that conflict with conventional sequencing. The circuit in Figure 4-1 shows one such arrangement.
This circuit uses the 3.3V supply to generate the remaining supply rails on the board. Because Device 1 requires 3.3V last and Device 2 requires 3.3V first, the 3.3V is applied to Device 2 with the remaining supplies. Then, the power sequencer enables 2.5V, followed by 1.2V, completing the powering up of Device 2. Next, because the 1.2V for Device 1 is already on, the power sequencer turns on the 1.8V, followed by the 3.3V that is enabled through the MOSFET.

One could have implemented this sequencing by using one more 3.3V supply and turning it on only when Device 1 needed it. However, that would increase the board cost. Adding a second multi-voltage device with its own sequencing requirements can make the sequencing more complex.

There are other factors that contribute to increased supply sequencing complexity.

**Other Factors Adding Complexity to Sequencing Algorithm**

**Number of Board-Mounted Supplies is Increasing**

Modern circuit boards use several multi-voltage ICs such as ASICs, CPUs, memories, and FPGAs. Due to the high level of integration, fabrication processes and support for multiple interface standards, each of these devices can require three to five power supplies. Furthermore, some of these devices require a non-standard, low voltage core supply. So, it is not uncommon for boards to require five to ten supplies! Sequencing the power supplies to meet the needs of each of the devices can be quite complex.

**Abort Sequencing if Any Supply Fails During Power-Up**

Supplies usually fail when they are turning on, leaving some of the devices partially powered. Often some of these devices can only withstand the partially powered condition for a limited time. To mitigate such conditions, the sequencer is required to abort supply sequencing when any supply fails to turn on within a given period. In this case, the sequencer is required to monitor supplies and monitor time during the supply sequencing.
Power-Down Sequencing
Some devices require the power supplies to be turned off in the reverse order of the turn on sequence to prevent undesirable side effects, such as excessive current consumption on one of the rails that can damage the circuitry. Removing power to all DC-DC converters at the same time may not guarantee safe shut down in these cases, because the capacitors connected to the DC-DC converter outputs may not all discharge at the same time.

Minimum Duration Between Two Supplies During Turn On
This condition is usually discovered during the board debug phase, when a board does not turn on reliably. The best solution is to be able to easily increase and/or decrease the delay between sequencing steps.

Accommodating Changes to Sequencing Observed During the Board Debug Phase
Board design engineers are required to meet the sequencing requirements of all devices on the board during the final phases of the board design. To prevent a board re-spin, power sequencing sections are designed with ample provisions for additional components and 0Ω jumpers. This increases the number of components but still may not avoid a jumper wire or two.

Power Supply Ramp-Rate Control
Some devices require that the supply be turned on with a slow ramp to minimize current in-rush. To meet this requirement, designers feed the power through a MOSFET and the ramp-rate is controlled through the gate of the MOSFET.

Turning Unused Power Domains Off to Save Power During Inactive Periods
In order to reduce overall board power dissipation, designers turn off sections of the board when they are not in use. This means that when a power domain is turned on, the supplies in that domain need to be turned on in a sequence. Sometimes, to avoid disruption to the operation of the rest of the board, a shut down sequence may be required to minimize current glitches in the system.

4.2 Flexible N-Supply Sequencing Using Power Manager II Devices
Power Manager II devices offer an ideal set of features, such as a PLD, multiple programmable threshold comparators, multiple programmable duration timers and multiple charge pumps, that can be used to turn MOSFETs on/off with programmable ramp-rate control. The resulting power management algorithm is very flexible because all features of the device, as well as the sequencing algorithm, can be controlled by the LogiBuilder utility in the PAC-Designer software tool. The sequencing algorithm also can be simulated to ensure that the algorithm is able to handle all of the faulty conditions.

Figure 4-2 shows a typical power supply sequencing implementation using the ispPAC-POWR1014A device. In this circuit, the DC-DC converters are controlled by the ispPAC-POWR1014A device. While it is possible to interface with the active-low enable signals directly with the ispPAC-POWR1014A device outputs, an external transistor may be necessary to interface with active high enable signals.

Voltages are Monitored During/After Sequencing
All DC-DC converter voltages are monitored by the programmable threshold comparators of the ispPAC-POWR1014A device. In this circuit, the ispPAC-POWR1014A device uses a programmable algorithm designed using the PAC-Designer software tool to turn the DC-DC converters on/off through the DC-DC

converter’s enable pins. During supply sequencing, the ispPAC-POWR1014A device will monitor the output voltage of each of the DC-DC converters using the on-chip programmable threshold precision comparators.

The power supply sequencing is controlled by the open drain output pins of the ispPAC-POWR1014A. These output pins are controlled by the on-chip PLD. The sequencing algorithm is implemented using the LogiBuilder utility in the PAC-Designer software. Using the LogiBuilder utility, one can implement the following sequencing methods:

1. No sequencing – Here all the supplies are turned on at the same time and no sequencing is necessary.

2. The ispPAC-POWR1014A device waits for all the supplies to reach their operating levels and then generates a power good signal for the board to begin the initialization process. Operating voltage levels are higher than the lower voltage limit and less than the over-voltage limit.

3. Closed loop sequencing – This is a sequence where one supply is turned on only after the previous supply has reached its operating levels.

4. Time-based sequencing – The power sequencer inserts a time delay between each of the supplies without first checking if the first supply reached its normal operating level.

5. Closed loop sequencing with time delay – The second supply is turned on a fixed time after the first supply is on and is within its normal operating voltage level.

6. The supply reaches its normal operating condition within a period of time. Often, supplies fail during turn on. To prevent the locking up of sequencing while waiting for this failed supply, the algorithm turns the supply on and, if the supply does not reach its normal operating voltage levels within a specified time, then the supply is considered faulty and action for incomplete sequencing is initiated.

7. Turn on multiple supplies with a watchdog timer – In this case, supplies are turned on using any of the previous methods. After all the supplies are turned on, the power sequencing algorithm ensures that all supplies are on within the total watchdog timer period. If the watchdog timer expires, the faulty sequence action is initiated.

Any or all of these sequencing methods can be implemented easily using the LogiBuilder utility within the PAC-Designer software. LogiBuilder enables implementation of a power management program using six types of intuitive, user friendly and powerful instructions. The user has the flexibility to apply these turn-on rules to each supply, or for groups of supplies, simply by using the appropriate LogiBuilder instructions to manage that supply.
N-Supply Closed Loop Sequencing Algorithm

This section describes a closed loop N-supply sequencing algorithm implemented in the ispPAC-POWR1014A device, as shown in Figure 4-2. Table 4-1 provides a detailed explanation of LogiBuilder instructions, along with the associated sequencing method.

Figure 4-2. Flexible N-Supply Sequencing using the ispPAC-POWR1014A Device

The power management algorithm is implemented in LogiBuilder in a sequence of steps using the LogiBuilder instructions. The Power Manager II device then executes these steps to sequence the supplies on the board. In this example there are N supplies.

During each of the first N steps, the LogiBuilder instruction turns on a power supply and waits for the voltage to reach its operating limit.

1. Turn on DC-DC/LDO #1, enable the converter and wait for its output voltage to reach the operating range. The ispPAC-POWR1014A device uses two precision programmable threshold comparators to monitor a given voltage rail. One comparator threshold is set to the lower voltage limit of that voltage rail and the second comparator threshold is set to the over-voltage limit. A DC-DC converter is in its operating limit when its voltage is between the over and the under-voltage limits.

2. Turn on the DC-DC/LDO #2 enable signal and wait for its voltage to reach operating range.

3. Turn on the DC-DC/LDO #3 enable signal and wait for its voltage to reach its operating range (Same function as step 2).

4. Continue turning on supply #4 (Same function as step 2).

5. Continue turning on supply #5 (Same function as step 2).
N. Continue turning on supply #N (Same function as step 2).

O. If all the supplies are within the operating range, activate the power good signal. If any of the supplies are faulty, turn all the supplies off and activate the Sequence_Fail signal.

P. Wait for the Recycle_Power to become active and then jump to step 1.

Q. Shut-Down Signal Interrupt Routine – When the shut down signal becomes active, jump to step O.

**N-supply Closed Loop Sequencing with Failure Monitor Algorithm**

In the N-supply closed loop sequencing algorithm shown above, a supply failure would hold up the sequence forever. While this phenomenon may be acceptable for most applications, some ICs may be sensitive to being in a partially powered state for extended periods. In that case, the algorithm can be modified to include turn on with monitor mode. For example, if a device is sensitive to the duration of a partial power condition at step 2 of the algorithm above, it can be changed to the following:

1. Turn on DC-DC #1, enable converter and wait for its output voltage to reach operating range.

2. Turn on DC-DC#2 enable signal and wait for its voltage to reach operating range within 5ms. If the supply does not reach operating range within 5ms jump to step O or else proceed to turn off the rest of the supplies.

3. Turn on DC-DC #3 enable converter and wait for its output voltage to reach operating range.

4. Continue turning on supply #4, similar to step 3.

5. Continue turning on supply #5 with fault monitor, similar to step 2.

N. Continue turning on supply #N, similar to step 3.

O. If all the supplies are within the operating range, activate the power good signal. If any of the supplies are faulty, turn all the supplies off and activate the Sequence_Fail signal.

P. Wait for Recycle_Power to become active and then jump to step 1.

**Applying LogiBuilder Instructions to Sequencing Methods**

As stated earlier, the LogiBuilder utility in the PAC-Designer software tool provides instructions to directly support different types of sequencing. Figure 4-3 shows the block diagram of a power sequencing circuit. Table 4-1 lists different LogiBuilder instruction sequences to implement the different sequencing methods used to enable the power to Device #1.
Device #1 specifies that the 1.2V should be the first supply to turn on, the second is 2.5V for I/O and finally 3.3V for another set of I/Os. Table 4-1 describes the LogiBuilder instructions to implement different sequencing methods while meeting the sequencing requirements of Device #1.

Table 4-1. LogiBuilder Instructions Description for a Given Sequence Method

<table>
<thead>
<tr>
<th>Sequence Method</th>
<th>LogiBuilder Instruction(s)</th>
<th>Output</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Closed Loop Sequencing with 1.2V followed by 2.5V &amp; 3.3V</td>
<td>Wait for Core_1V2_OK</td>
<td>En_1V2=1</td>
<td>The 1.2V DC-DC is enabled (Active high) and the instruction waits at this step until 1.2V is in regulation</td>
</tr>
<tr>
<td></td>
<td>Wait for IO_2V5_OK AND IO_3V3_OK</td>
<td>En_2V5=0, En_3V3=1</td>
<td>The 2.5V DC-DC is enabled (Active low) and The 3.3V DC-DC is also enabled (Active high). This instruction waits at this step until 2.5 &amp; 3.3 supplies are in regulation</td>
</tr>
<tr>
<td>Open Loop Sequencing with 1.2V followed by 2.5V Separated by 5ms</td>
<td>En_1V2 = 1</td>
<td></td>
<td>The 1.2V DC-DC is enabled (Active high) and the instruction does not wait at this step until 1.2V is in regulation</td>
</tr>
<tr>
<td></td>
<td>Wait for 5ms using Timer 1</td>
<td></td>
<td>Waits for 5ms at this step before activating the next supply</td>
</tr>
<tr>
<td></td>
<td>En_2V5 = 0</td>
<td></td>
<td>The 2.5V DC-DC is enabled (Active low) and the instruction does not wait at this step until 2.5V is in regulation but proceeds with the next instruction</td>
</tr>
<tr>
<td>Closed Loop Sequencing with 1.2V followed by 2.5V Separated by 5ms</td>
<td>Wait for Core_1V2_OK</td>
<td>En_1V2=1</td>
<td>The 1.2V DC-DC is enabled (Active high) and the instruction waits at this step until 1.2V is in regulation</td>
</tr>
<tr>
<td></td>
<td>Wait for 5ms using Timer 1</td>
<td></td>
<td>Waits for 5ms at this step before activating the next supply</td>
</tr>
<tr>
<td></td>
<td>Wait for IO_2V5_OK</td>
<td>En_2V5=0</td>
<td>The 2.5V DC-DC is enabled (Active low) and the instruction waits at this step until 2.5V is in regulation but proceeds with the next instruction</td>
</tr>
<tr>
<td>Turn-on and ensure that the supply turns on within a short period of time</td>
<td>Wait for Core_1V2_OK with Timeout of 5ms using Timer1. If Timer1 Go to Fault</td>
<td>En_1V2=1</td>
<td>The 1.2V DC-DC is enabled (Active high) and the instruction waits at this step until 1.2V is in regulation within 5ms (determined by Timer 1), if Timer 1 expires, jump to Fault routine</td>
</tr>
</tbody>
</table>
Any of these sequencing methods can be used for any supply or group of supplies. The timer values can be set to any value between 32µs and 2 seconds.

**Advantages of Power Manager II-based Supply Sequencing**

The sequencing of supplies is completely programmable. Designers can adjust the turn on or turn off sequence and the associated timing to provide reliable board start up after the board is assembled. No board re-spin is needed. Once the supplies are sequenced the ispPAC-POWR1014A device monitors all of the supplies for faults.

**Additional Power Management Functions that can be Integrated into Power Manager II**

In this circuit, the ispPAC-POWR1014A device provides flexible sequencing. The other functions that can be integrated into an ispPAC-POWR1014A device are:

1. **Voltage supervision** – Monitor all supplies after sequencing for fault and generate an interrupt signal such as a low voltage detect.

2. **Reset generation** – After the sequence is complete, the ispPAC-POWR1014A device can be used to release Reset for the CPU.

3. **Hot-swap controller** – If power supply sequencing is required in a positive voltage hot-swappable board, the hot-swap function can also be integrated.

4. **Voltage measurement** – In addition to all of the supplies being monitored for faults, an external microcontroller can measure individual voltages through the I²C interface.

5. **Fault logging** – In case of a fault, the ispPAC-POWR1014A device can output the status of all comparators to an external PLD for logging into a non-volatile memory to aid debug.

**Applicable Power Manager II Devices**

Power Manager II devices that can be used for implementing sequencing are the ispPAC-POWR1220AT8, ispPAC-POWR1014/A, ispPAC-POWR607 and ProcessorPM-POWR605.
4.3 Sequencing With MOSFETs and DC-DC Converter Enables

In some cases, to meet the device’s sequencing needs without using additional DC-DC converters, MOSFETs are required. Figure 4-4 shows one such circuit, where a ispPAC-POWR1014A device controls the DC-DC converter’s enable signals as well as an N-Channel MOSFET. In this circuit the MOSFET is used to enable 3.3V to Device 1 after all of its other supplies are turned on.

To turn-on an N-Channel MOSFET on a 3.3V rail, its gate potential should be at least 8V. Designers either use the 12V supply (if available on the board) or a charge pump IC to generate 8V or higher. The ispPAC-POWR1014A device integrates two MOSFET gate drivers based on integrated charge pumps that can generate up to 12V. The charge pump voltage can be programmed to 6V, 8V, 10V or 12V. In addition, the MOSFET turn on ramp-rate also can be controlled using the programmable current source feature of the MOSFET driver. The gate drive source current can be set to 12.5\(\mu\)A, 25\(\mu\)A, 50\(\mu\)A and 100\(\mu\)A. The higher the current setting, the faster the MOSFET turn-on time.

Circuit Operation

In the circuit shown in Table 4-4, the ispPAC-POWR1014A device is controlling the enable signals of 1.8V, 2.5V and 1.2V DC-DC converters. The MOSFET driver of the ispPAC-POWR1014 device is used to turn the MOSFET Q1 on/off. The sequencing logic is implemented in the PLD using the LogiBuilder utility in the PAC-Designer software tool.

After sequencing is complete, the ispPAC-POWR1014A activates the Power_Good signal. If the sequencing fails to complete, the algorithm activates the failed (to complete the sequence) signal.

The Shut_Dn signal is used to turn the supplies off in reverse sequence.

**Figure 4-4. An ispPAC-POWR1014A Device Implementing Sequencing with MOSFET and DC-DC Enables**
Power Sequencing Algorithm

The algorithm implemented in the Power Manager II is shown in Table 4-2 and Table 4-3. This section uses the actual LogiBuilder code extracted from the PAC-Designer software.

### Table 4-2. State Machine 0

<table>
<thead>
<tr>
<th>Step</th>
<th>Instruction</th>
<th>Outputs</th>
<th>Interruptible</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Begin Startup Sequence</td>
<td>0</td>
<td>ispPAC-POWR1014-02 reset</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Wait for AGOOD</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Wait for INP_3V3_OK</td>
<td>0</td>
<td>Do not proceed with the sequencing until input supply is within operating range</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Wait for IO_2V5_OK</td>
<td>En_2V5 = 1,</td>
<td>0</td>
<td>3.3V is stable for Device 2. Now enable 2.5V and wait for it to reach operating range</td>
</tr>
<tr>
<td>4</td>
<td>Wait for Core_1V2_OK or 2.56ms using Timer 1 If Time-out Then Go to 13 with {Failed = 1,}</td>
<td>En_1V2 = 1,</td>
<td>0</td>
<td>1.2V supply should turn on within 2.5ms. If 1.2V fails to turn on, activate Failed signal</td>
</tr>
<tr>
<td>5</td>
<td>Wait for IO_1V8_OK</td>
<td>En_1V8 = 0,</td>
<td>0</td>
<td>Turn on 1.8V with active low enable signal and wait for it to reach the operating level</td>
</tr>
<tr>
<td>6</td>
<td>Wait for FET_3V3_OK</td>
<td>En_3V3_MOSFET = 1,</td>
<td>0</td>
<td>Turn the MOSFET on to begin feed 3.3V to Device 1 and wait for it to be stable</td>
</tr>
<tr>
<td>7</td>
<td>Wait for NOT INP_3V3_OK OR NOT IO_2V5_OK OR NOT IO_1V8_OK OR NOT Core_1V2_OK OR NOT FET_3V3_OK</td>
<td>Power_Good = 1,</td>
<td>1</td>
<td>Wait for any supply to fail. If any supply fails, turn all supplies off in reverse order. The power good signal is activated as soon as the state machine enters this step</td>
</tr>
<tr>
<td>8</td>
<td>Begin Shutdown Sequence</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>En_3V3_MOSFET = 0, Power_Good = 0,</td>
<td>0</td>
<td>Fault condition, turn the MOSFET off first and deactivate Power_Good Signal</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>Wait for 2.56ms using timer 1</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>En_1V8 = 1,</td>
<td>0</td>
<td>Turn-off 1.8V supply</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>Wait for 2.56ms using timer 1</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>En_1V2 = 0,</td>
<td>0</td>
<td>1.2V supply off</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>Wait for 2.56ms using timer 1</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>En_2V5 = 0,</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>Halt (end-of-program)</td>
<td>0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Table 4-3. Exception Table

<table>
<thead>
<tr>
<th>EID</th>
<th>Expression</th>
<th>Outputs</th>
<th>Exception Handler</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>If Shut_Dn</td>
<td>(no outputs specified)</td>
<td>Go to step 8</td>
<td>Begin Shutting down supplies in reverse order when Shut_dn signal is active</td>
</tr>
</tbody>
</table>

### Applicable Power Manager II Devices

Power sequencing using MOSFETs can be implemented in ispPAC-POWR1220AT8, ispPAC-POWR1014/A and ispPAC-POWR607 devices.
Hot-Swap Controllers

5.1 What is a Hot-Swap Controller?
Hot-swap controllers limit the inrush current when a circuit board is plugged into a live backplane. In addition, these devices offer over-current, over-voltage and under-voltage protection to the circuit board. Figure 5-1 shows the block diagram of a typical hot-swap controller implementation for a positive backplane power supply rail. \( R_S \) is the current sense resistor. The MOSFET \( Q_1 \) is used to control the current through the circuit. The resistors \( R_1, R_2 \) and \( R_3 \) are used to monitor the backplane voltage. The hold-off capacitor, \( C_h \), is used to provide power to the board when the backplane voltage briefly drops below the low operating voltage (under-voltage) threshold (say, for less than 10ms).

Figure 5-1. Positive Rail Hot-Swap Controller

When the card is plugged into the live backplane, the hold-off capacitor, \( C_h \), begins to draw a large amount of current from the backplane. The hot-swap controller limits the current in-rush by controlling the voltage applied to the MOSFET gate using the voltage across \( R_S \) as feedback. The MOSFET will operate in this current limit mode until the capacitor \( C_h \) is fully charged.

During the brief capacitor charging period, the inrush current drawn from the backplane often can be significantly higher than the normal board operating current. As a result, the backplane voltage can dip below the under-voltage threshold momentarily for the other cards attached to...
the backplane. The charge stored in the capacitor, \( C_h \), keeps the card operating during this brief voltage dip period.

Hot-swap controllers are also required to isolate the board from the backplane in case it develops a fault during operation. For this purpose, the hot-swap controller will monitor the current through the sense resistor \( R_S \). When the voltage across the resistor \( R_S \) increases beyond its threshold value, the hot-swap controller turns the MOSFET off.

If the backplane voltage drops below the under-voltage threshold or goes above the over-voltage threshold, the power supply to the load is shut off by turning the MOSFET off.

**Figure 5-2. Negative Supply Hot-Swap Controller**

One of the popular backplane voltages in the telecom industry is -48V. Hot-swap controllers for negative supplies use the current limiting MOSFET on the negative supply limb, as shown in Figure 5-2. Functions of negative rail hot-swap controllers are similar to the positive voltage hot-swap controllers described above.

**Hot-Swap Circuit Design Considerations**

In a hot-swap controller circuit the MOSFET will be required to withstand high levels of power dissipation while the hold-off capacitor is being charged. The suitability of the MOSFET for this purpose is determined by its Safe Operating Area (SOA) curves.

When a circuit board fault occurs, the current through the MOSFET can increase significantly. If the MOSFET is not quickly turned off, the peak power dissipated on the MOSFET can damage it. hot-swap controllers are also required to monitor over-current conditions and initiate either a fold-back current limiting mechanism or turn the MOSFETs off. Usually under high current conditions, the MOSFET should be turned off within approximately 1\( \mu \)s. Some hot-swap controllers implement “retry” to turn the board on if the fault subsequently clears on its own accord. hot-swap controllers are also required to monitor for low voltage conditions and shut the board off when such a condition occurs.

**5.2 Implementing a Positive Supply Hot-Swap Controller Using Power Manager II Devices**

There are many types of hot-swap controllers with different current control and other monitoring mechanisms. Usually, the complexity of a hot-swap controller depends on the power dissipation requirement of a circuit board. This section shows how Lattice Power Manager II devices can be used to implement hot-swap controllers that range from the simple to the sophisticated.
Hot-Swap Controller Using Soft-start

Figure 5-3 shows the ispPAC-POWR1014A device implementing a simple hot-swap controller. The principle of operation of this circuit is also called a ‘soft-start’ mechanism.

Figure 5-3. Hot-Swap Control Implemented Through MOSFET Ramp Rate Control

Circuit Operation

In this design, the backplane supply is 5V. The card with the ispPAC-POWR1014A device is plugged into the live 5V backplane. The ispPAC-POWR1014A device first waits for the 5V backplane voltage to stabilize from the initial contact bounce. After the contact bounce period is complete, the ispPAC-POWR1014A turns the MOSFET Q1 on through the Soft_start pin (HVOUT pin). The HVOUT pin source current is set to a minimum (12.5 μA). This current charges the MOSFET gate capacitance slowly. As a result, the MOSFET on-resistance also drops slowly to its final RDS-on value (usually in a few tens to hundreds of mΩ range). This gradual reduction in MOSFET on-resistance reduces the current in-rush.

This circuit can only be used in low power and low voltage boards. It also requires that the instantaneous power dissipated by the MOSFET does not violate its safe operating area specification.

Soft-start algorithm:

1. Wait for 5V to be continuously on for 100ms and ensure it is within tolerance by monitoring Inp_5V signal.

2. Turn on Q1 by setting soft-start signal to logic 1.

3. Wait until supply at 5V load is within tolerance by monitoring the Out_5V signal.

4. Enable the 5V load through the Start_5V_Load signal.

Programmable Features

The following parameters can be changed to make this circuit meet a wide range of application needs:

- Comparator thresholds can be changed to suit difference backplane voltages, e.g., 5V or 3.3V. The soft-start function for 12V can be implemented using a P-Channel MOSFET and driven by one of the logic outputs. Negative rail soft-start can be implemented using N-channel MOSFETs.
- Contact de-bounce period can be changed from 50ms to 2 seconds.

- MOSFET turn on ramp rate can be set using the four current settings available for each HVOUT pin.
- Design can be used to implement a dual hot-swap controller for dual supply backplanes using two MOSFET drivers in the ispPAC-POWR1014 device.

**Integrate Other Board Power Management Functions into a ispPAC-POWR1014A Device**

This design consumes a very small portion of the ispPAC-POWR1014A device. The remaining resources can be used to implement board power management functions such as power sequencing, voltage supervision, reset generation and watchdog timer.

In addition, one may also include faulty board identification and protection. If the board is healthy, the voltage at the hold-off capacitor should stabilize within a short period of time (say, 5ms). If the board is faulty (drawing more current than expected), the voltage at the capacitor will drop to a value less than the lower voltage threshold. When such a condition arises, the MOSFET is turned off immediately. This prevents continuous overloading of the backplane.

One can also monitor the backplane voltage to generate early warning to the load circuit for safe turn off.

Backplane voltage and other on board rail voltages can be measured using the ispPAC-POWR1014A device’s ADC via the integrated I2C interface.

**Applicable Power Manager II Devices**

In this example, a ispPAC-POWR1014A device was used to implement the soft-start function. However, the soft-start control application can also be implemented in ispPAC-POWR1220AT8, ispPAC-POWR1014 and ispPAC-POWR607 devices. The ispPAC-POWR607 devices, however, do not support the programmable ramp-rate control feature.

**Hot-Swap Controller with Hysteretic Current Limit Mechanism**

When designing hot-swap controllers for boards with higher power dissipation, or when one is not able to guarantee the MOSFET safe operating area limits are not violated during the hot-swap operation, or when the backplane inrush current is to be limited to prevent disruption to other boards plugged into the same backplane, the following circuit (Figure 5-4) should be used. This circuit begins to operate with the MOSFET $Q_1$ turned on. The current starts to increase to charge the capacitor $C_h$. When the current exceeds the preset value, the logic in the hot-swap controller turns the MOSFET off. At that time, the current starts to decrease. When the current drops below the preset value, the logic turns the MOSFET on and the current starts to increase again. This method of limiting the current to a preset value by turning the MOSFET on/off is called hysteretic mode of operation.
There are two additional blocks in comparison to the soft-start control circuit shown in Figure 5-3: current monitoring and quick shut-off control. The name of ispPAC-POWR1014A device’s high voltage MOSFET gate drive pin has been changed from Soft_start to Hyst_Ctrl.

**Principle of Operation of the Hysteretic Control Mechanism**

Figure 5-5 shows plots of the gate drive of the MOSFET Q1, current through the MOSFET and the voltage across the capacitor C_h. When Hyst_Ctrl signal is turned on, Q1’s gate capacitance starts to charge. At the same time, the current through the MOSFET also begins to increase. The current through the MOSFET passes through the sense resistor Rs. The current sense amplifier (CSA) outputs a current proportional to the voltage dropped across Rs into series resistors R1 and R2. The voltage drop across R1 and R2 is monitored by the ispPAC-POWR1014A device through the signal I_In (one of the VMON pins). The comparator output of this VMON pin toggles when the current through Rs exceeds the maximum allowable limit (IH). As a result, the logic equation in the PLD turns the Hyst_Ctrl pin off. When the Hyst_Ctrl pin is at logic 0, the MOSFET gate starts to discharge, throttling the current through the MOSFET channel, and the current through the MOSFET begins to drop. The voltage at the I_In pin reduces. When the voltage drops below the I_In pin threshold (IL), the logic equation in the ispPAC-POWR1014A device turns the MOSFET back on.

This cyclic throttling action maintains the average current to a value determined by the current threshold settings. This technique provides many of the advantages of linear current control while sidestepping many of the potential stability issues.
Turning MOSFET Off Under Short Circuit Conditions
To prevent excessive current drain from the backplane and to protect the MOSFET against damage due to excessive power dissipation during a short circuit event, the MOSFET should be turned off within 1μs from the time the current reaches a dangerous level. In Figure 5-4, the ispPAC-POWR1014A device’s digital input pin IN1 is driven to Logic 0 by the transistor Q2 when the current through the 5V supply rail exceeds short circuit current limit. The voltage across R2 is 0.7V when the current through RS reaches the short circuit current level. The logic equation in the ispPAC-POWR1014A device turns the MOSFET off immediately within 200ns.

Hysteretic Hot-Swap Control Algorithm
The algorithm is divided into two sections:

• Logic equations for hysteretic control and fast-acting MOSFET shut down during a short circuit event
• Sequence control for overall hot-swap event control

**Equation 1:**

\[ Hyst\_Ctrl.D = En\_Hot\_swap \text{ AND NOT } I\_IN \]

Equation 1 implements the hysteretic control. The signal En_Hot_Swap turns the hot-swap controller on or off. This signal is turned on by the sequence control algorithm after the contact-de-bounce period. The Hyst_Ctrl (D-type flip-flop) is turned off when the I_In signal voltage exceeds the over-current limit level and turns back on when the I_In signal drops below the threshold. The comparator hysteresis provides the delay between turn-on and turn-off.

**Equation 2:**

\[ Hyst\_Ctrl.Reset = \text{NOT Short\_Ckt} \]

Equation 2 is a combinatorial equation that turns the MOSFET off as soon as the Short_Ckt signal is equal to logic 0.
Sequence control:

1. Wait for 5V to be continuously on for 100ms and within the tolerance limits (monitoring Inp_5V signal).

2. Turn on the hysteric hot-swap action by turning on En_Hot_swap signal.

3. Wait for supply at 5V load is within tolerance limits by monitoring the Out_5V signal.

4. Enable the 5V load through the Start_5V_Load signal.

5. During normal operation, if an over current or under-/over-voltage supply fault occurs for a period greater than the hold-off period (5ms to 10ms), then shut the MOSFET off and retry.

Programmable Features
This circuit offers many programmable features that make it suitable for a wide range of applications.

• Comparator thresholds can be changed to suit different backplane voltages, e.g., 5V or 3.3V.

• Contact de-bounce period can be changed from 50ms to 2 seconds.

• Over-current and short circuit current levels can be set independently.

• The design can be used to implement dual hot-swap controllers for dual supply rail backplanes.

• Hold-off time is programmable from 2 to 100ms (time during which the MOSFET should be left on under supply fault). After this period expires, the MOSFET is turned off.

The ispPAC-POWR1014A Device Can Integrate Other Board Power Management Functions
The difference between the soft-start method and hysteretic control in the algorithm is the addition of two logic equations. As a result, the remaining resources can be used to implement power sequencing, voltage supervision, reset generation and watchdog timer functions for the board.

For faulty board identification and protection, add a watchdog timer when monitoring the load voltage immediately after the hysteretic control loop is turned on (after step 4). If this timer expires before the 5V reaches the operating threshold level (implying a fault that is preventing the charge build up in the capacitor C_h), turn the MOSFET off and turn an LED on, indicating the supply fault.

Add backplane voltage monitoring logic to provide early warning to the load circuit for safe turn off.

Applicable Power Manager II Devices
This example used the ispPAC-POWR1014A device to implement the hysteretic control hot-swap function. However, the hysteretic control can also be implemented in ispPAC-POWR1220AT8, ispPAC-POWR1014 and ispPAC-POWR607 devices.

Advantages of Using Power Manager II Devices for Hot-Swap Controller
There are many hot-swap controllers in the market. Designers have to use these hot-swap controller devices in addition to the board management function. The Power Manager II device reduces the cost of implementation by integrating the hot-swap controller function along with overall board management into a single chip.

In addition, the design can be used across a wide range of applications.
12V/24V Hot-Swap Controller

The operating principle of this circuit is the same as that of the 5V hot-swap controller with hysteretic control mechanism. Two additional features are added to make it compatible with the 12V hot-swap function. These features are an external charge pump and limiting operation of the MOSFET within its safe operating range.

The maximum MOSFET gate drive voltage of ispPAC-POWR1014/A and ispPAC-POWR1220AT8 devices is 12V. However, to turn the N-Channel MOSFET on the 12V or 24V rail, one has to drive its gate voltage to 22V or 34V, respectively (about 10V above the rail voltage). To achieve this high voltage, the following circuit (Figure 5-6) implements an external charge pump using diodes, capacitors and a transistor.

The operating principle of the external charge pump is as follows (Figure 5-6). The C_Pmp signal (ispPAC-POWR1014A HVOUT pin) toggles between 12V (for 32μs) and 0V (for 8μs) cyclically. When the C_Pmp signal is at 0V, the capacitor C1 gets charged to backplane voltage of 12V through the diode D1. At this time the transistor Q2 is off. When the C_Pmp signal toggles up to 12V, the C1 voltage gets added to the C_Pmp pin voltage, resulting in the generation of approximately 24V at the junction of C1 and D1. This voltage turns Q2 on and charges the capacitor C2 to about 22V through the diode D2. This voltage is sufficient to turn the MOSFET Q1 on.

The transistor Q3, driven by the S_Dn signal, is used to shut the MOSFET Q1 off by discharging the MOSFET Q1 gate and C2 when there is a fault.

Figure 5-6. 12V/24V Hot-Swap Controller Using an ispPAC-POWR1014A Device

Limiting the Hot-Swap MOSFET Within its Safe Operating Area

The ispPAC-POWR1014A device implements a hysteretic control loop to limit the current through the MOSFET within safe operating limits when charging the hold-off capacitor Ch. The HVOUT pin stops toggling when the current through the resistor Rs exceeds the set threshold. When toggling is stopped, the
voltage at the MOSFET gate starts to drop down, reducing the current through the MOSFET. When the current drops below the threshold, the C-Pmp signal starts to toggle, turning the charge pump on again.

**Figure 5-7. MOSFET Safe Operating Area (IRF7832)**

The safe operating area of the chosen MOSFET (IRF7832) is shown in Figure 5-7 as a log-log graph with the voltage across the MOSFET on the x-axis and the current through the MOSFET on the y-axis. The dashed lines in the graph show the maximum allowable current at a given voltage across the MOSFET for a given pulse width. The red line on the graph shows the operating current limit of this circuit. Throughout the power-on process, the MOSFET never exceeds its safe operating area limits.

**Figure 5-8. Inrush Current Through the MOSFET**
In the oscilloscope plot shown in Figure 5-8, the green trace is the current through the MOSFET and the pink trace is the voltage across the capacitor. As can be seen, the current is limited to 2A until the voltage across the capacitor reaches 6V, and after that the current is limited to 4A.

*Figure 5-9. Circuit Operation During Short Circuit*

When the circuit is turned on to a short circuit, the power feed begins as usual. If the capacitor voltage does not reach 9V within 10ms, the MOSFETs are turned off and the circuit waits for a retry command. *Figure 5-9* shows the oscilloscope plot of the MOSFET turn-on current with the capacitor $C_h$ replaced with a short.

**12V Hot-Swap Controller Algorithm**

The hot-swap controller algorithm is divided into the following sections:

- Logic equations for the external charge pump operation
- Logic equations for hysteretic control and fast-acting MOSFET shut down during a short circuit event
- Sequence control for overall hot-swap event control

**Equation 3:**

$\text{Toggle}\_\text{C}\_\text{Pump}.D = 32 \ \mu\text{s Timer Terminal Count}$

**Equation 4:**

$32 \ \mu\text{s Timer Gate}.D = \text{NOT Toggle}_\text{C}\_\text{Pump}$

`Toggle_C_Pump` is an internal variable used to generate 8 $\mu$s wide pulses.

Equation 3 and Equation 4 use an on-chip hardware timer. There are four programmable timers in a ispPAC-POWR1014A device. Each timer delay can be set from 32$\mu$s to 2 seconds. Timer count-down is ini-
tiated by applying a logic 1 to the gate signal. The timer_TC signal transitions to logic 1 after the timer count-down is complete. When the timer gate signal is connected to the inverted Timer_TC (Figure 5-10), the timer generates a 4µs pulse every time the timer expires.

**Figure 5-10. Timer Configuration to Implement Programmable Frequency Clock**

If the timer delay is set to, say, 32µs, the timer TC and the timer gate outputs will be:

**Figure 5-11. Generating 4µs Wide Pulses with Programmable Interval Using Timer**

Equation 3 latches the timer TC into a variable Toggle_C_Pump. This stretches the timer gate by another 4µs. The waveform of Toggle_C_Pump is shown in Figure 5-12.

**Figure 5-12. Generating 8µs Wide Pulses with 32µs Interval Using Toggle_C_Pump**
Equation 5 controls the MOSFET drive circuit. The Toggle_C_Pump signal is used to drive the external charge pump circuit. This pulse train is modulated by:

- **En_Hot_Swap** – Controlled by the sequence control
- **(NOT I_IN_2_A AND NOT OUT_12V_GT_6V)** – Hysteretic control that limits the current to less than 2A when the voltage at \( C_h \) is less than 6V
- **(NOT I_IN_4_A AND NOT OUT_12V_GT_9V)** – Hysteretic control that limits the current to 4A when the voltage at \( C_h \) is less than 9V
- **MOSFET_FULLY_ON** – Term that turns the MOSFET fully on when the voltage at \( C_h \) is greater than 9V. This term is controlled by the sequence controller

Equation 5:

\[
C_{Pmp.D} = \text{NOT Toggle\_C\_Pump AND En\_Hot\_swap AND (NOT I\_IN\_2\_A AND NOT OUT\_12V\_GT\_6V OR (NOT I\_IN\_4\_A AND NOT OUT\_12V\_GT\_9V OR MOSFET\_FULLY\_ON)}
\]

Equation 6 is a combinatorial equation that turns the MOSFET off as soon as the Short_Ckt signal is equal to logic 0 or when the operating current is greater than 4A.

Equation 6:

\[
Shut\_Dn = \text{NOT Short\_Ckt or (MOSFET\_FULLY\_ON AND I\_IN\_4\_A)}
\]

Sequence control:

1. Wait for 12V to be continuously on for 100ms and within tolerance by monitoring the Inp_12V signal.
2. Turn on the hysteric hot-swap action by turning on the En_Hot_swap signal.
3. Wait for the supply at 12V load to be within tolerance by monitoring the Out_12V signal within 10ms. If 10ms timer expires, set En_Hot_Swap signal to 0.
4. Set the TURN_MOSFET_ON_FULLY signal on.
5. Enable the 12V load through the Start_12V_Load signal.

**Programmable Features**
This circuit offers many programmable features that make it suitable for a wide range of applications.

- Comparator thresholds can be changed to suit different backplane voltages, e.g., 12V or 24V.
- Contact de-bounce period can be changed from 50ms to 2 seconds.
- Over-current, and short circuit current levels can be set independently.
• Design can be used to implement dual hot-swap controller for dual supply backplanes using two MOSFET drivers of the ispPAC-POWR1014 device.

• Hold-off time programmable from 2 to 100ms (time during which the MOSFET should be left on under supply fault). After this period expires, the MOSFET is turned off.

The ispPAC-POWR1014A Can Integrate Other Board Power Management Functions
The hot-swap controller uses only about 25% of the ispPAC-POWR1014A device resources. The remaining resources can be used to implement power sequencing, voltage supervision, reset generation and watchdog timer functions for the board.

Applicable Power Manager II Devices
This example used the ispPAC-POWR1014A device to implement the hysteretic control hot-swap function. However, the hysteretic control can also be implemented in ispPAC-POWR1220AT8, ispPAC-POWR1014, and ispPAC-POWR607 devices.

5.3 Implementing a Negative Supply Hot-Swap Controller
Figure 5-13 shows the circuit diagram of a -48V hot-swap controller using the ispPAC-POWR607 device.

Figure 5-13. Hot-Swap Controller Circuit Using an ispPAC-POWR607 Device

The ispPAC-POWR607 controls the MOSFET (STB120NF) shown at the bottom right of the circuit diagram, for inrush current control while operating the MOSFET in its SOA. The controller monitors the circuit current using the current sense resistor shown to the left of the MOSFET. The backplane voltage and
the voltage across the MOSFET are monitored using two potential dividers of 43K and 3.3K. The 6V zener diode is used to protect the ispPAC-POWR607’s input section.

When the blade is plugged into the backplane, the ispPAC-POWR607 waits for the contact bounce to settle and then begins to charge the hold-off capacitor, using current pulses instead of a continuous current feed. The rate of current pulses is programmable to meet the MOSFET's power dissipation characteristics. Once the voltage reaches a preset threshold, the rate of current pulses is increased to hasten the charging of the hold-off capacitor. After the hold-off capacitor is completely charged, the MOSFET is fully turned on and the Power_Good Signal is activated. This signal is used to enable the DC-DC converter. The voltage across the MOSFET is monitored by the two voltage monitoring inputs of the ispPAC-POWR607. The programmable threshold set for the first voltage monitoring (Fast Charge Duty Cycle Threshold) input determines the changeover from slow charging to faster charging of the hold-off capacitor. The second threshold (End of Soft Start) indicates the completion of the charging of the hold-off capacitor and to fully turn on the MOSFET.

The ispPAC-POWR607 waits for a preset period (determined by the short circuit watchdog timer) for the voltage across the MOSFET to drop below the fast charge threshold. If the voltage across the MOSFET does not drop below the fast charge threshold, the MOSFET is turned off, indicating a fault such as a short circuit. With this implementation, the MOSFET continues to operate within its Safe Operating Area, even if a short circuit is present.

During normal operation, the ispPAC-POWR607 senses the beginning of a brownout period when the backplane voltage drops below a preset threshold and initiates an internal programmable timer of 10ms. If the power supply recovers within that time, the circuit continues to function normally. If the 10ms timer expires, the hot-swap controller classifies it as an under-voltage event and jumps to the power recycle routine, waiting for the supply to stabilize before initiating a recharge of the hold-off capacitor.

During normal operation, when a card is plugged into the backplane, the backplane supply dips momentarily. During the voltage dip period, all cards use the hold-off capacitor to remain functional. Consequently, the hold-off capacitor loses some charge. When the backplane recovers, the charge in these capacitors is replenished. This results in a brief current spike, usually less than 100μs. This should be ignored by the hot-swap controller. However, if there is a catastrophic current fault on the board, the hot-swap controller should respond to this high current and shut the MOSFET down in less than 1μs to prevent fault propagation and to prevent damages to the MOSFET. The transistor Q2 is used to protect the card when the current fault results in very high current. When the voltage across the current sense resistor exceeds 0.7V, the transistor Q2 turns on and applies a logical 0 to the digital input of the ispPAC-POWR607. The logic equation within the ispPAC-POWR607 then turns on the transistor Q3. Q3 discharges the MOSFET gate charge, resulting in turning the MOSFET off within 1μs.

Controlling Current Inrush While Operating the MOSFET in its Safe Operating Area

The top trace of the oscilloscope in Figure 5-14 shows 10ms wide, 1.5A current pulses charging the hold-off capacitor. The bottom trace is the voltage across the MOSFET while charging a 4700μF hold-off capacitor.

**Figure 5-14. Hold-off Capacitor Charging Current and Voltage Across the MOSFET**

Two of the ispPAC-POWR607’s MOSFET drivers drive the MOSFET gate. One MOSFET driver maintains the current amplitude at 1.5A, and the second MOSFET driver controls the modulation rate. In this circuit, the duty cycle was limited deliberately to one 10ms pulse every 260ms. This limits the worst-case (during short circuit) average power dissipated by the MOSFET to \(1.5A \times 48V \times 5ms / 260ms = 1.4W\).

**Hot-Swap Controller Algorithm**

- The hot-swap controller algorithm is mainly implemented in an ispPAC-POWR607 device using sequence control. However, the short circuit over current is monitored using a combinatorial logic equation because of speed.

```
If Short_ckt_Det (output of Q2) = 0 then turn on Q3 (Q3 discharges the MOSFET gate)
```

Sequence control:

1. Turn-off MOSFET and wait for contact bounce to settle.
2. Until the voltage across the MOSFET drops below 25V, charge the capacitor using 10ms wide 1.5A pulses repeated once every 260ms. If the voltage does not drop below 25V within 512ms, stop hot-swap.
3. After the voltage across the MOSFET drops below 25V, increase the duty cycle to 10ms wide 1.5A pulses repeated at a rate of 65ms.
4. Wait for the voltage across the MOSFET to drop below 1V and turn the MOSFET on fully.
5. If an over-current condition occurs, turn the MOSFET off and retry once in two seconds.

**Customizing the -48V Hot-Swap Controller**

The entire hot-swap algorithm can be implemented within the 16-macrocell PLD of the programmable hot-swap controller. Designers can customize this algorithm to suit their blade requirements. The following parameters of the programmable hot-swap controller can be customized:

- **Short circuit watchdog duration**: If the hold-off capacitor does not charge in the specified time period, the MOSFET is shut off.

- **Charging Current Pulse Duration**: The pulse width is set to guarantee that the MOSFET operates within its SOA.
- **Charging Current Pulse Frequency**: This parameter, along with the charging current pulse duration, determines the power dissipation for a given MOSFET.
- **Minimum Hold-off Time Before Recycling**: This determines the blade’s immunity to brownouts.
- **Current Sense Scaling**: This is set by the selection of the Rsense (R_S) resistor, R_1 and R_2.
- **Height of Charging Current Pulse**: Determined by the R_S resistor value, sets the amplitude of the charging current pulses.
- **Circuit Breaker Current**: Maximum current value to initiate shut off and re-start.
- **End of Soft-start Operation**: Sets the voltage at which the MOSFET is fully turned on and the Power_Good Signal is generated.
- **Transition to Fast Charge Duty Cycle**: Determines the voltage at which the charge pulse frequency is increased to safely reduce the hold-off capacitor charging time.
- **Minimum Operating Voltage**: Determines the backplane voltage below which the brownout process begins.
- **Over-Voltage Protection**: Above this voltage, the MOSFET is shut off to protect the blade circuitry.

**Applicable Power Manager II Devices**

This design is implemented using an ispPAC-POWR607 device. However, the ispPAC-POWR1014A device can also be used to implement the hot-swap controller if the design requires voltage measurement through the I^2C interface.

**5.4 CompactPCI Board Management**

Applications such as CompactPCI or CompactPCI Express use a backplane with multiple power supply rails.

Figure 5-15 shows the requirements of the hot-swap controller for CompactPCI standard backplane with voltages of +12V, +5V, +3.3V & -12V. In this design, the +5V and +3.3V rails carry the bulk of the power.
The Power Manager II ispPAC-POWR1220AT8 device has been used to implement not only the hot-swap controller but also the entire circuit board’s power management, as shown in Figure 5-15. In this design, the 5V and 3.3V hot-swap controllers use the hysteretic current control mechanism (as described in the section “Hot-Swap Controller with Hysteretic Current Limit Mechanism” on page 5-4) and the +12 and -12V use the soft-start control mechanism (described under “Hot-Swap Controller Using Soft-start” on page 5-3). The +12V rail uses a P-Channel MOSFET.

**CompactPCI Board Management Algorithm**

The hot-swap controller, after initiating the hysteretic and soft-start functions, waits for the board supplies to reach normal operating levels within the watchdog time period and then activates the Healthy# signal.
If the hot-swap function fails, the Healthy# signal is not activated and the main system does not activate the PCI card. One can then re-initiate the hot-swap function by extracting and re-inserting the board into the backplane. After all hot-swapped rails reach normal operating value, the ispPAC-POWR1220AT8 device initiates the sequencing of 2.5V and 1.8V supplies. After all supplies are stable (including the on-board sequenced supplies), the CPU reset signal (CPU_RSTb) is activated. If any supply fails, the brown_out signal is activated.

**Programmable Features**
The circuit shown in Figure 5-16 can be customized for the following:

- Over-current for 5V and 3.3V
- Sequencing of board mounted voltage
- Protecting against board faults – Turn off all hot-swap MOSFETs
- Generating other board specific power management signals
- Measuring voltage and current
- Trimming and margining of supplies

**Applicable Power Manager II Devices**
This example shows CompactPCI Express board power management functions implemented using an ispPAC-POWR1220AT8 device. If the CompactPCI Express board required the hot-swap function and minimal board management, then a ispPAC-POWR1014A device would be sufficient.
CompactPCI Express Board Management

CompactPCI Express backplanes are similar to CompactPCI backplanes. However, the 12V supply is also required to carry the bulk of the power in addition to +5V and 3.3V rails.

Figure 5-17. Complete CompactPCI Express Board Power Management

The difference between the CompactPCI and CompactPCI Express board power management implementation (Figure 5-17) is that in this circuit the 12V hot-swap uses a hysteretic current control mechanism. The +5V and +3.3V hot-swap implementation is the same as the one described in “Hot-Swap Controller with Hysteretic Current Limit Mechanism” on page 5-4. The 12V hot-swap mechanism is described in “12V/24V Hot-Swap Controller” on page 5-8.

Programmable Features

- The secondary board power management section can be completely customized to meet board management needs.
- Power rail voltage and current can be measured through I2C.
- 12V hot-swap behavior can be adjusted to meet the characteristics of any MOSFET.

Applicable Power Manager II Devices

This example shows CompactPCI Express board power management functions implemented using an ispPAC-POWR1220AT8 device. If the CompactPCI Express board required the hot-swap function and minimal board management, then a ispPAC-POWR1014A device would be sufficient.
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6.1 What is Power Rail OR’ing?

One method used to increase the reliability of high availability systems is through the use of systems that are powered by two or more (redundant) power supplies. These supplies are generated either by multiple sources or the system is connected to the main supply by the use of multiple paths. Boards connected to these redundant supplies derive a single high availability rail through the use of diodes, as shown in Figure 6-1. This arrangement is called a power rail OR’ing.

This is a simple arrangement. Only the supply that has the highest voltage drives the main board voltage. Also, if the supply voltages are roughly equal, the load power is shared between each source. If a supply fails, the load is transferred to other supplies automatically without any interruption.

Although this is the simplest and most reliable way of OR’ing supplies, this circuit has a disadvantage: it wastes power. Diodes usually drop about 700mV. If the load current is, say, 2A, the power dissipated by the diode is 1.4W. If there are ten boards in a shelf, the power dissipated is 14W, which stresses the cooling system. In addition, diodes that can dissipate more than 2W must be used. These diodes are not only expensive but also are large, requiring more circuit board area.
To minimize the power dissipation, some designs use Schottky diodes. These diodes drop about 400mV, resulting in approximately half the power dissipation. Nonetheless, the dissipated power is still too high, and Schottky diodes are usually more expensive.

Modern power OR’ing circuits use MOSFETS (Figure 6-2) to reduce the power dissipation significantly. Typical turn-on resistance of an N-channel MOSFET is about 25mΩ, so the power dissipated by this MOSFET at 2A is 100mW (2*2*25 E-3). In other words, the power dissipation is reduced by 93%.

**Figure 6-2. Power Supply OR’ing Control Using MOSFETs to Reduce Power Dissipation**

![Power Supply OR'ing Control Using MOSFETs to Reduce Power Dissipation](image)

## 6.2 Challenges of Designing a MOSFET OR’ing Circuit

When turned on, MOSFETs allow current to flow in both directions. Consequently, a voltage difference between any two rails results in a reverse current flow into the lower voltage supply rail. For example, a 1V difference between $V_{inA}$ and $V_{inB}$ can result in 20A ($1V / (0.025 + 0.025)$) flowing from the higher voltage supply into a lower supply rail. This causes overloading of supplies and, in some cases, damage to the supplies.

To prevent reverse currents, a power supply OR’ing control circuit is required. There are two methods used for preventing the reverse current:

- Monitor current through the MOSFET and turn off the MOSFET, which has less current than the threshold. Current dropping below the threshold can indicate reverse current build up in that limb. If the current in all the limbs is greater than the minimum threshold, all the MOSFETs are left turned on in order to enable load current sharing.

- Monitor the voltage difference between the rails of the input supplies and turn off the MOSFET that is connected to the lower voltage rail. When the voltage difference between the two rails is less than a diode voltage drop, then both MOSFETs are left on, the current to be shared.

The following section discusses positive voltage and negative voltage OR’ing circuits implemented using Lattice Power Manager II devices.
6.3 +5v Power Supply OR’ing (Using MOSFETs) Circuit

The circuit in Figure 6-3 shows OR’ing of two 5V supply rails, 5V_a and 5V_b. The OR’ing control algorithm is implemented in an ispPAC-POWR1014A device. The current through each limb is monitored by the ispPAC-POWR1014A device through current sense amplifiers CSA_a and CSA_b. MOSFETs Q_1 and Q_2 implement the OR’ing function. The common 5V supply rail is derived by combining the drain terminals of Q_1 and Q_2. When both MOSFETs are off, their body diodes provide an inefficient OR’ing mechanism. In Figure 6-3 the OR’d supply feeds a hot-swap controller.

![Figure 6-3. An ispPAC-POWR1014A Device Implementing Two-Rail 5V OR’ing Control](image)

The circuit starts with both MOSFETs turned off. The load is turned on by enabling the hot-swap controller. When the load starts drawing power, it automatically draws power from one of the MOSFET body diodes. If both voltages are very close, the load pulls current from both the MOSFET body diodes, and both are sensed by the respective current sense amplifiers.

The ispPAC-POWR1014A device turns on the MOSFET on a limb only if the current through that limb is above a threshold value. If the current in both rails is above their thresholds, then both MOSFETs are turned on.

The ispPAC-POWR1014A device continues to monitor the current level in both limbs. During operation, if the current through one of the MOSFETs drops below its low current threshold (due to a sudden drop of...

that power rail’s voltage), then that MOSFET is instantly turned off. When the MOSFET is turned off its body diode blocks the reverse current. Because the MOSFET is turned off when the current drops below the positive threshold, the reverse current that would be driven back into the power supply is avoided. In effect, this circuit implements OR’ing of supply rails through a proactive reverse current avoidance method.

Algorithm for Implementing OR’ing through MOSFETs

Step 1 – Wait for at least one of the rails to reach operating voltage value.

Step 2 – Enable the load or the hot-swap controller.

Step 3 – Wait for the load to turn on.

Step 4 – If the current in Limb A is greater than its turn-off threshold, turn on the MOSFET.

Step 5 – If the current in Limb B is greater than its turn-off threshold, turn on the MOSFET.

Step 6 – Wait for either of the currents in the MOSFETs that are turned on in a limb to drop below its turn-off threshold. If the current drops below the turn-off threshold, turn it off and wait for the current to increase above the turn-off threshold, then turn the MOSFET back on. Continue executing step 6.

Programmable Features

The following programmable features enable the design described above to meet the needs of a wide variety of OR’ing circuits.

• Individually program thresholds of two comparators to implement hysteresis using a logic equation for MOSFET turn on current and MOSFET turn-off current levels.

• Programmable thresholds for determining the valid input operating voltage range.

Additional Functions That Can be Integrated into the ispPAC-POWR1014A Device

• Hot-swap controller – Either soft start or hysteretic current controller.
  – One of the MOSFET drivers can be freed to implement the hot-swap controller by using the transistor circuit shown in Figure 6-4 on page 6-6.

• Integrate sequencing.

• Integrate voltage supervision, reset generation and watchdog timer functions.

Applicable Power Manager II Devices

Driving a 5V rail requires a MOSFET drive of 12V. This feature is supported in the ispPAC-POWR1220AT8, ispPAC-POWR1014 and ispPAC-POWR1014A devices.
6.4 Power Supply OR’ing of Three or More 5V Supply Rails Using MOSFETS

A ispPAC-POWR1014 device supports two MOSFET drive circuits; however, each MOSFET drive can drive gates of multiple MOSFETs simultaneously. The circuit in Figure 6-4 makes use of this feature to implement N-supply rail OR’ing through a MOSFET using one HVOUT signal from the Power Manager II device.

The operating principle of this circuit is the same as above. The only difference here is that a four-transistor circuit is used to drive the MOSFET gate, as shown in the inset block as OR MOSFET Control.

The P1 PNP transistor is turned on to enable the voltage and current from HVOUT to the gate of the MOSFET. P1 is turned on when N2 turns on, which is when the OUT pin of the ispPAC-POWR1014 is at Logic 0 (N1 is off). At that time N3 is also off. To turn the OR MOSFET off, digital output is set to Logic 0. At that time N2 turns off and N3 turns on, draining the charge stored in the MOSFET gate, which turns it off immediately.

The diode D1 is introduced in the base circuit of the N3 to delay turning on N3 compared to N1, and to turn the N3 off before N1. This avoids the condition where P1 and N3 are both on at the same time, preventing turning off the other MOSFETS in the OR circuit.
Algorithm Implementing N-channel OR’ing through MOSFETs

Step 1 – Wait for at least one of the rails to reach operating voltage value.

Step 2 – Enable the load or the hot-swap controller.

Step 3 – Wait for the load to turn on.

Step 4 – If the current in Limb A is greater than the minimum threshold, turn on the MOSFET through the corresponding digital control.

Step N – If the current in Limb N is greater than its minimum threshold, turn the MOSFET on.

Step N+1 – Wait for either the current through the limb whose MOSFET is turned on to drop below the threshold and then turn it off, or wait for the current in the limb whose MOSFET is turned off to go above threshold and then turn that MOSFET on. Continue executing step N+1.
(Steps N+1 is implemented using logic equations for all N-MOSFETs such that the circuit monitors and controls all MOSFETs in parallel.)

**Programmable Features**
The following programmable features enable the design described above to meet the needs of a wide variety of OR’ing circuits.

- Individually program the thresholds of two comparators to implement hysteresis (using logic equations) for MOSFET turn-on current and MOSFET turn-off current levels.
- Programmable thresholds for determining the valid input operating voltage range.

**Additional Functions That Can be Integrated Into the ispPAC-POWR1014A Device**

- Hot-swap controller – Either soft start or hysteretic current controller. The OR’ing circuit uses only one MOSFET drive output. The second MOSFET drive can then be used to implement the hot-swap controller.
- Integrate sequencing.
- Integrate voltage supervision, reset generation and watchdog timer functions.

**Applicable Power Manager II Devices**
Driving a 5V rail requires a MOSFET drive of 12V. This feature is supported in the ispPAC-POWR1220AT8, ispPAC-POWR1014 and ispPAC-POWR1014A devices.

**6.5 N-rail (12V/24V) OR’ing**
The operating principle of the N Rail 12V OR’ing with MOSFET is the same as that of the N-Rail 5V OR’ing with MOSFET. The difference is that the gate of the N-Channel MOSFET on the 12V rail requires higher voltage than the one supplied by the HVOUT pin of the ispPAC-POWR1014 device.

In addition to the blocks shown in Figure 6-4, Figure 6-5 shows an additional c-pump block at the bottom right corner that implements an external charge pump to generate 20V at the MOSFET gate.
Figure 6-5. N-12V Rail OR’ing through MOSFET Using an ispPAC-POWR1014A Device
Operating Principle of the C-Pump Block
The HVOUT pin of the ispPAC-POWR1014A device toggles, outputting 12V for 32μs and 0V for 8μs. When the HVOUT pin is at 0V, the capacitor C₁ gets charged to a voltage that is highest of all 12V rails through the diode D₂. When the HVOUT pin is at 12V, this voltage is then added to the capacitor (C₁) voltage and that turns the transistor P₂ on and charges C₂ through diode D₃ to approximately 20V. This voltage is then routed to the MOSFET gates through the OR MOSFET control block.

The ispPAC-POWR1014 device, like the N-rail (5V) OR’ing circuit operation, then monitors the currents through the rails and turns on the corresponding MOSFET if its current is higher than the turn-on threshold.

Algorithm Implementing N-Channel OR’ing Through MOSFETS
Step 1 – Wait for at least one of the rails to reach operating voltage value.

Step 2 – Enable the load or the hot-swap controller.

Step 3 – Wait for the load to turn on.

Step 4 – If the current in Limb A is greater than the minimum threshold, turn on the MOSFET through the corresponding digital control.

Step N – If the current in Limb N is greater than its minimum threshold, turn the MOSFET on.

Step N+1 – Wait for either the current through the limb, whose MOSFET is turned on, to drop below the threshold and then turn it off, or wait for the current in the limb whose MOSFET is turned off to go above threshold and then turn that MOSFET on. Continue executing step N+1.

(Steps N+1 is implemented using logic equations for all N-MOSFETs such that the circuit monitors and controls all MOSFETS in parallel)

Programmable Features
The following programmable features enable the design described above to meet the needs of a wide variety of OR’ing circuits.

• Individually program the thresholds of two comparators to implement hysteresis through logic equations for MOSFET turn-on current and MOSFET turn-off current levels.

• Programmable thresholds for determining the valid input operating voltage range.

Additional Functions That can be Integrated Into the ispPAC-POWR1014A Device
• Hysteretic current control hot-swap controller. The OR’ing circuit uses only one MOSFET drive output. The Second MOSFET drive then can be used to implement the hot-swap controller.

• Integrate sequencing.

• Integrate voltage supervision, reset generation and watchdog timer functions.
6.6 -48V Supply OR’ing Through MOSFETS

The circuit shown in Figure 6-6 monitors the voltage difference between the two -48V voltage rails using a simple resistive voltage divider. In the following circuit there are two rails, -48VA and -48VB. Initially the MOSFET is off and the OR’ing function is performed by the body diodes. The voltage difference between the two rails is monitored by the resistors R1 through R4. The values are selected such that when the voltage difference is greater than 0.4V, a Schottky turn-on voltage, the corresponding node A_Hi or B_Hi goes above 0.75V. The logic equation within the ispPAC-POWR607 device turns the MOSFET on and the less negative rail is turned off, preventing reverse current. If the voltage difference between the two rails is less than 0.4V, both MOSFETS will be turned on.

**Figure 6-6. Dual -48V MOSFET OR’ing Circuit Using an ispPAC-POWR607 Device**

**Programmable Features**

The values of R1, R2, R3 and R4 are selected such that there is a dead band of 0.4V about the common -48V rail. That is, if the -48VA and -48VB are within 0.4V of each other, both the MOSFETS are turned on. This dead band voltage value can be changed by selecting a different potential divider setting.

**Additional Functions That Can Be Integrated Into the ispPAC-POWR607 Device**

One of the useful functions that can be added to the circuit shown in Figure 6-6 is monitoring of -48VA and -48VB rails, as well as monitoring for fuse failure as shown in Figure 6-7. The voltage monitoring section generates two fault signals: Battery_Fail_VA and Battery_Fail_VB. These signals also become active when the corresponding fuse fails. If all the boards in the shelf show a battery failure, then it indi-
Indicates the main battery failure. However if one of the cards indicate the battery failure, it indicates a fuse fault.

Figure 6-7 shows the -48V voltage sensing circuit that uses two 50kΩ resistors (R₁ and R₂) to monitor the voltage. The voltage at the junction of R₁ and R₂ determines the current through the resistors R₂, R₄ and the transistor P₁. The ispPAC-POWR607 monitors the voltage across the resistor R₄, which is proportional to the voltage across the resistors R₁ and R₂.

The second ispPAC-POWR607 device performs the hot-swap function in hot-swappable boards. The voltage monitoring, fuse fault monitoring, MOSFET OR'ing, and hot-swap control functions can be integrated into an ispPAC-POWR1014 device. In addition, if power measurement is required, one can use an ispPAC-POWR1014A device instead of the ispPAC-POWR1014 device and use a opamp circuit to amplify the current through the circuit.

**Figure 6-7. Voltage Monitoring in Addition to OR'ing Two -48V Rails Using an ispPAC-POWR607 Device**

**Figure 6-8. -48V Rail Voltage Monitoring Circuit Shown as Vsense A and Vsense B Blocks in Figure 6-7.**

**Applicable Power Manager II Devices**
This circuit can be implemented using the ispPAC-POWR607 or ispPAC-POWR1014A devices.
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Power Feed Controllers

7.1 What are Power Feed Controllers?
In many systems, including base stations, microwave add-drop multiplexers and MicroTCA shelves, a circuit board is required to feed power to an external system. In base stations, the power is for a remote radio head; in the case of a microwave system, an external modem and an antenna on a tower require power to be sourced from the system on the ground; and in the case of MicroTCA, the power module is needed to feed power to multiple Advanced Mezzanine cards plugged into the same shelf.

In most of these cases, the power feed is required to monitor for faults such as over current and under current, as well as to provide short circuit protection. This chapter discusses -48V and 12V power feed arrangements because they are the most common. These designs can be modified to support other voltages as well.

7.2 Dual Rail -48V Supply Feed
The circuit shown in Figure 7-1 uses MOSFETs to control the power feed to two -48V rails. To prevent damage to the MOSFETs during the power feed event, the current through the MOSFET is limited using a hysteretic current control mechanism for a fixed period. After that period, the MOSFET is fully turned on and the circuit goes on to monitor the currents for over current and under current faults. There are three types of current faults that can occur in power feed circuits:

1. No current fault – If the external cable is broken
2. Over current fault- External system draws more current than normal (not dangerously high current)
3. Short circuit current fault – Dangerously high current due to a short circuit in the power feed cable

If a no-current or over-current fault is detected, the fault flag becomes active for that channel. If a short circuit is detected, the MOSFET is shut down in less than 500ns. After a fault is
detected, the circuit tries continuously to restart the power feed as long as the enable signal is active for that channel.

**Figure 7-1. The ispPAC-POWR607 Device Implements a Dual-Channel -48V Power Feed Circuit**

### Circuit Operation

The circuit generates two channels of power, -48V_1 and -48V_2, through the MOSFETs Q1 and Q2. The open circuit current limit (the value below which the circuit is assumed to be open) is set by the resistors R_S1 and R_S2. The monitoring threshold voltage of VMON1, VMON2, VMON3 and VMON4 pins of the ispPAC-POWR607 device are set to 0.075V. The values of series resistors R_S1 and R_S2 are selected such that at the lower current limit the voltage dropped across the R_S1 and R_S2 is 0.075V. The over current limit is set by the resistors R1 and R2 for the power feed 1, and R3 and R4 set the over current limit for power feed circuit 2. R1 and R2 are selected such that \( R1 / (R1+R2) = 0.075V \) when maximum current is flowing through the R_S1 resistor. In other words, \( I_{max} * R_S1 * R1 / (R1+R2) = 0.075V \). The values of R4 and R5 are also selected using the same equation.

When the enable signal is activated, the circuit turns on the MOSFET with the current limited to a value determined by the programmed over current limit for a period determined by the Timer 1 for power feed 1 and Timer 2 for the circuit 2. After Timer 1 or Timer 2 expires, the corresponding MOSFET is fully turned on and the circuit starts to monitor for over and under current. Note: The selected MOSFET should be able to handle the maximum current for the duration determined by Timer 1.

After the MOSFET is fully turned on, if an over or under current condition is detected, the MOSFET is turned off through the transistor N1/ N2, and Timer 3 and Timer 4 (retry timers) are started. When the retry timer expires, the MOSFET is turned back on with an initial hysteretic control, as before.

If the circuit detects a very high current (as detected by 0.7V across the series resistors R_S1, R_S2) the transistors N3, N4 pull down signal SC1 and SC2. These signals are connected to the digital inputs of the ispPAC-POWR607 device. The logic equations within the ispPAC-POWR607 device shut the MOSFET
Q₁, Q₂ down immediately through N₁, N₂ (in less than 500ns) and the retry timer is started. After the retry timer expires, the transistor N₁, N₂ that shuts down the MOSFET is turned off.

The Fault 1 and Fault 2 signals are controlled by a routine that monitors over and under current conditions in each of the circuits. When an over current fault occurs, the corresponding flag is set to high. Along with that, the UC_OCb (under current and over current flag) will be set to logic 0. If an under current event is detected, the UC_OCb signal will be set to Logic 1. If the fault exists in both circuits 1 and 2, then the status flag toggles between the conditions once every 8ms.

**Algorithm**

The design is implemented using logic equations to provide independent operation on each of the channels. The following algorithm makes use of simple logic equations. There are five equations that control the power feed for one of the circuits. All equations are active in parallel. For example, the short circuit monitoring section is always active and shuts the MOSFET down if a short circuit occurs when any one of the other four equations are operational. This algorithm (set of five equations) is repeated for the second channel power feed.

The fault indication flags are controlled by the algorithm implemented in the sequence controller section of the algorithm.

1. **Equation 1 circuit 1** – Waits for the enable signal to become active to begin the hysteretic controlled power feed. The Power feed is expected to be complete within a preset period set by the hysteretic control timer. The hysteretic control timer is also started when the enable signal gets activated and starts the hysteretic control timer. After the initial hysteretic control timer expires, the MOSFET is turned on fully. If a fault is detected, this equation waits for the retry timer to expire before initiating the hysteretic power feed.

2. **Equation 2 circuit 1** – Waits for a short circuit condition detection. When a short circuit is detected, this equation turns the MOSFET off through a fast asynchronous reset signal.

3. **Equation 3 circuit 1** – Monitors for over or under current conditions. When such a condition is detected, the MOSFET is turned off and a retry timer (2 seconds) is started.

4. **Equation 4 circuit 1** – Monitors for the retry signal and the enable signal to begin the 5ms hysteretic control timer. This hysteretic control timer is used by equation 1.

5. **Equation 5 circuit 1** – The fault flag is cleared to recapture the fault condition when the normal operation begins.

The fault conditions are reported by the sequence controller.

1. When the circuit 1 is operating normally and a fault has not already been reported, check on circuit 1 for over or under current fault on circuit 1 and, if a fault is detected, activate the Fault_1 output.

2. If it is an over current condition or short circuit condition, turn the UC_UCb flag off.

3. When the circuit 2 is operating normally and a fault has not already been reported, check on circuit 2 for over or under current fault on circuit 2 and, if a fault is detected, activate the Fault_2 output.
4. If it is an over current condition or short circuit condition, turn the UC_UCb flag off or else turn it back on.

**Programmable Features of this Circuit**

1. The over-current, no-current conditions can be set by selecting the R_S1, R_1 and R_2 for circuit 1 and R_S2, R_3 and R_4 for circuit 2.

2. Program the hysteretic current timer duration to meet the MOSFET’s safe operating area. Note: Both over current and the duration of hysteretic control duration are determined by the safe operating area of the MOSFET.

3. Retry duration can be set independently for both circuits.

**Applicable devices:**

This circuit uses the ispPAC-POWR607 device.

**7.3 Three Channels of a +12V Power Feed System**

In some applications, two or more channels of 12V power feed are required. For such applications, the following three-channel power feed circuit is used. More than three channels of power feed requires multiple implementations of the following circuit. This design is modular in order to address implementations requiring less than three channels of power feed so that free resources can be used for other payload power management functions.
Figure 7-2 shows an ispPAC-POWR1014A device used to feed 12V to three channels. Each of the channels can be controlled independently. For each channel this circuit offers under current, over current and short circuit current protection, along with fault indication. After the fault is detected, the circuit retries continuously with a programmable delay between retries. The power is controlled through a MOSFET and the circuit ensures operation of the MOSFET in its safe operating area. All voltage and current during the operation can be measured using the on-chip ADC through I²C.

**Circuit Operation**

The ispPAC-POWR1014A device derives its power from the input 12V supply. The operating principle of the external charge pump is as follows (Figure 7-2):

The ispPAC-POWR1014A HVOUT pin toggles between 12V (for 32μs) and 0V (for 8μs) cyclically. When the HVOUT1 pin is at 0V, the capacitor C₁ gets charged to backplane voltage of 12V through the diode D₂. At this time the transistor P₂ is off. When the HVOUT1 toggles up to 12V, the C₁ voltage is added to the HVOUT1 pin voltage, resulting in the generation of approximately 24V at the junction of C₁ and D₂. This voltage turns P₂ on and charges the capacitor C₂ to about 22V through the diode D₃. This voltage is sufficient to turn on the MOSFETs Q₁ through Q₃.
Once on, the device begins toggling the HVOUT1 pin to generate about 22V at the CPOUT pin and waits for a high on any of the 3 EN signals. After receiving the En signal, the corresponding MOSFET is turned on using the dual current level hysteretic control mechanism while monitoring for the output voltage.

When, say, the EN_1 signal is turned on, the OUT3 pin is set to logic 0. This turns off the transistor N1, which in turn turns on the transistor N2. The transistor N2 provides the gate drive for the transistor P1, turning it on. The transistor P1 then applies 22V from the CPOUT pin to the gate of the MOSFET Q1 through a resistor, turning it on.

If a supply fault is detected, the OUT3 and the OUT4 pins are set to Logic 1. This turns off the transistor P2 and turns on the transistor N4. The N4 then discharges the MOSFET gate to turn it off immediately.

When power feed operation begins the MOSFET Q1 is turned on. As a result, the current through the MOSFET starts to increase significantly. This results in the MOSFET operating outside its safe operation area (SOA), resulting in damage to the transistor. To avoid that damage, the MOSFET is turned on with a hysteretic current control. The following section describes the MOSFET current control operation.

**Dual Current Level Hysteretic Control**

Figure 7-3 shows the safe operating area for a MOSFET. This is a Log-Log graph with voltage across the MOSFET (V_{DS}) on the X-axis and current through the MOSFET on the Y-axis. The dotted lines represent the safe operation envelopes for different pulse width durations. When the power is applied to the MOSFET and begins to turn on, the point of operation is at the right bottom side of the graph. The red line indicates the current limit controlled by the hysteretic controller implemented in the ispPAC-POWR1014A device. The current through the MOSFET is limited initially to the lower level. This current charges the capacitor on the load, reducing the voltage across the MOSFET. When the voltage across the MOSFET drops to approximately its mid point (for example, 6V), the current is doubled while operating completely within the safe operation area. The first set point current and the second set point values are determined by the safe operation area of the MOSFET as shown by the red line in Figure 7-3.

*Figure 7-3. Safe Operating Area of MOSFET – (IRF7832)*
After the voltage at the load reaches the minimum operating value, the MOSFET is turned on fully. The circuit then begins to monitor for over current and no current faults. When a fault is detected, the corresponding fault output is activated and the circuit waits for the retry delay. During the retry waiting period, the fault indication is maintained. After the retry period, the circuit begins to restart the MOSFET current. If the output voltage does not reach its minimum operating value within 10ms, the fault flag is turned on and the circuit waits for another retry period.

**Algorithm for Each Power Feed Channel**

1. Wait for enable signal.

2. Start power feed and wait for output voltage to reach its minimum operating level within 10ms. This step turns on the MOSFET with two current settings.

3. If the output voltage is within its safe operating level, turn the MOSFET on fully and begin monitoring the output current for over and under current faults. If a fault is observed, flag the fault, then turn the MOSFET off and jump to retry timer.

4. Wait for the retry timer to expire, then jump to step 1 to begin the power feed process.

5. During the four step sequence above, the following operations are performed in parallel:
   - 12V Power feed control with two-step current feed.
   - Monitor for short circuit current and turn the MOSFET off within 500ns when a fault is detected.
   - Monitor for the enable signal and turn off the MOSFET.

**Programmable Features of Power Feed**

The following section outlines all the programmable features of this design:

1. Customize the design to meet any MOSFET characteristics: two current levels can be programmed. If the design requires only one current level, the corresponding equation can be changed easily.

2. If faster turn-on times are required, the circuit can be modified to pump larger currents during start up. These new currents can be independent of the min and max operating current limits.

3. The timer used to monitor the initial supply turn-on period is programmable. This design used 10ms. It can be increased or decreased, depending on the design’s requirement.

4. Retry period – this design used a two second timer. It can be programmed from 32µs to two seconds in 122 steps.

5. Over current and under current setting – this can be changed simply by altering the threshold of the comparator.

**Integrating Other Payload Power Management Functions into the ispPAC-POWR1014A Device**

This circuit uses the ispPAC-POWR1014A device to implement three channel 12V power feed functions. Each channel uses three VMON signals, one digital input signal and four output signals. If the circuit requires fewer power feed channels, that portion of the design can be removed and the free resources can be used to integrate other payload power management functions, such as sequencing, monitoring and
watchdog timers. This design can also be exported to a ispPAC-POWR1220AT8 device to implement the three channel power feed functions along with other payload power management functions.

**Applicable Power Manager II Devices**

This design used the ispPAC-POWR1014 device. However, the power feed algorithm can be integrated into a ispPAC-POWR1220AT8 device, or an ispPAC-POWR607 device can be used to implement the power feed algorithm for each channel.

### 7.4 2-Channel +12V & 3.3V Power Feed With MOSFET OR’ing

In applications such as MicroTCA, the power module is required to implement 16 channels of 12V power feed circuits. Each channel provides power to an Advanced Mezzanine Card (AMC) slot. When an AMC is plugged into the back plane, the power module turns on the 3.3V to power the AMC’s management module. The management module then communicates with a shelf manager, which then orders the power module to turn-on 12V. In some cases, the 12V supply is turned on along with the 3.3V supply and the circuit does not wait for an independent payload power enable signal. The power module then begins to monitor for over current and, if an over current condition is detected, the MOSFET is turned off. During system operation, if the AMC card is extracted the Power Module is required to turn the power off within 100μs.

For reliability purposes, the 12V and 3.3V supplies are sourced from two different power module cards. Both of these supplies are OR’d on the backplane. At any given time only one of the power modules supplies power to the backplane. The standby power module sets its voltage to a value lower than the online module. To avoid wasting power, MOSFETs are used to provide OR’ing functionality. A detailed description of the MicroTCA power feed standard is beyond the scope of this document.

The circuit in Figure 7-4 shows how a ispPAC-POWR1014A device can be used to implement a two-channel power feed.
**Circuit Operation**

Figure 7-4 shows the circuit required to implement one channel of 12V and 3.3V power feed. The 12V power feed is controlled through two MOSFETs, the Pass device (Q₁) and the OR’ing (Q₂) device, shown at the top right section of the circuit. The 3.3V power feed is controlled through a P-Channel MOSFET Q₃ using the transistor N₃. When the Enable# signal is active, the 3.3V supply is turned on through the MOSFET Q₃. Subsequently, when the Payload_On signal becomes active, the 12V power is fed to the circuit through the Pass MOSFET Q₁. The pass MOSFET Q₁ is turned on using the two-current hysteretic control mechanism. Because Q₁ is on the 12V rail, its gate voltage should be at about 20V when it is turned on. The 20V gate drive is generated through the external charge pump implemented using C₁, D₁, P₂, D₂ and C₂ (the circuit operation described in “Dual Current Level Hysteretic Control” on page 7-6), to ensure that the MOSFET is operated within its SOA. Once the output power is above its minimum operating level, Q₁ is fully turned on and the OR’ing MOSFET Q₂ is turned on or off depending on the EMMC primary or redundant status. This ensures that only the primary supply wins the OR’ing arbitration. When an over current event is detected, the ispPAC-POWR1014A device shuts Q₁ and Q₂ down through the transistor N₁.
During Operation

1. If the output supply drops below the minimum threshold (probably because the on-line supply has failed), the standby device turns on the OR’ing MOSFET $Q_2$ and the primary device turns the OR’ing MOSFET off and flags the EMMC Alert signal. This ensures that the AMC does not see its 12V supply voltage dip below its operating level.

2. The current in the 12V supply is also monitored for fault. If the current exceeds the maximum operating level, the Pass MOSFET is turned off, activating the EMMC Alert signal.

3. Before the extraction of the AMC from its slot, the AMC usually sends a signal to the shelf manager. The shelf manager then deactivates its payload power supply by disabling the Payload_On signal. When the payload signal is turned off, the user can extract the AMC from its backplane. Subsequently, when the AMC is extracted, the enable signal gets deactivated and the 3.3V supply feed to the AMC is turned off within 100$\mu$s. In some cases, the enable payload voltage signal does not exist. In such cases, the design can be modified to support only Step 4.

4. In the case of an accidental AMC card extraction process, both 12V and the 3.3V supplies are turned off at the same time within 100$\mu$s from the time the enable signal becomes inactive.

ispPAC-POWR1014A (MicroTCA) Power Feed Algorithm

1. Wait for the enable signal, and when it becomes active turn the 3.3V supply on.

2. Wait for the Payload_On signal and turn 12V on. This can be modified easily to turn 12V on when the enable signal is activated. If the 12V does not turn on within 10ms, turn 12V off and report the fault.

3. Turn OR’ing MOSFET on if the card is primary; otherwise, turn the OR’ing MOSFET off.

4. Start to monitor the following and take action:
   a. Current – Should be lower than the over current limit. If the current is more than the over current limit, shut the Pass MOSFET off and flag the error to EMMC.
   b. Output voltage – If the voltage is not higher than the lower threshold for primary, then turn the OR’ing MOSFET off and report the error. If the payload voltage is higher than the over-voltage limit, turn the Pass and OR’ing MOSFETs off and report the error to the EMMC.
   c. If the card is configured as secondary or redundant, and if the voltage is lower than the minimum primary voltage, turn the OR’ing MOSFET on and report the error back to EMMC.
   d. If the enable signal becomes inactive, turn the Pass and OR’ing MOSFETs off immediately.
   e. If the primary becomes secondary during operation, turn the OR’ing MOSFET off and monitor for lower than allowed voltage to turn the MOSFET on.
   f. If the secondary becomes primary, turn the OR’ing MOSFET on and start monitoring for a higher than allowed voltage range.
Programmable Features

- The power feed turn on monitor duration can be programmed to meet the requirements of different MOSFETs.
- The maximum value of the output current can be altered by reprogramming the ispPAC-POWR1014A device’s current monitor thresholds.

Other Functional Enhancements

- The voltage and current values can be measured through I²C.
- Not all MicroTCA implementations use all of the features specified in the standard. In such cases, one can keep the OR’ing MOSFET off when the current is below a lower threshold limit. This protects against reverse current flow from the secondary when its voltage is higher than the primary.

Applicable Power Manager II Devices

While up to four channels of Power Feed can be implemented in a ispPAC-POWR1220AT8 device, an ispPAC-POWR607 device can be used to power a single channel.
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8.1 What is Voltage Margining?

Margining is a test step that ensures a board is operational across the input variable range. A voltage margining test ensures that the board is functional across the operating range of its onboard and input supplies. Circuit boards are also subject to other margining tests such as temperature, timing and noise.

For example, if the allowed tolerance of input supply is ±10%, the voltage margining test ensures that the board is functional when the input supply is at its margin-high (nominal voltage + 10%) value and when its supply is at margin-low (nominal voltage -10%) value. If the board has a number of board-mounted supplies, then the margining test should also cover the variation of individual board-mounted supplies.

Semiconductor devices typically operate slowest when their operating temperature is at its highest value and applied voltages are at their lowest. Similarly, these devices are fastest when the operating temperature is at its lowest and the voltages are at their highest. To ensure that the design is stable across temperature and voltage, designers subject their circuit boards to high temperature in an environmental chamber with the operating voltages dialed down, and then check the operation at colder temperatures with their voltages dialed up. This is called 4-corner testing.

Margining tests typically are conducted during board debug. In some cases, Quality and Reliability departments will require margining before they will approve manufactured boards.

8.2 Voltage Margining Implementation

Figure 8-1 shows a DC-DC converter with a resistor connected to its Trim/Feedback Node. The value of this resistor typically determines the nominal output voltage value of the DC-DC converter.
DC-DC converters usually require standard resistor values to set their output voltage to a standard value – e.g., 3.3V, 2.5V, 1.5V. To change the output voltage by ±5% of their nominal operating voltage, designers use either a potentiometer for each of the DC-DC converters or a series parallel combination of standard resistor values. One has to manually implement the resistor change to all the boards that will be subject to testing in an environmental chamber.

Some disadvantages of manually altering resistor values for margining:

• Increased Delay - finding resistor values that accurately alter the output voltage often require a series and/or parallel combination of standard resistors that must be manually soldered. Different resistor combinations for each of the supplies must be found. Sometimes the board failures in the environmental chamber could be due to bad solder joints caused by manual soldering. Even if a potentiometer is used, the moisture in the environmental chamber creates contact problems that delay the margin test.
• Manually soldering a resistor for margining cannot be used for automated reliability testing.
• Due to accuracy requirements, manual methods cannot be used for margining the low core supply voltages of modern VLSIs and CPUs.

8.3 What is Trimming?

Modern circuit boards require multiple DC-DC converters with low voltages (1.2V or less) with high current capacity. A specification of 10A to 20A at such low voltages is not uncommon. In addition, ICs require very tight output voltage regulation of approximately 1.5% or less to ensure that there is enough headroom to meet the dynamic current requirements of the CPU/ASIC without violating the input voltage specs.

Trimming is the process of accurately setting and maintaining the output voltage of a DC-DC converter close to a pre-determined value across voltage and temperature. Margining is a special case of trimming.

Trimming also uses the same mechanism shown in Figure 8-1 to set a given voltage. However, to meet accuracy requirements of 1.5% or better, DC-DC converters use very high accuracy (0.1% or better) trim resistors to set the output voltage. In some cases, laser trimmed resistors and compensating resistors are used to allow for converter to converter output voltage accuracy differences.

As can be seen, when the DC-DC converter is required to meet high accuracy demands, cost increases significantly. In some cases, digital power converters are used to meet these high power and high current demands. These DC-DC converters are more expensive, as they require ADCs, DACs and accurate voltage references.
Typical Applications That Require Power Supply Trimming

Trimming is required for circuit boards using ICs that require low supply voltages (1.2V or lower) with high current ratings (5A or more).

For example, a 1.2V DC-DC converter should guarantee a maximum of ±5% (±60mV) variation under all of the following conditions:

- No-load to full-load average current variation
- Output voltage ripple
- Dynamic power demands by the IC during different average current levels
- Component tolerances during manufacturing

In general, to meet the voltage device spec under all of the above conditions safely, the DC-DC converter requires an initial operating voltage accuracy of 2% or better. These high accuracy, low voltage supplies are usually more expensive and require high precision resistors to set the voltage.

Alternatively, the accuracy of a conventional lower cost DC-DC converter can be improved by using an external trimming mechanism. The next section describes trimming using the Lattice Power Manager II IC.

8.4 Trimming and Margining – Principle of Operation

Figure 8-2 below shows a Lattice Power Manager II device implementing trimming and margining functions for an analog DC-DC converter.

![Diagram of supplies trimmed and margined](image)

On the top portion of Figure 8-2 is a DC-DC converter supplying power to its load. The output voltage is determined by the components used in its feedback circuitry. The Power Manager II device at the bottom measures the voltage using the on-chip ADC though differential sense inputs. The Power Manager II can increase or decrease the output voltage of the DC-DC converter by increasing or decreasing the voltage or current applied to the DC-DC converter’s feedback node, using its on-chip DAC. For some DC-DC converters, increasing the feedback node current or voltage reduces its output voltage.
A set point register in the Power Manager II holds the required voltage value at the load. Once every 580µs the Power Manager II device measures the voltage at the load using its on-chip ADC. The digital output of the ADC is compared against the set-point register contents. If the load voltage is higher, the DAC contents are decremented, which in turn reduces the voltage applied to the feedback node of the DC-DC converter. If the load voltage is lower, the DAC contents are incremented, applying higher voltage to the node. This is called the closed loop trim mechanism.

It is possible to break the closed loop trim and load the DAC register directly through the I²C bus. This method is used to implement margining. An external microprocessor directly loads a pre-selected DAC value into the Power Manager II, which will result in changing the output voltage by, for example, ±5%. The microprocessor can also measure the output voltage of the DC-DC converter using the Power Manager II’s ADC, and tweak the output voltage up and down as needed to implement closed loop margining.

In a circuit board, there typically are multiple types of supplies providing different supply voltages. These individual supplies require different current levels to be injected into their feedback nodes. This in turn requires a unique resistor network for each type of DC-DC converter to be connected between the Power Manager II and the DC-DC converter feedback node.

The next section briefly describes the Power Manager II’s architecture blocks and then explains the details of designing a resistor network connected between the DC-DC converter feedback node and the Power Manager II DAC output.

**Power Manager II TrimCell Architecture**

The DAC in Figure 8-2 stores the DAC codes for nominal output voltage, as well as for margining up and down. For example, to support margining (for example ±5%) and trimming of a low voltage set-point (for example 1.2V ±10mV), the three individual DAC values must be stored in different DAC registers. The Power Manager II device supports six registers for each DAC. The block that includes the DAC and its associated registers is called a TrimCell. Figure 8-3 is a TrimCell block diagram.
Six DAC registers are divided into four hardware addressable groups called Voltage Profiles. Of these six DAC codes, four are stored in on-chip EEPROM memory. The two remaining registers are volatile. One of the volatile registers can be loaded directly via the I²C interface. The second register is controlled by the closed loop trim circuit. Voltage Profiles 3, 2 and 1, when selected by either the external hardware pins or internally by the PLD, load the corresponding codes stored in the EEPROM memory into the DAC. With this feature one can margin each supply high or low using the on-chip PLD, or through the hardware pins of the Power Manager II device. While operating in these profiles, the Power Manager II is said to be operating in an open-loop; that is, the DAC register contents are static and are not adjusted during operation, depending on the actual DC-DC converter output voltage.

To support the controlling of output voltage to a very high degree of accuracy (Set-point voltage ±10mV), the Profile 0 should be used. There are three modes of operation in Profile 0:

1. Open Loop operation with the DAC code stored in the E²CMOS® configuration memory. Operation in this mode is similar to that of the profiles 1, 2 and 3.

2. Open Loop/ External Closed Loop operation – Load the I²C DAC register via the I²C bus. This mode of operation is used by an external microcontroller to fine tune the output voltage, depending on the DC-DC converter’s actual output voltage. This is called an external closed loop mode of operation.

3. Closed Loop Trim – This mode of operation is used to trim a given DC-DC converter output voltage accurately. Tight control of the output voltage is maintained by the on-chip closed loop control circuitry. Closed loop circuitry gets activated once every 580µs. It can also be programmed to be activated at a slower rate: 1.15ms, 9.2ms or 18.5ms. When activated, the on-chip closed loop control circuitry measures the DC-DC converter output voltage and compares it to the value stored in the set point register. Depending on the DC-DC converter’s output voltage excursion, the closed loop circuitry increments or decrements the DAC contents in a way that counters the output voltage excursion.
direction. The ispPAC-POWR1220AT8 device supports eight TrimCells in its TrimBlock, as shown in Figure 8-4.

**Power Manager II Integrates Multiple TrimCells**

The ispPAC-POWR1220AT8 device supports eight TrimCells in its TrimBlock, as shown in Figure 8-4.

Each of the TrimCells can be programmed independently to control a DC-DC converter. The Voltage profile selection is common to all TrimCells and is controlled by either the hardware control pins (VPS [0:1]) or through the on-chip PLD.

*Figure 8-4. The ispPAC-POWR1220AT8 Device Provides Eight TrimCells in its Trim Block*

When the Voltage proPOWR file is set to, for example, 3 in Figure 8-4 shown above, the DC-DC1 converter outputs 0.95V (5% below the normal operating voltage of 1V), while the DC-DC 2 converter outputs 1.14V (5% below the 1.2V nominal), and so on.

When the voltage profile is set to, for example, 1, the DC-DC1 converter outputs 1V+5%. The DC-DC2 converter outputs 1.2V + 5%. This method is used to implement margining.
When VPS [0:1] = 0 the DC-DC 1 converter outputs 1V and the DC-DC2 converter outputs 1.2V. However, TrimCell 0 maintains the DC-DC converter output voltage using the on-chip closed loop control mechanism, while TrimCell1 uses an external microcontroller to maintain the voltage at 1.2V.

**Closed Loop Trim - Mode Operation of TrimCell**

Figure 8-5 shows the connection between the TrimCell and the DC-DC converter when configured to operate in closed loop trim mode. The resistor between the Trim pin and the DC-DC converter Trim_in pin converts the voltage applied by the DAC into a current added to the Trim summing node of the DC-DC converter. The ADC is used to measure the DC-DC converter voltage. The three-state comparator compares the ADC measured value with the set-point and the output increments, decrements or holds the content of the closed loop trim register as is.

**Figure 8-5. The ispPAC-POWR1220AT8 Device Closed Loop Trimming Mechanism**

When the Power Manager II device is powered on, the DAC output voltage starts at the bi-polar zero value. The bipolar zero voltage is determined by its offset voltage setting 0.6V, 0.8V, 1V and 1.25V. This results in starting the DC-DC converter output voltage very close to its nominal value. Using this value, all supplies are sequenced. Once the supply sequencing is complete, the closed loop trimming process is activated.

The closed loop trimming circuitry operates on each of the TrimCells in a cycle. The closed loop trimming cycle can be activated using a programmable timer and can be set to 580μs, 1.15ms, 9.2ms or 18.5ms. The closed loop trim circuitry consists of the ADC, three state comparator, set point register, channel polarity controller, the control loop register increment/ decrement control and the DAC. During a trim cycle, the closed loop trim circuitry performs the following functions for each of the TrimCells:

1. Measures the voltage of the DC-DC converter differentially through the ADC.
2. Compares the output of the ADC with the set point register. If the polarity is set as positive, the following are the effects of the comparison:
   a. If the DC-DC converter voltage is higher than set point, decrement the contents of the closed loop trim register.
b. If the DC-DC converter voltage value is less than the set point register value, the closed loop trim register contents are incremented.

c. If the ADC value is the same as that of the set point register, maintain the closed loop trim register value.

If the polarity set is negative, the incrementing and decrementing register in steps a. and b. above are reversed.

Closed loop trimming ensures that the voltage at the load is accurate within ±10mV from the set-point value. This error includes the maximum ADC measurement steady state error and the DAC quantization error. According to the datasheet, the maximum ADC error (including its gain, offset, INL and DNL across process, voltage and temperature) is 8mV.

The error from the DAC is due to its step size. This error is calculated as follows:

Usually the resistors between the DAC and the DC-DC converters are calculated such that the full scale (128) swing of DAC results in swinging the output voltage of the DC-DC converter by 5%. This means that each step of the DAC code results in an output voltage step of 5% / 128 ~ 0.05%. For a 3.3V supply, the voltage variation due to a single step of DAC code results in changing the output voltage by 3.3*0.05/100*128 = 130µV (approximately). In effect the major error component is the ADC error. Errors due to DC-DC converter components, DC-DC converter accuracy, etc. are compensated for by the closed loop trim mechanism, which maintains the output voltage accurately.

**Closed Loop Trim and Closed Loop Margining Using a Microcontroller**

Figure 8-6 shows the configuration used for closed loop trimming with a microcontroller. Here the microcontroller measures the DC-DC converter output voltage periodically, using the on-chip ADC through the I²C bus. The microcontroller then algorithmically calculates the new DAC value depending on the DC-DC converter voltage and loads the new DAC code through the I²C interface.

The microcontroller-based margining is implemented entirely through the I²C bus and uses profile 0 in the Power Manager II. To implement closed loop margining, the microcontroller loads the starting DAC code into the DAC register via I²C and waits for the ADC voltage to stabilize. Depending on the stabilized voltage value, the microcontroller increments or decrements the DAC code. This method enables setting and controlling the margined voltage accurately.
Interfacing Power Manager II with a DC-DC converter

Interfacing a DC-DC converter with the DAC requires that the DC-DC converter output voltage is at its nominal value when the DAC register value is at its bipolar-zero voltage in Profile 0. It also requires that the DAC maximum or minimum code results in swinging the DC-DC converter voltage to its margin voltage value through appropriate current injection into the feedback node.

The resistor values also should take into consideration the type of feedback node arrangements used in DC-DC converters, their internal reference type (current/voltage), and type of feedback. To map all types of DC-DC converter variables to the DAC output voltage swing, a number of resistor network topologies, shown in Figure 8-7 through Figure 8-11 are required.

Figure 8-7 shows a typical resistor network between a Power Manager II device and a DC-DC converter. As discussed earlier, the ispPAC-POWR1220AT8 device can monitor and trim up to eight DC-DC converters individually. The trim circuit of the Power Manager interfaces to different types of DC-DC converters through a resistor network, as shown in Figure 8-7.

The resistors R₁ and R₂ and R₃ determine the starting voltage of the DC-DC converter. This is equivalent to connecting a resistor to ground from the trim pin. The values of these resistors are selected such that the voltage at the node between R₁ and R₃, is equal to the DAC voltage at power up.

The values of these three resistors are calculated by the PAC-Designer software using the following inputs:

1. Type of DC-DC Converter. There are four types of DC-DC converters:
   a. Fixed voltage
   b. Output voltage programmable through a resistor to ground connected to its trim input
   c. Output voltage programmable through a resistor to the output voltage terminal
   d. Output voltage is determined by two resistors connected from its feedback node output voltage terminal and to ground
2. Nominal operating voltage
3. Margining voltage range in positive and negative directions

*Figure 8-7. Resistor Network Topology #1 Connecting a TrimCell to a DC-DC Converter*

Not all DC-DC converter types require the same resistor network of R1, R2 and R3 as that shown in *Figure 8-7*. The other possible types of resistor networks generated by the PAC-Designer software are shown in *Figure 8-8*, *Figure 8-9*, *Figure 8-10* and *Figure 8-11*.

*Figure 8-8. Resistor Network Topology #2*

*Figure 8-9. Resistor Network Topology #3*

*Figure 8-10. Resistor Network Topology #4*
Designing Trimming and Margining Networks using PAC-Designer Software

Determining the required resistor topology involves finding a solution for a number of nodal equations and an understanding of the error amplifier architecture of the DC-DC converter. In addition, the design can be iterated until the solution yields standard resistor values.

The PAC-Designer software automates the process of determining the resistor topology while using standard resistors in the resistor network. Calculating the resistor values shown in Figure 8-7 through Figure 8-11 using the PAC-Designer software is a two-step process:

1. Create a DC-DC Converter Library using the DC-DC converter’s feedback and trim section characteristics – This uses a few parameters commonly specified in a DC-DC converter datasheet.

2. Associate a DC-DC converter to a TrimCell and calculate the resistors for a given output trim and margin voltage specification for that DC-DC converter.

Creating a DC-DC Converter Library Entry

1. To create a DC-DC converter library entry, open the ispPAC-POWR1220AT8 design and click on the button ‘DC-DC’ as shown in Figure 8-12 to open the DC-DC Model Selection menu. Click the <New> button, enter the name of the DC-DC module (example - Murata_1V2_POL) and click on <Next> to open “Select the DC-DC Converter Type” dialog box.
2. The “Select the DC-DC Converter Type” dialog box shows four types of DC-DC converters:

a. **DC-DC Converter with Trim-up & Trim-down** – This DC-DC converter usually is available as a module with a fixed voltage. These supplies can be margined up and down by connecting a resistor to GND or to VOUT

b. **DC-DC Converter with Programmable Output Voltage** – The output voltage of these DC-DC Converters is set by connecting a resistor from trim pin to ground. The value of the resistor determines the output voltage.

c. **Programmable DC-DC Converter with Rtrim connected to VOUT** – The output voltage of these DC-DC Converters is set by connecting a resistor from its trim pin to its Vout terminal. The value of the resistor determines the output voltage.

d. **The Discrete Implementation** – Represents a class of DC-DC converters whose output voltage is determined by two resistors: one between the Vout terminal to the feedback node and the second between the feedback node and the ground.
Refer to the DC-DC converter datasheet to select the type of DC-DC converter and click on the <Next> button.

3. This section describes configuration for each type of DC-DC converter.

Fixed voltage – DC-DC Converter with Trim Up and Down Supply

This type of DC-DC converter is usually a module and is designed to provide a fixed voltage. The following message box (Figure 8-14) is used to create the library entry.
These supplies have a trim pin. This pin is used to margin the supply up by 5-10% or margin the supply down by 5-10%.

Nominal output voltage – This is the normal operating voltage of the DC-DC converter when its trim pin is open. This is its normal operating state.

Next, there are two fields under the headings “Example 1 R to GND”, “Example 2 R to GND” and “Example 3 R to Vout.” Examples 1 and 2 are conditions used to generate a margin voltage that is different than the nominal voltage. Different target voltages will require different resistor values. These values are provided in the DC-DC converter datasheet, usually in a table format. Some datasheets provide a formula to calculate these resistors. Enter the values of the target output voltage and the values of the target resistors that are connected between Trim and GND pins into the required fields.
The third column requires the value of the resistor to be connected between the trim pin and the Vout pin of the DC-DC to achieve the corresponding output voltage. Input the resistor value and voltage values in the required fields. Again, these values are found in the DC-DC converter datasheet.

After entering these values, enter the necessary comments that describe the use of the DC-DC converter and click on the <save> button followed by the <Finish> key. In this case the software creates a library element called “Murtata_1V2_POL.

*Programmable Voltage with Resistor Connected from Trim pin to Gnd*

*Figure 8-15* shows the dialog box that appears when the programmable voltage DC-DC converter is selected.

*Figure 8-15. Reference Voltage/Current for the DC-DC Converter*

All DC-DC converters use some type of reference voltage or current to set the output voltage. The value of the reference voltage ‘Vref’ is shown either in the specifications section of the datasheet or in its output voltage calculation formula. Sometimes, the datasheet shows the architecture of the error amplifier with the value of Vref.
In some cases, the DC-DC converters use current reference instead of a voltage reference. The current reference value is accompanied by a parallel resistor. Again, some DC-DC converter datasheets show the equivalent circuit in the error amplifier section. After entering the Vref or Iref & Rref values, click on Next to get the dialog box shown in Figure 8-16.

Figure 8-16. Configuring the Programmable Voltage DC-DC Converter Library Entry

The output voltage of these types of DC-DC converters is determined by the resistor connected from their Trim pin to Gnd.

To complete this dialog box, refer to the DC-DC converter datasheet for a table that maps the resistor values connected between the trim pin and GND to the desired output voltage values. In some cases, the DC-DC datasheet provides a formula for calculating the output voltage for a given trim resistor.
The first field is the output voltage of the DC-DC converter when the trim pin is open. This usually will be one of the entries in the table, or is calculated using a formula in the datasheet. The two examples columns are also completed using the same table or the formula in the datasheet of the DC-DC converter.

Note: one of the voltage values selected should be the maximum output voltage and the second voltage value should correspond to the minimum voltage. These voltage values need not be the actual output voltage used in the circuit board.

Finally, enter the DC-DC converter model name (for example, Murata_OKYT3_D12) and save the file.

Programmable Voltage with Resistor Connected from Trim Pin to Vout

Figure 8-17 shows the dialog box that appears when the programmable voltage DC-DC converter is selected.

Figure 8-17. Reference Voltage/ Current for the DC-DC Converter

All DC-DC converters use some form of reference voltage or current to set the output voltage. The value of the reference voltage ‘Vref’ is shown either in the specifications section of the datasheet or in its output voltage calculation formula. Sometimes the datasheet shows the architecture of the error amplifier with the value of Vref.

In some cases, the DC-DC converters use current reference instead of voltage reference. The current reference value is accompanied by a parallel resistor. Again, some DC-DC converter datasheets show the equivalent circuit in the error amplifier section. After entering the Vref or Iref & Rref values, click on <Next> to get the dialog box shown in Figure 8-18.

Figure 8-18. Configuring the Programmable Voltage DC-DC Converter Library Entry

The output voltage of these types of DC-DC converters is determined by the resistor connected from their Trim pin to Gnd. To complete this dialog box, refer to the DC-DC converter datasheet for a table that maps the output voltage to the resistor values connected between the trim pin and Vout. In some cases, the DC-DC datasheet provides a formula for calculating the output voltage for a given trim resistor.

The first field is the output voltage of the DC-DC converter when the trim pin is open. This usually will be one of the entries in the table, or is calculated using a formula in the datasheet. The two examples columns are also completed using the same table or the formula in the datasheet of the DC-DC converter.

Note: one of the voltage values selected should be the maximum output voltage and the second voltage value should be minimum voltage. These voltage values need not be the actual output voltage used in the circuit board.

Finally, enter the DC-DC converter model name (for example, POL_XYZ) and save the file.
Creating a Library Entry for a Discrete DC-DC Converter

These types of DC-DC converters are common when they are realized using switcher ICs, switching and filter elements. The output voltage is programmed by connecting two resistors, Rfb and Rin. The output voltage of the DC-DC converter is calculated using the formula:

\[
V_{out} = \frac{R_{fb} \times V_{ref}}{R_{in}}. \quad \text{(Vref is the DC-DC converter reference voltage)}
\]

When the DC-DC converter used is of this type, the dialog box, shown in Figure 8-19, is used to create the library entry.

The dialog box is completed by entering the Rfb and Rin values calculated for a given output voltage, and Vref, which is found in the datasheet.

Note: the number of resistors used for controlling these types of DC-DC converters can be minimized by using the actual voltage that is used on the board.

**Figure 8-19. Creating a Library Entry for a Discrete DC-DC Converter**

4. Once the library entry is created, the next step is to associate the DC-DC converter from the library to the Trim pin. This is done using the following procedure, shown in Figure 8-20.

   a. Start with the ispPAC-POWR1220AT8 schematic

   b. Double Click on the Margin/ Trim block
c Double Click on the TrimCell of interest (for example, TrimCell 1)

d. The dialog box shown in Figure 8-21 is used to design the resistor network

Figure 8-20. Accessing the Margin and Trim Dialog Box

Designing the resistor network for a DC-DC converter connected to a TrimCell.

The following dialog box opens after double clicking a TrimCell in the bottom schematic in Figure 8-21.
**Figure 8-21. Calculating the Resistor Network for a Given DC-DC Converter**

<table>
<thead>
<tr>
<th>Schematic Net Name:</th>
<th>Trim1</th>
<th>OK</th>
<th>Cancel</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC-DC Converter:</td>
<td>Murata_OKY3_D12</td>
<td>Import DC-DC</td>
<td></td>
</tr>
<tr>
<td>Profile 0 Mode:</td>
<td>Closed Loop Trim</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Voltage Profile</th>
<th>Target Voltage</th>
<th>Realized Voltage</th>
<th>DAC Code</th>
<th>DAC Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 (0, 0)</td>
<td>1.2 V</td>
<td>1.138 V</td>
<td>2</td>
<td>-0.03 uA</td>
</tr>
<tr>
<td>1 (0, 1)</td>
<td>1.26 V</td>
<td>1.256 V</td>
<td>-8</td>
<td>-0.03 uA</td>
</tr>
<tr>
<td>2 (1, 0)</td>
<td>1.14 V</td>
<td>1.140 V</td>
<td>10</td>
<td>-0.03 uA</td>
</tr>
<tr>
<td>3 (1, 1)</td>
<td>1.2 V</td>
<td>1.139 V</td>
<td>2</td>
<td>-0.03 uA</td>
</tr>
</tbody>
</table>

**Schematic Net Name** – The actual name of the pin in the schematic

**DC-DC converter** – Select the appropriate DC-DC converter from the library by clicking the import DC-DC menu. In this example, Murata_OKY3_D12 is selected.

**Profile 0 mode** – The pull down menu selects the operating mode of the TrimCell: Closed loop trim, Trim using I^2C interface with an external microcontroller and E^2^CMOS value (open loop trimming), is selected.

**Voltage Profile 0** – The nominal operating voltage of the DC-DC converter.

**Voltage Profile 1** – One of the margining profiles: it can be margin-up or margin-low value.

**Voltage Profile 2** – The other margin profile. Again, this can be margin-down or margin-up voltage value.

**Voltage Profile 3** – An additional profile provided for convenience. In some cases, this can be used for additional margin testing.

After entering the required voltage values, click on `<calculate>`. The software calculates the resistors to be placed between the TrimCell output and the DC-DC converter trim pin. Calculated DAC code values...

along with the DAC currents for each of the profiles are also shown. When the **OK** button is clicked, these values are stored into the source file.

The **<Options>** button opens the following dialog box (Figure 8-22) that can be used to fine tune the calculated resistor values.

*Figure 8-22. Optimizing Resistor Values*

<table>
<thead>
<tr>
<th>Trim Configuration Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>EIA Resistor Standard</td>
</tr>
<tr>
<td>Maximum DAC Code Range</td>
</tr>
<tr>
<td>Max Supply Adjustment Range</td>
</tr>
<tr>
<td>Attenuation Crossover Voltage</td>
</tr>
<tr>
<td>Open External Resistor(s) Threshold</td>
</tr>
<tr>
<td>Vbpz Selection</td>
</tr>
</tbody>
</table>

**EIA resistor standard** – limits the resistor selection to EIA 12, EIA24, EIA48, EIA96, EIA192. It also provides a method to calculate the exact resistor values. The selection of this option depends on design requirements

**Maximum DAC code range** – used to provide additional headroom in the DAC code for maximum voltage variation. This is to account for the errors in resistor values and the DC-DC converter inaccuracies.

**Maximum supply adjustment range** – this is the maximum margin voltage range with respect to the nominal value that is specified on profile 0. If the design requires margining of 10%, this value is set to 10%.

**Attenuation crossover voltage** – the maximum input voltage for the ADC is 2.048V. If this ADC is used for measuring voltage higher than the Attenuation Crossover Voltage, the on-chip 1:3 attenuator should be turned on. This allows the maximum voltage input to the ADC to increase to 6.144V. This entry sets the voltage at which the attenuator should be switched on.

**Open External Resistor(s) Threshold** – the maximum resistor value above which the resistor is treated as an open circuit - The trim and margin routine calculates up to three resistors and the associated topology as shown in Figure 8-7, Figure 8-8, Figure 8-9, Figure 8-10 and Figure 8-11. This field can be used to force the algorithm to minimize the number of resistors to the equivalent circuit shown by Figure 8-11. To do that, first calculate the resistors using the default values. Change the Open External Resistor(s) Threshold field to a value slightly higher than the series resistor value and click on the **<OK>** button. The software automatically calculates the new resistors and the associated DAC values.

**Vbpz Selection** – usually it is best left as auto. In some cases, by forcing the Vbpz values to one of the other voltages (0.6V, 0.8V, 1V or 1.25V), the number of resistors can be reduced.
After calculating the resistor values for all TrimCells, the software automatically saves all the values in to the “XXX.PAC” file.

To generate a report file of all resistors connected to all TrimCells the following procedure is followed.

Click on **Files> Export** and the following dialog box (Figure 8-23) opens.

**Figure 8-23. Generating a Report File for Margin and Trim**

Under “Export What,” select Margin/Trim to a file selected by using the **Browse** button, and click **OK**. The output text file format is as shown as follows:

```
MarginTrimCell
 Idx0
 TrimCellNumber1
 TargetVoutSP11.200
 TargetVoutSP21.260
 TargetVoutSP31.140
 TargetVoutSP41.200
 RealizedVoutSP11.198
 RealizedVoutSP21.256
 RealizedVoutSP31.140
 RealizedVoutSP41.198
 VdacCodeSP12.000
 VdacCodeSP2-6.000
 VdacCodeSP310.000
 VdacCodeSP42.000
 Vref0.752
 Rbuffer2561546.920
 Rfb14467007.127
 Rin1000000000.000
```
Invert1
IsProgrammable1
IsModule1
IsRtGnd1
Rseries24000000.000
Rpdn110000000.000
Rpup210000000.000
Rpdn210000000.000
Rpup110000000.000
BPZVoltage0.600
BrickNameMurata_OKYT3-D12.xml
BrickFilename
TargetVdacCodesMax110
EIAStdIdx1
LooseEIAStdIdx1
AttenuationCrossoverVoltage1.900
MaxDeltaVoutPercent5.000000
Rpdn0
Ropen100000000.000000000000000
BPZSel0.000000000001056
ResistorComputationAlgorithm1
MarginTrimCell_end
9.1 PAC-Designer: Power Management Design Tool

One major reason for the popularity among system engineers of programmable devices like the Power Manager II family is the flexibility of the hardware solution. One silicon device can serve in a variety of applications or integrate multiple board power management functions. While the term “programmable” usually conjures images of a software engineer writing ‘C’ or assembly language for an embedded microcontroller, programmable devices like the Power Manager II are designed using a class of Electronic Design Automation (EDA) software that is easy to learn for a hardware engineer with expertise in the analog, system or digital electronics disciplines. Rather than a software engineer writing firmware, the hardware designer will model the design using a hardware design language (HDL) or graphical tools like a schematic or waveform editor.

To make designing with the Power Manager II device as easy as possible for the engineer with a power circuit design background, Lattice provides a free EDA tool called PAC-Designer*. In the PAC-Designer tool, circuit designs are entered graphically and then verified, all within the software environment. In the example below, the PAC-Designer schematic window provides access to all configurable elements of an ispPAC-POWR1014A device via its graphical user interface. All analog input and output pins are represented. Static or non-configurable pins such as power, ground and the serial digital interface are omitted for clarity. Any element in the schematic window can be accessed via mouse operations as well as menu commands. When completed, configurations can be saved, simulated and downloaded to devices.

Programmable hardware with a software design tool provides a more flexible solution for engineering and a cost-cutting measure for component procurement departments. Programmability is attractive from an economic standpoint to component engineers and procurement personnel who wish to reduce the number of discrete solutions and vendors that they must qualify, inventory, and manage. It’s for these economic benefits that procurement departments will heavily influence the preferred part inventory of electronic components.

This chapter describes how PAC-Designer software and development kits are applied to solve the power management and control scenarios described in earlier chapters of Power 2 You.

* This document refers to PAC-Designer version 5.3 or later.
Benefits of Software-Driven Programmable Hardware Design

Power management and control solutions traditionally have been implemented with discrete analog and mixed-signal ICs. Browse the component catalog of any popular vendor of voltage supervisor or watch-dog timer ICs and you’ll quickly see the hundreds of variations available to satisfy a range of accuracy, operating conditions and capacity. Further, depending on the degree of functional integration required, even more product variations are available. The Power Manager II technology is disruptive due to its versatility, enabled through programmability. In the same way the TTL discrete logic ICs of the 1970s have been almost entirely integrated by modern CPLDs and FPGAs, Power Manager II integrates multiple discrete analog ICs and is flexible enough to be applied across most power management configurations.

Benefits of software-driven programmable hardware design include:

• Reduce cost by reducing the number of Power Manager II components – Multiple power management functions can be integrated into a single power management device. The integrated solution can also be customized to meet board-specific sense and control interface requirements.
• Reduced risk of board re-spins and faster time to market – New designs or changing board requirements can be handled by an updated program for the Power Manager II. HDL-based designs are flexible to meet changing functional requirements.
• Increased likelihood of first-time success and reduced time to market - Functions and performance can be modeled by a software program and the model can be tested fully using simulation methods.

Advantages of Power Manager II over Microcontroller Firmware-Based Solutions

One of the alternative approaches to a flexible power management solution is a microcontroller with firmware. Some of the major drawbacks of this approach are:

• Reduced reliability due to slow response to power faults: Power monitoring is controlled by hardware-generated interrupts, which occur once in 5 to 10ms. This determines the response time of the power management function, which is too slow to prevent faults such as Flash memory corruption.
• Increased time to market due to limited fault coverage of the power management algorithm: A major advantage of HDL-based designs over firmware-based designs is that the HDL-based designs can be simulated fully on a computer rather than a testing circuit board with limited fault coverage. The types of faults that can be created on a circuit board are limited because of secondary fault conditions due to other components on the circuit board that can interfere with the power management algorithm.
• As a result, any changes to software require extensive board-level regression tests that are costly and time consuming. Consequently, changes to firmware are avoided, reducing its flexibility.
9.2 PAC-Designer Overview

Table 9-1 provides an overview of the major features of PAC-Designer software.

<table>
<thead>
<tr>
<th>Design Entry Tools</th>
<th>Purpose</th>
</tr>
</thead>
</table>
| Power Manager II Schematic | Navigate and access the configuration of Power Manager II functional blocks such as:  
  - Digital I/O buffer configuration  
  - Analog input comparators  
  - High-voltage output drivers  
  - Timer/oscillator settings  
  - Margin and trim cell settings  
  - Sequence control and supervisory logic |
| LogiBuilder                 | LogiBuilder is used to design the embedded digital functions of the Power Manager II. Logic can be captured as a sequence of events described in a high-level state machine like language or as traditional Boolean equations.  
  LogiBuilder provides a Sequence Controller window that allows you to create control sequences and define logic functions and a Supervisory Equation window to enter combinatorial or registered logic independent of sequence controller logic. |
| DC-DC Library Builder      | The Library Builder is used to define the voltage adjustment characteristics of DC-DC converters and voltage regulators. A detailed description of trimming and margining software GUI is provided in the ‘Margining and Trimming,’ Chapter 7. |

<table>
<thead>
<tr>
<th>Simulation Tools</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>HDL Export</td>
<td>The HDL writer included with PAC-Designer exports an industry standard Verilog HDL or VHDL model of the digital logic and timer/counter of the Power Manager II design. HDL models can be executed with any popular third party simulator such as Aldec's Active-HDL program.</td>
</tr>
<tr>
<td>Waveform Editor</td>
<td>The Waveform Editor is a graphical application used to create and edit waveforms for logic stimulus. Each waveform is given a user-defined name, and then edited to show transitions. The stimulus is applied to the LogiBuilder - generated model and waveform results are produced much like those of a traditional logic analyzer.</td>
</tr>
<tr>
<td>Lattice Logic Simulator</td>
<td>PAC-Designer includes a logic simulator to verify logic produced by the LogiBuilder tool.</td>
</tr>
</tbody>
</table>

Selecting the Power Manager II Device from a Design Specification

The first step in a power management and control design is to determine how many functions can be integrated into a Power Manager II device. Here are some of the key considerations (Refer to Figure 9-1 “PAC-Designer Software - ispPAC-POWR1014A” on page 9-7 for a brief description of these functions):

- Primary Power Management  
  - Hot-swap, redundant power feed management, external power feed  
  - Input voltage – Positive/ negative, need for isolation  

- Secondary power management functions  
  - Main secondary rail(s)  
  - Number of DC/DC converters that will be sequenced, supervised.  
  - Number of DC/DC converters that will be margined/trimmed
– Number of reset signals that will be distributed on the board for microprocessor, DSP, ASIC, FPGA devices.
– Number of external watchdog timers required for the system

Once the board power management functions are finalized, use Table 9-2 to select potential Power Manager II devices to integrate the power management functions.

Table 9-2. Power Manager II Vs Board Power Management Functions

<table>
<thead>
<tr>
<th>Managing Supply Rails in a Circuit Board</th>
<th>ProcessorPM-POWR605</th>
<th>ispPAC-POWR607</th>
<th>ispPAC-POWR1014</th>
<th>ispPAC-POWR1014A</th>
<th>ispPAC-POWR1220AT8</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Board Input (Primary) Supply Management</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hot-swap</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-48V Hot-swap Controller (Payload - isolated)</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>+12 / 24V Hot-swap Controller</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td><strong>Power Feed To External Systems</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-48V Supply Feed</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>+12/24V Supply Feed</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td><strong>Redundant Supply Selection</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-48V Supply OR'ing using MOSFET (Payload - isolated)</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>+12/24V Supply OR'ing using MOSFET</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td><strong>Payload (Secondary) Power Management</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Sequencing</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Voltage Supervision</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Reset Generation</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Watchdog Timer</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Voltage Measurement Using ADC</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Supply Voltage Trimming</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Supply Margining</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
The next step is to identify the smallest Power Manager II device using the number of secondary power supply rails as well as the functions in Table 9-3.

### Table 9-3. Select the Smallest Power Manager II Device Using the Number of Rails

<table>
<thead>
<tr>
<th>Number of rails</th>
<th>&lt;3</th>
<th>3 to 5</th>
<th>5 to 8</th>
<th>&gt;8</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset Generation</td>
<td>ProcessorPM-POWR605</td>
<td>ispPAC-POWR1014</td>
<td>ispPAC-POWR1220AT8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage Supervision</td>
<td>ProcessorPM-POWR605</td>
<td>ispPAC-POWR1014</td>
<td>ispPAC-POWR1220AT8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Watchdog Timer</td>
<td>ProcessorPM-POWR605</td>
<td>ispPAC-POWR1014</td>
<td>ispPAC-POWR1220AT8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimal sequencing &lt; 3 groups</td>
<td>ProcessorPM-POWR605</td>
<td>ispPAC-POWR1014</td>
<td>ispPAC-POWR1220AT8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Individual Supply Sequencing Control</td>
<td>ProcessorPM-POWR605</td>
<td>ispPAC-POWR607</td>
<td>ispPAC-POWR1220AT8</td>
<td>ispPAC-POWR1220AT8</td>
<td></td>
</tr>
<tr>
<td>Hot-swap controller - 48V</td>
<td>ispPAC-POWR607</td>
<td>ispPAC-POWR607</td>
<td>ispPAC-POWR1220AT8</td>
<td>ispPAC-POWR1220AT8</td>
<td>Used on -48V Rail</td>
</tr>
<tr>
<td>Hot-swap controller +5 or 12 or 24V</td>
<td>ispPAC-POWR607</td>
<td>ispPAC-POWR1014</td>
<td>ispPAC-POWR1220AT8</td>
<td>ispPAC-POWR1220AT8</td>
<td></td>
</tr>
<tr>
<td>I²C, ADC Measurement</td>
<td>ispPAC-POWR1014A</td>
<td>ispPAC-POWR1014A</td>
<td>ispPAC-POWR1220AT8</td>
<td>ispPAC-POWR1220AT8</td>
<td></td>
</tr>
<tr>
<td>Supply Margining/Trimming</td>
<td>ispPAC-POWR6AT6</td>
<td>ispPAC-POWR6AT6</td>
<td>ispPAC-POWR1220AT8</td>
<td>ispPAC-POWR1220AT8</td>
<td></td>
</tr>
</tbody>
</table>

### Power Manager II Design Example

The example considered in this section is a PCI-Express add-on card application. This example is used to describe the procedure for integrating the power management design into a Power Manager II device. The first step is to collect the power management design specifications for the PCI Express add-on card. Table 9-4 summarizes the power management functions implemented in a PCI-Express add-on card:

### Table 9-4. PCIe Board Power Management Specifications

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Backplane voltage</td>
<td>12V</td>
</tr>
<tr>
<td>Hot-swap function required?</td>
<td>Yes</td>
</tr>
<tr>
<td>Redundant supplies used?</td>
<td>No</td>
</tr>
<tr>
<td>External power feed function required?</td>
<td>No</td>
</tr>
<tr>
<td>Number of secondary rails</td>
<td>5</td>
</tr>
<tr>
<td>Secondary supply sequencing needed?</td>
<td>Yes</td>
</tr>
<tr>
<td>Reset generation needed?</td>
<td>Yes</td>
</tr>
<tr>
<td>Number of reset signals</td>
<td>2</td>
</tr>
<tr>
<td>Watchdog Timer required?</td>
<td>Yes</td>
</tr>
<tr>
<td>Voltage and current measurement needed?</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Table 9-2 shows that these functions can be integrated into an ispPAC-POWR1014A or an ispPAC-POWR1220AT8 device. However, using Table 9-3, the smallest Power Manager II device that can integrate all these functions is an ispPAC-POWR1014A. The next step is to start designing the Power Management algorithm using the information given in earlier chapters.
Design Flow

This section describes a typical user scenario using PAC-Designer software to design a power management algorithm.

The typical design flow to design with PAC-Designer software:

1. Create/Open a project.
2. Configure analog input signals.
3. Configure digital inputs.
5. Configure high-voltage output (HVOUT) pins (MOSFET driver outputs).
6. Configure timer values.
7. Configure an I2C address.
8. Implement the power management algorithm using the LogiBuilder tool.
9. Simulate the design and iterate steps 2 through 6.
10. Download the design into a Power Manager II device and verify design.

9.3 Example Design Resources

The fastest way to a solution for your particular application often is to modify an existing example. Lattice provides three types of example designs:

- Project examples installed with PAC-Designer software -
  To open a project example from PAC-Designer, choose File > Design Example. A dialog listing of each example with a brief description is provided. Details of each example can be found in <PAC Designer root>\Examples\Design Examples.ppt.

- Power Manager II Reference Designs at the Lattice website -
  Each Lattice Reference Design has a web page that provides a brief overview of that function and available options. Complete details can be found in the documentation for that particular design. The documentation, along with the actual source code, can be downloaded from the web pages. Link to Lattice Reference Designs: http://www.latticesemi.com/products/intellectualproperty/aboutreferencedesigns.cfm

- Demonstration designs included with Power Manager II Development Kits -
  Demo designs are typically preprogrammed into Power Manager II evaluation boards and are designed to showcase key features and benefits of the hardware. Other demonstrations and interface utilities are available at the respective Development Kit web page. Link to Lattice Development Kits: http://www.latticesemi.com/products/developmenthardware/developmentkits/index.cfm
9.4 Designing PCI-Express Add-on Card Power Management Using an ispPAC-POWR1014A Device

1. Open/Create a New Design
This section uses the design example ispPAC-POWR1014A-3_PCIE_HS_Seq_Rd_Sup.PAC. The feature list of this design is found on page 40 of the ‘Design Examples.PPT’ file found in the <PAC-Designer root>/ Examples directory.

The circuit diagram of the implementation is shown on page 41 of the Design Examples.PPT file. Page 42 provides the algorithm for implementing 12V hot-swap, sequencing, supervision and reset generation for this design. The next step is to implement the design in PAC-Designer software.

The PAC-Designer software provides the complete design source code. Start the PAC-Designer software. Click on File > Design Examples and select the above mentioned design example file and click on <Open File> button.

The software opens the screen shown in Figure 9-1.

Figure 9-1. PAC-Designer Software - ispPAC-POWR1014A

2. Configuring Analog Input Signals
The next step is to configure the monitoring voltage thresholds. To do that, click on the Analog Inputs block on the top right of the schematic. The software shows two programmable threshold comparators with the associated window logic for each of the VMON inputs. In the ispPAC-POWR1014A device there are 20 programmable threshold comparators.
Double click on any of the programmable threshold comparators to open the dialog box. This dialog box shows the names of the voltage monitoring comparator outputs as well as the thresholds for each of the comparators.

*Figure 9-2. Configuring Voltage Monitoring Inputs of the ispPAC-POWR1014A Device*

![Analog Input Settings](image)

This dialog box is used to specify the current and voltage monitoring thresholds of both the hot-swap section and the secondary power management sections. This enables fault detection anywhere on the circuit board. The fault threshold level can be changed by using the Trip point selection pull-down menu. For each VMON input, its window monitoring mode and/or the associated glitch filter can also be enabled.

This dialog box can also be used to change the pin allocation of any of the VMON pins by using the ‘Pin Name’ pull down menu.

Then, click on <OK> button, navigate back to the main screen and double click on any portion outside the schematic.
3. Configure Digital Inputs
To configure the digital inputs, click on the digital inputs in the schematic shown in Figure 9-1. The software opens a screen with input signals with input buffers.

Click on any of the input buffers to open the dialog box shown in Figure 9-3.

*Figure 9-3. Configure Digital Inputs*

Enter the names of the digital input pins and also identify the source of the signal (I²C/JTAG/ device pin) and click OK.

This section specifies the interfacing of the Power Manager II with the active low signals on the backplane, such as PRST_N or PERST_N, as well as to the onboard active low signal using the FPGA_Done_N.

This dialog box can also be used to change the pin allocation of any of the IN pins by using the **Pin Name** pull down menu.

Navigate back to the main schematic by double clicking anywhere on the blank screen around the input pin connection schematic.

4. Configure Digital Output Pins
From the main schematic in Figure 9-1, double click on the digital output to navigate to the next screen with multiple output buffers. Double click on any of the output buffers to open the dialog box shown in Figure 9-4.
This dialog box is used to configure the output pin name that is used in the algorithm. If a pin is used as an I²C output port expander, click on the appropriate radio button for that output.

This section identifies the signals that drive the DC-DC converter signals for sequencing on-board control signals such as PERST local, brown_out_N, etc.

This dialog box can also be used to change the pin allocation of any of the OUT pins by using the ‘Pin Name’ pull down menu.

Click on the OK button to navigate back to the screen with output buffers. Click anywhere on that screen.

5. Configure HVOUT Pins
These pins are used to drive the 12V hot-swap control MOSFET as well as the 3.3V soft start MOSFET.

To configure these signals, first click on the HVOUT outputs block on the screen. This opens an intermediate dialog box. Click on any of the boxes to open the dialog box shown in Figure 9-5.
This dialog box enables setting the MOSFET drive voltage as well as MOSFET turn-on/turn-off ramp rates.

Enter the names of the output signals used in the design to control the external charge pump for the 12V MOSFET, as well as the MOSFET turn on for 3.3V.

Click OK and navigate back to the main screen using the same methods described previously.

6. Configure Timer Values
This design uses multiple hardware design timers for the external charge pump, for pulse stretching the reset output, etc.

To configure the timer, double-click on the timer control box between the input and output control signals to open an intermediate schematic. Click on the timer blocks to open the timer configuration dialog box as shown in Figure 9-6.
This dialog box enables changing the Master/Slave mode of operation when more than one Power Manager II device is used on the board. The time delay for each of the timers can also be set from this menu. For example, the Timer 4 is used for external charge pump implementation that requires the HVOUT2 pin toggle with a cadence of 32μs on and 8μs off.

Once the timers are configured, click on the <OK> button to return to the main schematic.

7. Configure I²C Addresses
The ispPAC-POWR1014A device can be used to measure the voltages and currents through the I²C interface. For this, the ispPAC-POWR1014A should be assigned a unique address by clicking on the I²C box in the main schematic in Figure 9-1 to open the dialog box shown in Figure 9-7.
Figure 9-7. Setting the I2C Address for the ispPAC-POWR1014A Device

The address is set by using the pull down menu on top of the dialog box shown in Figure 9-7. The output control for each of the output pins as well as for the input pins can be set through this dialog box as well.

Click **OK** to navigate back to the main schematic.

**8. Implementing the Power Management Algorithm Using the LogiBuilder Tool**

The power management algorithm as described in the ‘Design Examples.PPT’ file is entered into the ispPAC-POWR1014A device in this section using the LogiBuilder utility.

Double click on the sequence control block of the main schematic to open the LogiBuilder screen, as shown in Figure 9-8.

To facilitate understanding of the PCI-Express add-on card algorithm, the next section explains the LogiBuilder screen sections.

The LogiBuilder screen is divided into three sections:

**The sequential execution sections** – Enter a list of instructions listed in Table 9-5 to implement the sequential execution part of the algorithm.

**The exception conditions section** – Enables a set of Boolean expressions which, when they become true, interrupt the sequential execution flow. These exception conditions can only interrupt the steps which are marked as interruptible. All other steps are not affected by the exception conditions.

**The supervisory logic section** – Enables the Boolean expressions direct control of some of the outputs that are not controlled by the sequential execution portion of the algorithm.

The Boolean expressions in the exception condition as well as supervisory logic section operate in parallel to the instructions executed in the sequential execution section.
In the sequential execution section each step is divided into five columns:

- **Step** – This indicates the step number of a given instruction. This step number is used to branch to a given step from a different location.

- **Sequencer instruction** – This is the instruction that is being executed by that step. Each step can take one to several clock cycles. For example, a start timer instruction takes one clock cycle. A wait for timer instruction stays in that step until the timer expires.

- **Outputs** – This lists all the outputs whose output values are changed at that step. The output state changes after the first clock pulse while in that step.

- **Interruptible** – This flag enables the exception condition to interrupt the flow of execution. If the interruptible flag is set to ‘no,’ the exception condition cannot alter the flow at that step.

- **Comment** – This column is used to enter the comment for that instruction.

**Sequencer Instructions**

There are six types of instructions used to implement the sequential execution portion of the power management algorithm. These instructions are listed in Table 9-5.

Table 9-5. Sequencer Instructions and Description

<table>
<thead>
<tr>
<th>Instruction Type</th>
<th>Instruction Sub Type</th>
<th>Operands</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wait for timer</td>
<td></td>
<td>Selected Timer</td>
<td>Starts a given timer, waits for it to expire and jumps to the next sequential step. The timer is reset in the prior step.</td>
</tr>
<tr>
<td>Wait for &lt;Boolean&gt;</td>
<td></td>
<td>Boolean Expression</td>
<td>Waits for the Boolean expression to become true at that step. When Boolean is true, it jumps to next sequential step.</td>
</tr>
<tr>
<td>Wait for &lt;Boolean&gt; with Timer</td>
<td></td>
<td>Boolean Expression &amp; Selected Timer</td>
<td>Waits for the Boolean expression to become true until the timer expires at that step. When Boolean is true, it jumps to next sequential step. If the timer expired, it branches to a step indicated by the instruction. The timer is reset in the prior step.</td>
</tr>
<tr>
<td>IF-Then-Else</td>
<td></td>
<td>Boolean Expression</td>
<td>Tests the Boolean expression: If true the control branches to the location specified by the 'Then' Branch. It is possible to alter selected outputs only during this branch. If false the control branches to the location specified by the 'Else' Branch. It is possible to alter selected outputs only during this branch.</td>
</tr>
<tr>
<td>IF-Then-Else with Timer</td>
<td></td>
<td>Boolean Expression &amp; Selected Timer</td>
<td>Tests the Boolean expression: If true the control branches to the location specified by the 'Then' Branch. It is possible to alter selected outputs only during this branch. If the condition is not true, if the timer is expired, control branches to the location specified by the 'On Timeout Go to Sequencer Step' Branch. If the condition is not true and the timer has not expired, the control branches to a location specified by the 'Else' branch.</td>
</tr>
<tr>
<td>Output</td>
<td>None</td>
<td>Specified outputs</td>
<td>Only the selected output condition is set to the state specified by this instruction. Writing the same value to the output pin does not result in glitches.</td>
</tr>
<tr>
<td>Go To</td>
<td>Go to</td>
<td>Step Number</td>
<td>Control Branches to the step indicated</td>
</tr>
<tr>
<td></td>
<td>Halt</td>
<td>None</td>
<td>Jumps to the same step and waits forever.</td>
</tr>
</tbody>
</table>
Exception conditions section

Each of the exception condition is divided into five columns:

Exception ID – The number of the exception condition: used by the compiler to point errors in that line

Boolean expression – this is the Boolean expression which, when it becomes true, will force the sequence execution to jump to the step indicated by the exception handler step.

Outputs – Forces the outputs to the value set by the exception condition. Setting or resetting an output results in the Boolean expression always controlling that output, and is independent of the sequence instruction execution.

Exception handler – This is the step number in the sequential execution section to which the control jumps when the exception condition becomes true and the sequential execution section is executing a step that has been flagged as an interruptible step.

Comments – This section is used for providing useful comments about that exception condition.

Supervisory equation section

The supervisory equation window is used to control outputs that are not controlled by the sequential execution section. The supervisory equation is divided into four columns.

Equation – This field indicates the supervisory equation number and is used by the compiler to flag errors.

Supervisory Logic Equation – this column is where the Boolean logic condition and the associated output that is controlled by the equation is specified.

Macrocell Configuration – This column indicates the type of assignment in the supervisory logic equation for that output. It can be combinational, D-type, T-type, Asynchronous Reset or Asynchronous Preset.

Comment – provides additional information about the step for better understanding of that equation.

9. PCI-Express Example LogiBuilder Code

Figure 9-8 shows the implementation of the PCI-Express add-on card algorithm implemented using the instructions shown above.
The algorithm implemented in this LogiBuilder screen is shown below:

**Sequential Execution Section**

1. Disable hot-swap operation.
2. Wait for 12V and 3.3V rails to stabilize.
3. Enable hot-swap operation on 12V, operate MOSFET in SOA
   <Actual MOSFET hot-swap operation control is performed by the supervisory logic section>
4. Wait for 12V output from the MOSFET to reach acceptable thresholds.
5. Start sequencing by enabling 3.3V and 1V supplies.
6. Wait for 3.3V and 1V supplies to reach acceptable voltage levels.
7. Enable 1.8V and soft start 3.3V from the connector.
8. Wait for all board supplies to reach acceptable voltage levels & FPGA to configure.
9. Activate early configuration start signal.
10. Release CPU_Reset signal after the stretch period.
11. Wait for voltage or current faults.

13. Activate CPU_Reset signal and disable 1.8V supply & turn off the 3.3V MOSFET.

14. Wait for 2ms and disable 3.3V and 1V supplies.

15. Wait for 2ms and turn off 12V MOSFET.

**Exception conditions section**

1. If over current condition is detected jump to step 12.

2. Transfer input PERST state to PERST_Local signal.

**Supervisory Equations section**

1. Operate charge pump to drive the 12V control N-channel MOSFET by toggling the HS-12V_MOSFET drive pin (8μs Off, 32μs On).

2. Limit 12V MOSFET operation in SOA until 12V rail reaches acceptable level, after that turn the MOSFET on fully.

3. Turn-off 12V MOSFET when over current condition is detected.

The programmable features, shown below, of this design can be used to adapt the design across different PCI-express add-on card configurations.

- SOA and over current levels.
- Customize the design to suit most MOSFETs.
- Initial contact de-bounce period programmable from 32μs to 2 seconds.
- Short circuit timeout during start up programmable from 32μs to 2 seconds.
- Reset pulse can be stretch duration programmable from 32μs to 2 seconds.
- Each of the voltage monitoring thresholds are programmable from 0.67V to 5.8V.

This algorithm can be imported easily into an ispPAC-POWR1220AT8 device if the number of supplies in the PCI-Express add-on card increases beyond five or other control functions need to be added.

**10. Compiling the Design**

After the design is entered, the next step is to compile the program. To compile the program click on **Tools> Compile the LogiBuilder Design**

The program converts the code into ABEL (Advanced Boolean Expression Language) language and compiles the ABEL language into a highly optimized equations netlist. These equations are then sent to the Fitter program that fits the design into the CPLD of the Power Manager II.

**11. Simulating Control and Supervisory Logic**

When the primary supply rails for a circuit board are energized how will the Power Manager II respond and sequence the various DC-DC converters and distribute the reset signals? If the firmware of a microcontroller hangs and fails to reset the watchdog timers you have defined, will the WDT assert an interrupt the way you expect? These are the types of scenarios you’d like to model before you commit your design.
to hardware. To help, PAC-Designer software can extract a model of your digital and timer logic to any popular HDL simulator.

From PAC-Designer, the optimized equations produced by LogiBuilder can also be exported into VHDL or VerilogHDL languages. These files can then be used for simulation. To export an HDL file, choose File > Export. The Export dialog, shown in Figure 9-9, appears. From the Export What list, choose VHDL File or Verilog File.

*Figure 9-9. Dialog Box to Export the Design in Verilog for Simulation*

![Export dialog](image)

The exported Verilog source file shown in Figure 9-10 can be tested fully using any of the popular HDL simulators such as Aldec’s Active-HDL.
Figure 9-10. Exported Verilog Source File

```verilog
module POWER104A_9_PCIE_NS_Seq_NS_Sup
  (IN 12V_OK, IN 3V3_OK, IN 12V Over SDA Limit,
   BUS 3V3_OK, BUS 3V3 Over LIT, RSD 3V3 OK,
   BUS 3V3 Over LIT, Core 1V0 OK, Core 1V0 Over LIT,
   IO 1V8 OK, IO 1V8 Over LIT, Seq 3V3 OK,
   NS 12V_OK, NS 12V Over LIT, AGOOD, PERST_N,
   FPGA Done, THERM1_T, THERM2_T, THERM3_T,
   THERM4_T, SoftStart 3V3, NS 12V Mopwr On,
   Shcut 12V Down, En 3V3, En 1V0, En 1V0,
   PERST Local N, Early Config Start,
   Brown Out N, CPU Reset N, CLK_IN, RESET);

input IN 12V_OK /*synthesis loc="001"*/; //exemplar attribute IN 12V_OK loc 001
input IN 3V3_OK /*synthesis loc="903"*/; //exemplar attribute IN 3V3_OK loc 903
input IN 12V OK /*synthesis loc="905"*/; //exemplar attribute IN 12V OK loc 905
input IN 12V Over SDA Limit /*synthesis loc="906"*/; //exemplar attribute IN 12V Over SDA Limit loc 906
input BUS 3V3_OK /*synthesis loc="907"*/; //exemplar attribute BUS 3V3_OK loc 907
input BUS 3V3 Over LIT /*synthesis loc="908"*/; //exemplar attribute BUS 3V3 Over LIT loc 908
input RSD 3V3_OK /*synthesis loc="909"*/; //exemplar attribute RSD 3V3_OK loc 909
input RSD 3V3 Over LIT /*synthesis loc="910"*/; //exemplar attribute RSD 3V3 Over LIT loc 910
input Core 1V0_OK /*synthesis loc="911"*/; //exemplar attribute Core 1V0_OK loc 911
input Core 1V0 Over LIT /*synthesis loc="912"*/; //exemplar attribute Core 1V0 Over LIT
input IO 1V8_OK /*synthesis loc="913"*/; //exemplar attribute IO 1V8_OK loc 913
```

For Help press F1

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About the Author

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