Sil8784 Multi-format Analog Video Front-end with HDMI/MHL Transmitter

Data Sheet

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1. General Description
The Lattice Semiconductor SiI8784 device is a high quality, multi-format analog video decoder and processor with an integrated dual-mode High Definition Multimedia Interface (HDMI®)/Mobil High-definition Link (MHL®) transmitter. A microcontroller is integrated to reduce the system Bill Of Materials (BOM) cost.

The SiI8784 device supports worldwide PAL, NTSC and SECAM standards, YPbPr video signals up to 1080p @ 60 Hz resolution, and RGB graphics signals from VGA to UXGA resolutions. It also supports the SCART interface with Fast Blanking and the D-Terminal.

This device contains a Time Base Correction (TBC) module, a de-interlacer with a post-processor engine, and a VBI decoder. For content protected analog videos, HDCP will automatically be enabled on the HDMI or MHL output.

1.1. Features

1.1.1. Analog Video Front-end
- Four 10-bit Analog to Digital Convertors (ADC) sampling up to 170 MHz
- Flexible input multiplexers to support composite, component, VGA, SCART with Fast Blanking and D-Terminal interfaces
- Supports cable plug-in detection and active video signal detection

1.1.2. Multi-format Video Decoder
- Automatic format detection
- Supports NTSC, PAL, and SECAM standards of composite input with adaptive comb filter
- Supports 240p, 480i/p, 576i/p, 720p, 1080i/p component video
- Supports RGB graphics from VGA to UXGA
- Supports Macrovision Type I, II, III copy protection detection
- Supports multi-standard VBI decoding: Teletext, WSS, VPS, CC, CGMS, and V-CHIP

1.1.3. Video Processing
- Time Base Correction
- De-interlacer with Edge Smoothing
- Automatic Phase/Position Detection

1.1.4. HDMI/MHL Transmitter
- Selectable HDMI/MHL Dual-mode
- Compliant with HDMI 1.4b and MHL 2.1 specifications
- HDMI output up to 1080p @ 60 Hz or UXGA @ 60 Hz resolution
- MHL output up to 1080p @ 60 Hz resolution
- HDCP 1.4
- Audio insertion with I2S/ SPDIF input
- VBI data forwarding over HDMI/MHL

1.2. Applications
The SiI8784 device is targeted for the Digital TV (DTV) market.

1.3. Packaging
- 88-pin QFN with exposed pad (ePad)
- 10 mm × 10 mm × 0.9 mm

1.4. Temperature Range
- 0 °C to +70 °C
2. **Product Family**

A comparison of the features between the SiI8784 device and the SiI8788 device is shown in Table 2.1.

<table>
<thead>
<tr>
<th>Feature</th>
<th>SiI8784</th>
<th>SiI8788</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Analog Video Input</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Component (YPbPr)</td>
<td>YES</td>
<td>YES</td>
</tr>
<tr>
<td>Composite (CVBS)</td>
<td>YES</td>
<td>YES</td>
</tr>
<tr>
<td>D-Terminal</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td>RGB graphics (VGA)</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td>SCART with Fast Blanking</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td><strong>Digital Video Output</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Parallel</td>
<td>NO</td>
<td>YES</td>
</tr>
<tr>
<td>HDMI</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td>MHL</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td><strong>Audio Input</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SPDIF Input</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td>I²S Input</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td><strong>Package</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package Type</td>
<td>QFN</td>
<td>QFN</td>
</tr>
<tr>
<td>Pin Count</td>
<td>88</td>
<td>88</td>
</tr>
</tbody>
</table>
3. Functional Description

The SiI8784 device has four subblocks in its signal path and one control block: Analog Front-end (AFE), Video Decoder (VDC), Video Processing, HDMI/MHL transmitter and Control Logic. Figure 3.1 shows the block diagram.

Each subblock is described in the following sections.
3.1. Analog Front-end

The Analog Front-end (AFE) provides four input channels for CVBS, R, G, and B. Each channel includes an Input Multiplexer, a Clamp and Offset DAC, a Programmable Low-pass Filter, and a high quality 10-bit ADC with Programmable Gain Amplifier. In addition, there is a Line Locked PLL to generate sampling clocks for ADCs, Sync Slicers to handle SOG signals, a set of input comparators to support SCART and D-terminal interfaces, and a CVBS output buffer to support SCART.

3.1.1. Input Multiplexer

The SiI8784 device provides two CVBS inputs, and three R/G/B inputs for flexible configurations. Table 3.1 and Table 3.2 show some examples.

Table 3.1. Inputs Configuration with SCART Interface

<table>
<thead>
<tr>
<th>Component</th>
<th>CVBS0</th>
<th>CVBS1</th>
<th>RED0</th>
<th>RED1</th>
<th>RED2</th>
<th>GRN0</th>
<th>GRN1</th>
<th>GRN2</th>
<th>BLU0</th>
<th>BLU1</th>
<th>BLU2</th>
</tr>
</thead>
<tbody>
<tr>
<td>VGA</td>
<td>CVBS</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>SCART</td>
<td>—</td>
<td>CVBS</td>
<td>R</td>
<td>—</td>
<td>—</td>
<td>G</td>
<td>—</td>
<td>—</td>
<td>B</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Table 3.2. Inputs Configuration with D-Terminal Interface

<table>
<thead>
<tr>
<th>Component</th>
<th>CVBS0</th>
<th>CVBS1</th>
<th>RED0</th>
<th>RED1</th>
<th>RED2</th>
<th>GRN0</th>
<th>GRN1</th>
<th>GRN2</th>
<th>BLU0</th>
<th>BLU1</th>
<th>BLU2</th>
</tr>
</thead>
<tbody>
<tr>
<td>VGA</td>
<td>CVBS</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>D-Terminal</td>
<td>—</td>
<td>—</td>
<td>Pr</td>
<td>—</td>
<td>—</td>
<td>Y</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>
3.1.2. Clamp and Offset

As most of the video signals, such as CVBS, are AC coupled, their DC component is lost during the transmission. A voltage type clamp circuit is positioned in front of each channel to restore the DC component.

![Clamp and Offset Diagram](image)

Figure 3.2. Clamp and Offset

The clamp DAC output voltage is 3-bit programmable and AFE provides more accurate 10-bit ±0.5 V output offset DAC to keep the input signal within the ADC input range. The offset level can be controlled automatically by ADCIF block of VDC or manually by software.

3.1.3. Low-pass Filter

The Low-pass Filter (LPF) is a first order analog filter to remove the out-of-band noise from video signal. Its –3 dB bandwidth can be set to 600 MHz (Bypass), 400 MHz, 200 MHz, 100 MHz, or 50 MHz by software. Combined together with ADC over-sampling technology and the high order digital AA (Anti-alias) filter inside VDC, the SiI8784 device can meet the demand of overall AA performance.

3.1.4. ADC with Programmable Gain Amplifier

The ADC samples the input video signal and converts each sample into 10 bits digital data. It supports the sampling rates from 25 MSPS to 170 MSPS, and the sampling clock of CVBS channel can be independent with R, G, and B channels.

For the formats with lower pixel rate, oversampling is recommended. The SiI8784 device supports 2X, 4X and 8X oversampling.

The Programmable Gain Amplifier (PGA) in the front stage of ADC has a nominal gain range from –6 dB to +6 dB, so the SiI8784 device can adapt to a wide range of input video signal levels, especially the CVBS signal from an RF tuner. The PGA can be controlled either automatically by the gain control function of VDC or manually by software.
3.1.5. Line Locked PLL (LLPLL)

The Line Locked PLL (LLPLL) is designed to generate the ADC sampling clock, i.e. pixel clock or oversampled pixel clock. It can be synchronized with a slower reference HSync pulses or run at a fixed frequency. The allowable input HSync range is from 15 kHz to 150 kHz, and the output pixel clock range is from 25 MHz to 170 MHz.

The LLPLL contains a high performance programmable digital PLL (DPLL) and an analog PLL (APLL) which generates the high frequency reference clock needed by the DPLL from the 24 MHz crystal frequency.

The relative phase between the input sync pulse and the output clock of LLPLL can be adjusted in 32 steps by setting registers or automatically by the Auto Phase Detection (APD) block of the video processing module.

3.1.6. Sync Slicer

The Sync Slicer converts SOG and HSYNC signals into core domain digital signals. As shown in Figure 3.3, there are two sets of SOG slicers, each of contains an input multiplexer, a bottom level (0.5 V) clamp, a low pass filter, and a comparator. The comparator threshold is programmable. Also, there are two sets of HS slicers for TTL level syncs. When one of the slicers is configured as an active input, the other can be used to detect the activity of other inputs. This feature is helpful to implement the active channel detection and auto-switch functions.

![Figure 3.3. Sync Slicers](image)

3.1.7. Video Buffer (VBUF)

The Video Buffer (VBUF) buffers and outputs the selected CVBS input signal. This feature is useful to implement the CVBS return channel of the SCART interface. VBUF includes two major subblocks: clamp and voltage-to-current conversion. The Voltage-to-current conversion subblock converts the input signal to the output current which is proportional to the signal voltage level. A 75 Ω source termination resistor should be connected to the CVBS_OUT output pin and signal ground.
3.2. Video Decoder (VDC)

The SiI8784 device provides a multi-format video decoder. VDC includes ADCIF, Sync Processor, adaptive 2D Comb decoder, and VBI Decoder blocks as shown in Figure 3.1 on page 7.

3.2.1. ADCIF

The ADCIF logic block contains Automatic Gain Control and Offset Calibration, and Anti-alias filtering and decimation subblocks. It also generates clamp pulses for clamp circuits at the proper time so that ADC is able to digitize the input analog within the proper range. The main indicator used to determine where the clamping position should be is the horizontal synchronization pulse coming from the Sync Processor block. Since this filtered HSync pulse may not always be correct, several layers of logic have been developed to ensure the clamping is not done at an incorrect position.

3.2.1.1. Automatic Gain Control and Offset Calibration

Parameters such as Sync Amplitude, Back Porch Levels are measured based on the HSync position, register controls, and logic executed in the Offset Gain Calculations sub block. These measured values are then used in determining the offset and gain adjustments. To ensure the stability and accuracy of digitized video signal, several control loops are built in the ADCIF block. These loops include Clamp, Coast, Gain, and Offset. The Clamp and Coast pulses, Gain and Offset parameters are generated by the ADCIF logic and directly connected to the AFE.

3.2.1.2. Anti-alias Filtering and Decimation

The Anti-aliasing (AA) filters remove high frequency noise from the raw digitized signals produced by the front-end video ADCs, and decimate the over-sampled video signal.

The AA filter has flexibility in the frequency response, sharp transition bandwidth, and good stop band attenuation. The AA filter allows the software to change the bandwidth of the filters as the signal conditions changes.

3.2.1.3. Video Decoder

Video Decoder block processes both CVBS data stream and component/RGB data stream. It also supports the SCART Fast Blanking functions.

3.2.1.4. CVBS Processing

CVBS Processing involves the Standard Detection, 2D Video Decoder, and Sync Processor subblocks, as shown in Figure 3.4 below.

![Figure 3.4. CVBS Processing Diagram](image-url)
The SiI8784 device can automatically detect NTSC (M/J/4.43), PAL (B/D/I/G/H/60/70/N/Nc), and SECAM (B/D/G/L/K) standards, and decode them properly.

An adaptive 2D comb filter is used in video decoder. The 2D comb filter has three output options, only horizontal filter, only vertical filter and blending of horizontal and vertical filter. When the current sample is on a horizontal transition edge, the vertical filter is selected. When the current sample is on a vertical transition edge, the horizontal filter is selected. When it is not one of the above two phenomenon, the blending output is selected.

When the input signal is lost, the SiI8784 device can operate in a free-running mode to ensure a stable output.

3.2.1.5. Component/RGB Processing

Component/RGB Processing processes Component Video and RGB Graphics. Component Video Processing includes Sync Processor. Figure 3.5 shows the block diagram of the component video and RGB Graphics processing. The following sections explain each of the blocks in detail.

The SiI8784 device supports 480i/576i, 480p/576p, 720p, 1080i, and 1080p for standard and high definition resolutions. The SiI8784 device supports PC resolutions up to 1600 x 1200 @ 60 Hz (UXGA).

3.2.1.6. SCART Fast Blanking

VDC is designed to support SCART interface: Composite, RGB, and Fast Blanking.

The 4 channel 10-bit ADCs in AFE are mapped to CVBS, RED, GRN, and BLU inputs of SCART interface. A color space converter converts the digitized RGB data from RGB to YUV (BT601). Then the YUV data are resampled from 108 MHz to the 8Fsc frequency used in the 2D comb filter, and meanwhile the YUV444 data are converted to YUV422. These YUV422 data matched the timing of the 2D comb filter output 8Fsc Y/C data, and the two data streams are blended together according to the FB signal information, which indicates the current display source is from original RGB or Composite inputs.

The SCART_ASPECT information is from ASPECT0/1 comparator outputs of AFE, and their results are read-only status registers which can be handled by software.
3.2.2. Sync Processor

The Sync Processor block contains sophisticated digital circuitry that analyzes and extracts synchronization pulses from the incoming video stream. It generates filtered vertical and horizontal sync pulses. The Sync Processor includes Sync separation, format detection, and Sync stabilization.

- **Sync Separation**
The Sync Separation separates the HSync and VSync from the composite sync sliced from video decoder or SOG slicer.

- **Sync Stabilization**
Sync Stabilization does de-glitch, removes serration, and equalizes pulses from the sync signal. It also detects Macrovision protection status.

- **Format Detection**
The format detection detects vertical period and horizontal period and total line number per field.

3.2.3. VBI Decoder

The VBI Processing block slices and processes digitized VBI data from the video. Following are some of the features of the VBI block:

- 108 MHz operating with programmable down sampling
- Supports PAL standards
- Supports NTSC standards
- Enhanced Teletext parity and hamming 8/4 correction

Table 3.3 shows the supported VBI standards.

<table>
<thead>
<tr>
<th>VBI Standard</th>
<th>Video Standard</th>
<th>Data Rate</th>
<th>Scan Lines</th>
<th>Data per Line</th>
<th>Encoding</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>WSS 625</td>
<td>PAL SECAM</td>
<td>5 MHz</td>
<td>23/336</td>
<td>14 Bits</td>
<td>Phase Encoding. Each bit is transmitted using 6 bits of encoded data.</td>
<td>Wide Screen Signaling. Used for aspect ratio settings.</td>
</tr>
<tr>
<td>VPS</td>
<td>PAL SECAM</td>
<td>5 MHz</td>
<td>16/336</td>
<td>13 Bytes</td>
<td>Biphase Encoding. Each bit is effectively represented by 2 bits.</td>
<td>Video Programming System. Used in Germany for program/broadcast info.</td>
</tr>
<tr>
<td>CC</td>
<td>NTSC</td>
<td>0.5030 MHz</td>
<td>21/336</td>
<td>2 bytes</td>
<td>Parity.</td>
<td>Closed Captioning for the hearing impaired.</td>
</tr>
<tr>
<td>XDS VChip</td>
<td>NTSC</td>
<td>0.5035 MHz</td>
<td>284/336</td>
<td>2 bytes</td>
<td>Parity.</td>
<td>Extended Data Service. Used for MISC. NTSC services.</td>
</tr>
<tr>
<td>WSS 525</td>
<td>NTSC</td>
<td>0.4474 MHz</td>
<td>20/336</td>
<td>14 Bits</td>
<td>CRC.</td>
<td>Copy Guard Management System. Used for copy protection and aspect ratio.</td>
</tr>
</tbody>
</table>
3.3. Video Processing
The video processing block performs some necessary processing functions to the decoded video streams before they are outputted. There are also some measurement blocks inside to implement automatic Phase/Position/Gain adjustment functions.

3.3.1. Time Base Corrector
The Time Base Corrector (TBC) is designed to provide stable clock and video data for HDMI/MHL output. It uses a line buffer based architecture in lieu of a frame buffer to save cost and power. To keep HDMI/MHL output TMDS clock jitter in a safe range, the TBC output field frequency is limited to 50 Hz ±0.5% or 59.94 Hz/60 Hz ±0.5% as default. If the field frequency of input video is beyond this range, the display will be scrolling.

Composite video formats are supported by the TBC. 480i/576i component formats can be supported by the TBC if needed.

3.3.2. VBI Post Processor
The VBI Post Processor is used to transmit VBI data to DTV over the HDMI/MHL connection.

In case the raw VBI data i.e. digitized luma portion of the incoming video signal, or Teletext need to be transmitted to DTV over HDMI/MHL, they are embedded into the video stream and transmitted. As the decoded VBI data, they can be transmitted over HDMI or MHL using Vendor Specific Info Frame (VSIF).

3.3.3. De-interlacer and Edge Smoother
De-interlacing is designed to convert an interlaced (480i/576i) video signal to a progressive (480p/576p) video signal. BOB de-interlacing method is adopted to reduce cost and power consumption. An edge smoother is included to reduce the saw tooth artifacts generated by de-interlacing and to improve the picture quality.

The de-interlacer and edge smoother must be used together with the TBC.

3.3.4. Color Processing
Color Processing (CP) enables brightness, contrast, saturation, and hue controls for end users. It supports YCbCr color space only.

3.3.5. Auto Phase Detection
The Auto Phase Detection (APD) is a module used to search for the phases that can generate the best display quality. The desired phases, in general, can generate sharp and stable images, if the input image meets certain criteria during phase detection period. APD is an automatic algorithm that can be enabled or disabled by software. It can be applied to both VGA and Component inputs.

3.3.6. Auto Position Calibration
The Auto Position Calibration (APC) detects the active picture area of input video signal and adjusts the output timing so that the final picture can fit to the display properly.

3.3.7. Auto Gain Calibration
Slight mismatch of analog input channels including offset and gain may impact the picture quality. The SiI8784 device has been designed to keep the mismatches in an acceptable range (<0.5 dB). It is still important to calibrate these mismatches in some cases to achieve the most accurate picture. To help manufacturers finish this process efficiently, an Auto Gain Calibration (AGCWIN) mechanism is designed in the SiI8784 device. This mechanism automatically measures the digitalized signal levels through the AGCWIN module, calculates the correct values, and stores them into the external SPI Flash memory. These values can be used by firmware in user mode to compensate the analog mismatches.
3.4. Dual-mode HDMI/MHL Transmitter

The SiI8784 device incorporates the latest HDMI 1.4 and MHL 2 dual-mode transmitter. It multiplexes video and audio data into the HDMI/MHL stream and performs TMDS encoding. It contains digital video data capture and its processing block, digital audio data capture and its processing block, HDMI/MHL transmitter, and PHY. Figure 3.6 shows the dual-mode HDMI/MHL transmitter diagram.

![Dual-mode HDMI/MHL Transmitter Diagram](image)

**Figure 3.6. Dual-mode HDMI/MHL Transmitter Diagram**

3.4.1. Video Data Capture Logic

The Video Data Capture Logic receives uncompressed digital video with a data width of 8 to 24 bits from the digital parallel video interface. The bus configurations support most standard video input formats as well as other widely used non-standard formats.

3.4.2. Video Processing Path

*Figure 3.7* shows the video data processing stages. Each of the processing blocks can be bypassed by setting the appropriate register bits.
The input processor can create DE, HSYNC, and VSYNC signals using the start of active video (SAV) and end of active video (EAV) codes within the ITU-R BT.656-format video stream.

### 3.4.2.1. Data Enable Generator

The transmitter includes logic to construct a DE signal from the incoming HSYNC, VSYNC, and clock. Registers are programmed to enable the DE signal to define the size of the active display region.

### 3.4.2.2. Combiner

The clock, data, and sync information is combined into a complete set of signals required for TMDS encoding. From here, the signals are manipulated by the register-selected video processing blocks.

### 3.4.2.3. 422 to 444 Up-sampler

Chrominance up-sampling and down-sampling increase or decrease the number of chrominance samples in each line of video. Up-sampling doubles the number of chrominance samples in each line, converting 4:2:2 sampled video to 4:4:4 sampled video.

### 3.4.2.4. 444 to 422 Decimation

Decimation reduces the number of chrominance samples in each line by half, converting 4:4:4 sampled video to 4:2:2 video.

### 3.4.2.5. Color Space Converters (CSC)

Two color space converters (CSCs) (YCbCr to RGB and RGB to YCbCr) are available to interface to the many video formats supplied by A/V processors and to provide full DVI backward compatibility. The CSC can be adjusted to perform standard-definition conversions (ITU.601) or high-definition conversions (ITU.709) by setting the appropriate registers.

#### RGB to YCbCr

The RGB→YCbCr color space converter can convert from video data RGB to standard definition or to high definition YCbCr formats. The HDMI AVI packet defines the color space of the incoming video.
SiI8784 Multi-format Analog Video Front-end with HDMI/MHL Transmitter

Table 3.4. Color Space Versus Video Format

<table>
<thead>
<tr>
<th>Video Format</th>
<th>Conversion</th>
<th>Formulas</th>
</tr>
</thead>
<tbody>
<tr>
<td>640 x 480</td>
<td>ITU-R BT.601</td>
<td>CE Mode 16-235 RGB</td>
</tr>
<tr>
<td>480i</td>
<td>ITU-R BT.601</td>
<td>Y = 0.299R’ + 0.587G’ + 0.114B’</td>
</tr>
<tr>
<td>576i</td>
<td>ITU-R BT.601</td>
<td>CB = -0.172R’ - 0.339G’ + 0.511B’ + 128</td>
</tr>
<tr>
<td>480p</td>
<td>ITU-R BT.601</td>
<td>CR = 0.511R’ - 0.428G’ - 0.083B’ + 128</td>
</tr>
<tr>
<td>576p</td>
<td>ITU-R BT.601</td>
<td></td>
</tr>
<tr>
<td>240p</td>
<td>ITU-R BT.601</td>
<td>Y = 0.213R’ + 0.715G’ + 0.072B’</td>
</tr>
<tr>
<td>288p</td>
<td>ITU-R BT.601</td>
<td>CB = -0.117R’ - 0.394G’ + 0.511B’ + 128</td>
</tr>
<tr>
<td>720p</td>
<td>ITU-R BT.709</td>
<td>CR = 0.511R’ - 0.464G’ - 0.047B’ + 128</td>
</tr>
<tr>
<td>1080i</td>
<td>ITU-R BT.709</td>
<td></td>
</tr>
<tr>
<td>1080p</td>
<td>ITU-R BT.709</td>
<td></td>
</tr>
</tbody>
</table>

YCbCr to RGB

The YCbCr→RGB color space converter allows MPEG decoders to interface with RGB-only inputs. The CSC can convert from YCbCr in standard-definition (ITU.601) or high-definition (ITU.709) to RGB. Refer to Table 3.5 for the detailed formulas. Note the difference between RGB range for CE modes and PC modes.

Table 3.5. YCbCr-to-Rgb Color Space Conversion Formula

<table>
<thead>
<tr>
<th>Format Change</th>
<th>Conversion</th>
<th>YCbCr Input Color Range</th>
<th>2, 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>YCbCr 16-235 Input(^2, 3) to RGB 16-235 Output(^2, 3)</td>
<td>601(^1)</td>
<td>R’ = Y + 1.371(Cr - 128)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>G’ = Y - 0.698(Cr - 128) - 0.336(Cb - 128)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>B’ = Y + 1.732(Cb - 128)</td>
<td></td>
</tr>
<tr>
<td>YCbCr 16-235 Input(^2, 3) to RGB 0-255 Output(^2, 3)</td>
<td>709(^1)</td>
<td>R’ = Y + 1.540(Cr - 128)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>G’ = Y - 0.459(Cr - 128) - 0.183(Cb - 128)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>B’ = Y + 1.816(Cb - 128)</td>
<td></td>
</tr>
<tr>
<td>YCbCr 16-235 Input(^2, 3) to RGB 0-255 Output(^2, 3)</td>
<td>601</td>
<td>R’ = 1.164((Y-16) + 1.371(Cr - 128))</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>G’ = 1.164((Y-16) - 0.698(Cr - 128) - 0.336(Cb - 128))</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>B’ = 1.164((Y-16) + 1.732(Cb - 128))</td>
<td></td>
</tr>
<tr>
<td>YCbCr 16-235 Input(^2, 3) to RGB 0-255 Output(^2, 3)</td>
<td>709</td>
<td>R’ = 1.164((Y-16) + 1.540(Cr - 128))</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>G’ = 1.164((Y-16) - 0.459(Cr - 128) - 0.183(Cb - 128))</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>B’ = 1.164((Y-16) + 1.816(Cb - 128))</td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. No clipping can be done.
2. For 10-bit deep color, all occurrences of the values 16, 128, 235, and 255 should be multiplied by 4.
3. For 12-bit deep color, all occurrences of the values 16, 128, 235, and 255 should be multiplied by 16.

3.4.2.6. RGB Range Expansion

The SiI8784 input processor can scale the input color from limited-range into full-range using the range expansion block. When enabled by itself, the range expansion block expands 16 – 235 limited-range data into 0 – 255 for each video channel. When the range expansion and the YCbCr to RGB color space converter are both enabled, the input conversion range for the Cr and Cr channels is 16 – 240.

3.4.2.7. RGB/YCbCr Range Compression

When enabled by itself, the Range Compression Block compresses 0 – 255 full-range data into 16 – 235 limited-range data for each video channel. When enabled with the RGB to YCbCr converter, this block compresses to 16 – 240 for the Cr and Cr channels. The color range scaling is linear.

3.4.2.8. Clipping

The clipping block, when enabled, clips the values of the output video to 16 – 235 for RGB video or the Y channel, and to 16 – 240 for the Cr and Cr channels.
3.4.2.9. Dither
The dither block dithers internally processed data to 8, 10, or 12 bits for output on the HDMI link.

3.4.2.10. HDCP Encryption Engine/XOR Mask
The HDCP encryption engine contains the logic necessary to encrypt the incoming audio and video data and includes support for HDCP authentication and repeater checks. The system microcontroller or microprocessor controls the encryption process by using a set sequence of register reads and writes. An algorithm uses HDCP keys and a Key Selector Value (KSV) stored in the on-board ROM to calculate a number that is then applied to an XOR mask. This process encrypts the audio and video data on a pixel-by-pixel basis during each clock cycle.

3.4.2.11. TMDS Digital Core
The TMDS digital core performs 8-to-10-bit TMDS encoding on the data received from the HDCP XOR mask. This data is sent to three TMDS differential data lines, along with a TMDS differential clock line. A resistor tied to the EXT_SWING pin controls the TMDS swing amplitude.

3.4.3. Audio Data Capture and Processing Logic
The SiI8784 device accepts digital audio over an S/PDIF interface, four I^S inputs, or eight one-bit audio inputs.

3.4.3.1. S/PDIF
The S/PDIF stream can carry 2-channel uncompressed PCM data (IEC 60958) or a compressed bit stream for multi-channel (IEC 61937) formats. The audio data capture logic forms the audio data into packets described in the HDMI Specification. The S/PDIF input supports audio sampling (Fs) rates from 32 to 192 kHz. A separate master clock input (MCLK), coherent with the S/PDIF input, is required for time-stamping purposes. Coherent means that the MCLK and S/PDIF have been created from the same clock source. This step usually uses the original MCLK to strobe out the S/PDIF from the sourcing chip. There is no setup or hold timing requirement on an input with respect to MCLK.

3.4.3.2. I^S
Four I^S inputs allow transmission of DVD-Audio or decoded Dolby Digital to A/V receivers and high-end displays. The interface works in slave mode, supports sample rate up to 192 kHz.

Register control allows the audio data to be down-sampled by one-half or one-fourth, so that the transmitter can be compatible with the attached display that supports lower sample rate audio only. Conversions from 192 to 48 kHz, from 176.4 to 44.1 kHz, from 96 to 48 kHz, and from 88.2 to 44.1 kHz are supported. Audio data can only be downsampled on 2-channel audio.

The appropriate registers must be configured to describe the audio format provided to the SiI8784 input processor. This information is passed over the HDMI link in the CEA-861D Audio Info (AI) packets.

Table 3.6 shows the MCLK frequencies that support seven audio sample rates.

<table>
<thead>
<tr>
<th>Table 3.6. Supported MCLK Frequencies</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Multiple of Fs</strong></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>128</td>
</tr>
<tr>
<td>192</td>
</tr>
<tr>
<td>256</td>
</tr>
<tr>
<td>384</td>
</tr>
<tr>
<td>512</td>
</tr>
<tr>
<td>768</td>
</tr>
<tr>
<td>1024</td>
</tr>
<tr>
<td>1152</td>
</tr>
</tbody>
</table>
3.5. Control Logic

3.5.1. Internal Microcontroller

As shown in Figure 3.1 on page 7, an 8-bit 8051 compatible microcontroller is integrated in the SiI8784 device. It contains 3 KB data RAM and 96 KB code RAM. The code can be loaded into code RAM from external SPI Flash or EEPROM memory automatically after power on. If the check sum of the code data is correct, the code will be executed. Otherwise the internal microcontroller is disabled and the chip can be controlled by external controller through I2C bus. The internal controller can access all the internal registers directly over the internal bus. The 8051 microcontroller runs at the crystal clock of 24 MHz.

When the booting procedure is finished, the SPI interface will be handed over to the 8051 SPI module so that firmware can read/write the external memory if needed.

The internal controller can also operate other peripherals through the I2C bus of the SiI8784 device by setting it to the master mode.

3.5.1.1. Data Structure of External SPI Memory

Figure 3.8 shows the memory structure which is required for the internal microcontroller to load the code correctly.

Figure 3.8. External Memory Structure

Table 3.7. Head Flags

<table>
<thead>
<tr>
<th>EEPROM/Flash Address</th>
<th>EEPROM/Flash Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>00000H</td>
<td>Head0 'S'</td>
</tr>
<tr>
<td>00001H</td>
<td>Head1 'I'</td>
</tr>
<tr>
<td>00002H</td>
<td>Head2 'M'</td>
</tr>
<tr>
<td>00003H</td>
<td>Head3 'G'</td>
</tr>
</tbody>
</table>

Note: The head flag will be four bytes ASCII code of 'S', 'I', 'M', 'G'.

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### Table 3.8. Info Bytes

<table>
<thead>
<tr>
<th>EEPROM/Flash Address</th>
<th>EEPROM/Flash Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>00004H</td>
<td>SPI PARAMETER.</td>
</tr>
<tr>
<td>00005H</td>
<td>Calibration Version (low byte)</td>
</tr>
<tr>
<td>00006H</td>
<td>Calibration Version.</td>
</tr>
<tr>
<td>00007H</td>
<td>Calibration Version (high byte).</td>
</tr>
<tr>
<td>00008H</td>
<td>Code Version (low byte).</td>
</tr>
<tr>
<td>00009H</td>
<td>Code Version.</td>
</tr>
<tr>
<td>0000AH</td>
<td>Code Version (high byte).</td>
</tr>
<tr>
<td>0000BH</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0000CH</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0000DH</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0000EH</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0000FH</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>

**Note:** The info bytes contain the information about the feature of Max read frequency of external EEPROM/Flash, the calibration version, and the code version. It occupies 12 bytes.

### Table 3.9. SPI Parameter

<table>
<thead>
<tr>
<th>SPI Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>2 MHz baud rate to access SPI Flash/EEPROM.</td>
</tr>
<tr>
<td>0x01</td>
<td>24 MHz baud rate to access SPI Flash/EEPROM.</td>
</tr>
</tbody>
</table>

### Table 3.10. Calibration Checksum

<table>
<thead>
<tr>
<th>EEPROM/Flash Address</th>
<th>EEPROM/Flash Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>0010EH</td>
<td>Calibration Checksum (low byte).</td>
</tr>
<tr>
<td>0010FH</td>
<td>Calibration Checksum (high byte).</td>
</tr>
</tbody>
</table>

**Note:** The calibration checksum is two bytes which locates at the last site of 256 size calibration data.

### Table 3.11. HW Configuration Data

<table>
<thead>
<tr>
<th>EEPROM/Flash Address</th>
<th>EEPROM/Flash Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>00110H</td>
<td>BT_SPI_PINMUX_SEL.</td>
</tr>
<tr>
<td>00H</td>
<td>00H – SPI function</td>
</tr>
<tr>
<td>01H</td>
<td>01H – Reserved. Don’t use</td>
</tr>
<tr>
<td>02H</td>
<td>02H – Reserved. Don’t use</td>
</tr>
<tr>
<td>00111H..0012FH</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>

### Table 3.12. 8051 Code Size

<table>
<thead>
<tr>
<th>EEPROM/Flash Address</th>
<th>EEPROM/Flash Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>00130H</td>
<td>Code Size (low byte).</td>
</tr>
<tr>
<td>00131H</td>
<td>Code Size.</td>
</tr>
<tr>
<td>00132H</td>
<td>Code Size (high byte).</td>
</tr>
</tbody>
</table>

### Table 3.13. HW Configuration Data and Code Checksum

<table>
<thead>
<tr>
<th>EEPROM/Flash Address</th>
<th>EEPROM/Flash Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>00133H + code size</td>
<td>Code Checksum0 (lowest byte).</td>
</tr>
<tr>
<td>00134H + code size</td>
<td>Code Checksum1.</td>
</tr>
<tr>
<td>00135H + code size</td>
<td>Code Checksum2.</td>
</tr>
<tr>
<td>00136H + code size</td>
<td>Code Checksum3 (highest byte).</td>
</tr>
</tbody>
</table>
The boot module tries to load data from external device and write into chip SRAM. The 8051 code content is written into the 96K bytes SRAM of 8051. The 256 system calibration is written into the high 3 K bytes SRAM in data memory. For details on the selection of the SPI Flash memory, refer to the relevant Application Note (SiI-AN-1108).

3.5.2. Registers
The register block incorporates all the registers required for configuring and managing the SiI8784 device. These registers are used to perform AFE processing, VDC processing, MHL/HDMI processing, and all other control functions.

3.5.3. I²C Bus
The local I²C slave bus provides the host with communication to the entire system. The controller I²C interface on the SiI8784 device (signals CSCL and CSDA) is a slave interface, which is capable of running up to 400 kHz.

All functions of the SiI8784 device are controlled and observed with I²C registers. Device addresses can be altered with the level of the CI2CA signal. Table 3.14 shows the device addresses as altered by the level of the CI2CA signal.

### Table 3.14. Control of Transmitter I²C Address with CI2CA Signal

<table>
<thead>
<tr>
<th>CI2CA = 0</th>
<th>CI2CA = 1</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x8C</td>
<td>0x8E</td>
<td>System Control and Status</td>
</tr>
<tr>
<td>0x84</td>
<td>0x84</td>
<td>VD_DPGA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VD_SIGNALROUTING</td>
</tr>
<tr>
<td>0x86</td>
<td>0x86</td>
<td>VD_VBI</td>
</tr>
<tr>
<td>0x8A</td>
<td>0x8A</td>
<td>VD_VDREG</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VD_ADCIF</td>
</tr>
<tr>
<td>0x92</td>
<td>0x92</td>
<td>VD_SYNCPROC</td>
</tr>
<tr>
<td>0x96</td>
<td>0x96</td>
<td>VD_ADCSTATUS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VD_VPP</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Edge Smooth</td>
</tr>
<tr>
<td></td>
<td></td>
<td>INT</td>
</tr>
<tr>
<td>0xDA</td>
<td>0xDA</td>
<td>FPGA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>APD</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ADC_WIN</td>
</tr>
<tr>
<td>0x9C</td>
<td>0x9C</td>
<td>VidPath</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Calibration</td>
</tr>
<tr>
<td>0x8D</td>
<td>0xD8</td>
<td>AFE</td>
</tr>
<tr>
<td>0x72</td>
<td>0x76</td>
<td>HW_TPI</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TX Page 0/2</td>
</tr>
<tr>
<td>0x7A</td>
<td>0x7E</td>
<td>TX Page 1</td>
</tr>
<tr>
<td>0x90</td>
<td>0x94</td>
<td>Reserved</td>
</tr>
<tr>
<td>0xC0</td>
<td>0xC4</td>
<td>CEC 1.6</td>
</tr>
<tr>
<td>0x60</td>
<td>0x60</td>
<td>TX PHY</td>
</tr>
<tr>
<td>0xC8</td>
<td>0xCC</td>
<td>CBUS</td>
</tr>
</tbody>
</table>

**Note:** When the internal microcontroller is enabled, the I²C bus is taken over by the firmware. It can work as both master and slave mode, and the addresses are alterable.

3.5.4. Interrupt
The SiI8784 device contains a configurable interrupt generator with an open-drain type output pin. It can be used to notify application processor (if there is application processor) to handle some events.

3.5.5. GPIOs
There are five general purpose IO pins on the SiI8784 device. Generally they can be used to detect the cable plug-in status, but they can be used for other purposes as well.
### Table 3.15. List of GPIOs

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Pull up/down</th>
<th>Reset Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO0$^1$</td>
<td>IO</td>
<td>Pull down</td>
<td>I</td>
</tr>
<tr>
<td>GPIO1</td>
<td>IO</td>
<td>Pull up</td>
<td>I</td>
</tr>
<tr>
<td>GPIO2</td>
<td>IO</td>
<td>Pull up</td>
<td>I</td>
</tr>
<tr>
<td>GPIO3</td>
<td>IO</td>
<td>Pull up</td>
<td>I</td>
</tr>
<tr>
<td>GPIO4</td>
<td>IO</td>
<td>Pull up</td>
<td>I</td>
</tr>
</tbody>
</table>

**Notes:**

1. GPIO0 is also used as CI2C A pin to decide the I2C slave address during reset.
2. The internal Pull up/down resistors are fixed and weak just to avoid floating input level when they are left unconnected. Peripheral circuits should not rely on them. 10 K or smaller resistors are recommended for external pull up/down circuit to override them if needed.
4. Electrical Specifications

4.1. Absolute Maximum Conditions

Table 4.1. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>VP2V5A</td>
<td>Analog Power for ADC</td>
<td>−0.3</td>
<td>—</td>
<td>3.0</td>
<td>V</td>
<td>1, 2</td>
</tr>
<tr>
<td>VP2V5D</td>
<td>Digital Power for ADC</td>
<td>−0.3</td>
<td>—</td>
<td>3.0</td>
<td>V</td>
<td>1, 2</td>
</tr>
<tr>
<td>VP2V5_SPLICER</td>
<td>Analog Power for SOG Slicer</td>
<td>−0.3</td>
<td>—</td>
<td>3.0</td>
<td>V</td>
<td>1, 2</td>
</tr>
<tr>
<td>VP1V0_PLL</td>
<td>Power for APLL and LLPLL</td>
<td>−0.3</td>
<td>—</td>
<td>1.2</td>
<td>V</td>
<td>1, 2</td>
</tr>
<tr>
<td>VCC10_TPLL</td>
<td>TCI PLL Power</td>
<td>−0.3</td>
<td>—</td>
<td>1.2</td>
<td>V</td>
<td>1, 2</td>
</tr>
<tr>
<td>AVCC_PPLL</td>
<td>Analog PLL Power of HDMI/MHLTX</td>
<td>−0.3</td>
<td>—</td>
<td>1.2</td>
<td>V</td>
<td>1, 2</td>
</tr>
<tr>
<td>AVCC</td>
<td>Power for HDMI/MHL TX</td>
<td>−0.3</td>
<td>—</td>
<td>1.2</td>
<td>V</td>
<td>1, 2</td>
</tr>
<tr>
<td>AVCC3V3_CBUS</td>
<td>Power for CBUS I/O</td>
<td>−0.3</td>
<td>—</td>
<td>4.0</td>
<td>V</td>
<td>1, 2</td>
</tr>
<tr>
<td>CVCC10</td>
<td>Power for Digital Core</td>
<td>−0.3</td>
<td>—</td>
<td>1.2</td>
<td>V</td>
<td>1, 2</td>
</tr>
<tr>
<td>VDDIO3V3</td>
<td>Power for Digital I/O</td>
<td>−0.3</td>
<td>—</td>
<td>4.0</td>
<td>V</td>
<td>1, 2</td>
</tr>
<tr>
<td>XTALVCC33</td>
<td>Power for XTAL</td>
<td>−0.3</td>
<td>—</td>
<td>4.0</td>
<td>V</td>
<td>1, 2</td>
</tr>
<tr>
<td>V_D</td>
<td>Digital Input Voltage</td>
<td>−0.3</td>
<td>—</td>
<td>VDDIO + 0.3</td>
<td>V</td>
<td>1, 2</td>
</tr>
<tr>
<td>V_O</td>
<td>Digital Output Voltage</td>
<td>−0.3</td>
<td>—</td>
<td>VDDIO + 0.3</td>
<td>V</td>
<td>1, 2</td>
</tr>
<tr>
<td>AV_I</td>
<td>Analog Input Voltage</td>
<td>−0.3</td>
<td>—</td>
<td>VP2V5A + 0.3</td>
<td>V</td>
<td>1, 2</td>
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<tr>
<td>V5V_Tolerant</td>
<td>Input Voltage on 5 V Tolerant Pins</td>
<td>−0.3</td>
<td>—</td>
<td>5.5</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>T_J</td>
<td>Junction Temperature</td>
<td>—</td>
<td>—</td>
<td>125</td>
<td>°C</td>
<td>—</td>
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<tr>
<td>T_STG</td>
<td>Storage Temperature</td>
<td>−65</td>
<td>—</td>
<td>150</td>
<td>°C</td>
<td>—</td>
</tr>
</tbody>
</table>

Notes:
1. Permanent device damage can occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under normal operating conditions.
## 4.2. Normal Operating Conditions

### Table 4.2. Normal Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>VP2V5A</td>
<td>Analog Power for ADC</td>
<td>2.375</td>
<td>2.50</td>
<td>2.625</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{VP2V5A}$</td>
<td>Total Current Consumption of VP2V5A</td>
<td>—</td>
<td>90</td>
<td>—</td>
<td>mA</td>
<td>4, 8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>58</td>
<td>—</td>
<td>mA</td>
<td>5, 8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>68</td>
<td>—</td>
<td>mA</td>
<td>6, 8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>78</td>
<td>—</td>
<td>mA</td>
<td>7, 8</td>
</tr>
<tr>
<td>VP2V5D</td>
<td>Digital Power for ADC</td>
<td>2.375</td>
<td>2.50</td>
<td>2.625</td>
<td>V</td>
<td>—</td>
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<tr>
<td>$I_{VP2V5D}$</td>
<td>Total Current Consumption of VP2V5D</td>
<td>—</td>
<td>9</td>
<td>—</td>
<td>mA</td>
<td>4, 8</td>
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<td>5</td>
<td>—</td>
<td>mA</td>
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<td></td>
<td>—</td>
<td>6</td>
<td>—</td>
<td>mA</td>
<td>6, 8</td>
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<td>7</td>
<td>—</td>
<td>mA</td>
<td>7, 8</td>
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<tr>
<td>VP2V5_SLICER</td>
<td>Analog Power for SOG Slicer</td>
<td>2.375</td>
<td>2.50</td>
<td>2.625</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>$I_{VP2V5_SLICER}$</td>
<td>Current Consumption of VP2V5_SLICER</td>
<td>—</td>
<td>3</td>
<td>—</td>
<td>mA</td>
<td>6, 8</td>
</tr>
<tr>
<td>VP1V0_PLL</td>
<td>Power for APLL and LLPLL</td>
<td>0.95</td>
<td>1.00</td>
<td>1.05</td>
<td>V</td>
<td>3</td>
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<tr>
<td>$I_{VP1V0_PLL}$</td>
<td>Current Consumption of VP1V0_PLL</td>
<td>—</td>
<td>20</td>
<td>—</td>
<td>mA</td>
<td>7, 8</td>
</tr>
<tr>
<td>VCC10_TPLL</td>
<td>TCI PLL Power</td>
<td>0.95</td>
<td>1.00</td>
<td>1.05</td>
<td>V</td>
<td>3</td>
</tr>
<tr>
<td>$I_{VCC10_TPLL}$</td>
<td>Current Consumption of VCC10_TPLL</td>
<td>—</td>
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<td>—</td>
<td>mA</td>
<td>5, 8</td>
</tr>
<tr>
<td>AVCC_PLL</td>
<td>Analog PLL Power of HDMI/MHLTX</td>
<td>0.95</td>
<td>1.00</td>
<td>1.05</td>
<td>V</td>
<td>3</td>
</tr>
<tr>
<td>$I_{AVCC_PLL}$</td>
<td>Current Consumption of AVCC_PLL</td>
<td>—</td>
<td>4.5</td>
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<td>mA</td>
<td>7, 8</td>
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<td>AVCC</td>
<td>Power for HDMI/MHL TX</td>
<td>0.95</td>
<td>1.00</td>
<td>1.05</td>
<td>V</td>
<td>—</td>
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<tr>
<td>$I_{AVCC}$</td>
<td>Current Consumption of AVCC</td>
<td>—</td>
<td>4.5</td>
<td>—</td>
<td>mA</td>
<td>7, 8</td>
</tr>
<tr>
<td>CVCC10</td>
<td>Power for Digital Core</td>
<td>0.95</td>
<td>1.00</td>
<td>1.05</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>$I_{CVCC10}$</td>
<td>Total Current Consumption of CVCC10</td>
<td>—</td>
<td>70</td>
<td>—</td>
<td>mA</td>
<td>4, 8</td>
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<td></td>
<td></td>
<td>—</td>
<td>65</td>
<td>—</td>
<td>mA</td>
<td>5, 8</td>
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<td></td>
<td></td>
<td>—</td>
<td>80</td>
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<td>mA</td>
<td>6, 8</td>
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<td></td>
<td>—</td>
<td>85</td>
<td>—</td>
<td>mA</td>
<td>7, 8</td>
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<td>85</td>
<td>—</td>
<td>mA</td>
<td>4, 9</td>
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<td></td>
<td>—</td>
<td>70</td>
<td>—</td>
<td>mA</td>
<td>5, 9</td>
</tr>
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<td></td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>mA</td>
<td>6, 9</td>
</tr>
<tr>
<td>$I_{VDDIO3V3}$</td>
<td>Current Consumption of VDDIO3V3</td>
<td>—</td>
<td>2</td>
<td>—</td>
<td>mA</td>
<td>4, 8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>2</td>
<td>—</td>
<td>mA</td>
<td>5, 8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>7</td>
<td>—</td>
<td>mA</td>
<td>6, 8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>8</td>
<td>—</td>
<td>mA</td>
<td>7, 8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>40</td>
<td>—</td>
<td>mA</td>
<td>4, 9</td>
</tr>
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<td></td>
<td></td>
<td>—</td>
<td>55</td>
<td>—</td>
<td>mA</td>
<td>5, 9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>60</td>
<td>—</td>
<td>mA</td>
<td>6, 9</td>
</tr>
<tr>
<td>AVCC3V3_CBUS</td>
<td>Power for CBUS I/O</td>
<td>3.135</td>
<td>3.30</td>
<td>3.465</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>$I_{AVCC3V3_CBUS}$</td>
<td>Current Consumption of AVCC3V3_CBUS</td>
<td>—</td>
<td>8</td>
<td>—</td>
<td>mA</td>
<td>6, 9</td>
</tr>
<tr>
<td>XTALVCC33</td>
<td>Power for XTAL</td>
<td>3.135</td>
<td>3.30</td>
<td>3.465</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>$I_{XTALVCC33}$</td>
<td>Current Consumption of XTALVCC33</td>
<td>—</td>
<td>3.5</td>
<td>—</td>
<td>mA</td>
<td>6, 8</td>
</tr>
<tr>
<td>TA</td>
<td>Ambient Temperature (with power applied)</td>
<td>0</td>
<td>25</td>
<td>70</td>
<td>°C</td>
<td>—</td>
</tr>
<tr>
<td>$\Theta_{ja}$</td>
<td>Ambient Thermal Resistance (Theta JA)</td>
<td>—</td>
<td>—</td>
<td>25.6</td>
<td>°C/W</td>
<td>1</td>
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</table>
### Table 4.2. Normal Operating Conditions (Continued)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>$$\Theta_{jc}$$</td>
<td>Case Thermal Resistance (Theta JC)</td>
<td>—</td>
<td>—</td>
<td>11.9</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

**Notes:**
1. Airflow at 0 m/s. Package ePad soldered to PCB.
2. The power ripple must be below 60 mVpp to avoid video quality detrition.
3. Avoid any noise coupling to PLL power rails.
5. Measured with CVBS input.
6. Measured with YPbPr 1080p60 input.
7. Measured with UXGA60 input.
8. HDMI output mode.
9. MHL output mode.

### 4.3. ESD Specifications

#### Table 4.3. ESD Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Latch up</td>
<td>ESD Latch up</td>
<td>± 200</td>
<td>—</td>
<td>—</td>
<td>mA</td>
<td>1, 2</td>
</tr>
<tr>
<td>HBM</td>
<td>Human Body Model</td>
<td>2000</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>3</td>
</tr>
<tr>
<td>MM</td>
<td>Machine Model</td>
<td>200</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>4</td>
</tr>
<tr>
<td>CDM</td>
<td>Charged Device Model</td>
<td>500</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>5</td>
</tr>
</tbody>
</table>

**Notes:**
1. At 70 °C.
2. Measured as per JESD78B standard.
3. Measured as per JESD22-A114 standard.
4. Measured as per JESD22-A115 standard.
5. Measured as per JESD22-C101 standard.
4.4. DC Specifications

Table 4.4. Digital I/O Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital Inputs</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIL</td>
<td>Input Low Voltage</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>VIH</td>
<td>Input High Voltage</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>2.0</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>VTH+</td>
<td>Schmitt Trigger LOW to HIGH Threshold</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>1.61</td>
<td>1.69</td>
<td>1.77</td>
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<tr>
<td>VTH-</td>
<td>Schmitt Trigger HIGH to LOW threshold</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>1.18</td>
<td>1.27</td>
<td>1.35</td>
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<td>IIL</td>
<td>Input Leakage Current</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>μA</td>
<td>1</td>
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<tr>
<td>RPU</td>
<td>Pull-up Resistor</td>
<td>—</td>
<td>27</td>
<td>38</td>
<td>59</td>
<td>KΩ</td>
<td>1</td>
</tr>
<tr>
<td>RPD</td>
<td>Pull-down Resistor</td>
<td>—</td>
<td>31</td>
<td>46</td>
<td>80</td>
<td>KΩ</td>
<td>1</td>
</tr>
<tr>
<td>VTH-DDC</td>
<td>Schmitt Trigger LOW to HIGH Threshold of DSCL and DSDA Pins</td>
<td>—</td>
<td>3</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>VTH-DDC</td>
<td>Schmitt Trigger HIGH to LOW Threshold of DSCL and DSDA Pins</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>1.5</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>VTH-CEC</td>
<td>Schmitt Trigger LOW to HIGH Threshold of CEC Pin</td>
<td>—</td>
<td>2</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>VTH-CEC</td>
<td>Schmitt Trigger HIGH to LOW Threshold of CEC Pin</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>RPU-CEC</td>
<td>Pull-up Resistor on CEC Pin</td>
<td>—</td>
<td>24.3</td>
<td>27</td>
<td>29.7</td>
<td>KΩ</td>
<td>—</td>
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<tr>
<td>VTH+DCC</td>
<td>Schmitt Trigger LOW to HIGH Threshold of LSCL and LSDA Pins</td>
<td>—</td>
<td>2.0</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>VTH-DCC</td>
<td>Schmitt Trigger HIGH to LOW Threshold of LSCL and LSDA Pins</td>
<td>—</td>
<td>3.0</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>3</td>
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<tr>
<td>Digital Outputs</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOH</td>
<td>HIGH-level Output Voltage</td>
<td>IOH = 8mA</td>
<td>2.4</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>VOL</td>
<td>LOW-level Output Voltage</td>
<td>IOL = –8mA</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>IOLZ</td>
<td>Tri-state Output Leakage Current</td>
<td>—</td>
<td>—10</td>
<td>—</td>
<td>10</td>
<td>μA</td>
<td>1</td>
</tr>
<tr>
<td>VOH-CEC</td>
<td>HIGH-level Output Voltage of CEC Pin</td>
<td>IOH = 100μA</td>
<td>2.5</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>VOL-CEC</td>
<td>LOW-level Output Voltage of CEC Pin</td>
<td>IOL = –100μA</td>
<td>—</td>
<td>—</td>
<td>0.4</td>
<td>V</td>
<td>—</td>
</tr>
</tbody>
</table>

Notes:
1. Applies to general digital IOs.
2. Compatible to 3.3 V I/O level in default.
3. Compatible to 5 V DDC level (need to be configured by register).

Table 4.5. HDMI TMDS Output DC Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSWING</td>
<td>Single-ended Output Swing Voltage</td>
<td>RLOAD = 50 Ω</td>
<td>400</td>
<td>—</td>
<td>600</td>
<td>mV</td>
</tr>
<tr>
<td>VH</td>
<td>Single-ended High-level Output Voltage</td>
<td>—</td>
<td>AVCC – 200</td>
<td>—</td>
<td>AVCC + 10</td>
<td>mV</td>
</tr>
<tr>
<td>VL</td>
<td>Single-ended Low-level Output Voltage</td>
<td>—</td>
<td>AVCC – 700</td>
<td>—</td>
<td>AVCC – 400</td>
<td>mV</td>
</tr>
<tr>
<td>IDDS</td>
<td>Differential output short-circuit current</td>
<td>VOUT = 0 V</td>
<td>—</td>
<td>—</td>
<td>5</td>
<td>μA</td>
</tr>
</tbody>
</table>
### Table 4.6. MHL TMDS Output DC Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSE_HIGH</td>
<td>Single-ended HIGH-level Output voltage</td>
<td>VTERM - 540</td>
<td>—</td>
<td>—</td>
<td>VTERM + 10</td>
<td>mV</td>
</tr>
<tr>
<td>VSE_LOW</td>
<td>Single-ended LOW-level Output voltage</td>
<td>VTERM - 1760</td>
<td>—</td>
<td>—</td>
<td>VTERM - 700</td>
<td>mV</td>
</tr>
<tr>
<td>VOFF*</td>
<td>Single-ended Standby (off) Output Voltage</td>
<td>VTERM - 10</td>
<td>—</td>
<td>—</td>
<td>VTERM + 10</td>
<td>mV</td>
</tr>
<tr>
<td>VDFSWING</td>
<td>Differential Output Swing Amplitude</td>
<td>RLOAD = 50 Ω</td>
<td>600</td>
<td>—</td>
<td>1000</td>
<td>mV</td>
</tr>
<tr>
<td>VCMSWING</td>
<td>Common Mode Output Swing</td>
<td>RLOAD = 50 Ω single-ended</td>
<td>360</td>
<td>—</td>
<td>Min (720, 0.85×VDFSWING)</td>
<td>mV</td>
</tr>
</tbody>
</table>

* Note:
VOFF is the source output voltage when terminated to VTERM through R_T1, and the source device is in standby mode or power off mode.

### Table 4.7. CBUS DC Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VTERM_CBUS</td>
<td>CBUS Termination Voltage</td>
<td>—</td>
<td>1.7</td>
<td>—</td>
<td>1.9</td>
<td>V</td>
</tr>
<tr>
<td>VIH_CBUS</td>
<td>HIGH-level Input Voltage</td>
<td>—</td>
<td>1.0</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>Vil_CBUS</td>
<td>LOW-level Input Voltage</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>0.6</td>
<td>V</td>
</tr>
<tr>
<td>VOH_CBUS</td>
<td>HIGH-level Output Voltage</td>
<td>IOVCC18 = 1.8 V, 85 °C</td>
<td>1.5</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>VOL_CBUS</td>
<td>LOW-level Output Voltage</td>
<td>IOVCC18 = 1.8 V, 85 °C</td>
<td>—</td>
<td>—</td>
<td>0.2</td>
<td>V</td>
</tr>
<tr>
<td>IOH_CBUS</td>
<td>HIGH-output Drive Current</td>
<td>VOH = 1.5 V</td>
<td>2</td>
<td>—</td>
<td>—</td>
<td>mA</td>
</tr>
<tr>
<td>IOL_CBUS</td>
<td>LOW-output Drive Current</td>
<td>VOL = 0.2 V</td>
<td>300</td>
<td>—</td>
<td>—</td>
<td>μA</td>
</tr>
<tr>
<td>IL/ILH</td>
<td>Input Leakage Current</td>
<td>High-impedance</td>
<td>—1.0</td>
<td>—</td>
<td>1.0</td>
<td>kΩ</td>
</tr>
<tr>
<td>ZCBUS_SRC_DISCOVER</td>
<td>Pull-up Resistance – Discovery</td>
<td>—</td>
<td>9</td>
<td>10</td>
<td>11</td>
<td>kΩ</td>
</tr>
<tr>
<td>ZCBUS_SRC_ON</td>
<td>Pull-up Resistance – ON</td>
<td>—</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>kΩ</td>
</tr>
<tr>
<td>ZRID_MHL_ACCEPT</td>
<td>R_ID range identified as MHL</td>
<td>—</td>
<td>800</td>
<td>1000</td>
<td>1200</td>
<td>Ω</td>
</tr>
<tr>
<td>ZRID_MHL_REJECT</td>
<td>R_ID identified as not MHL</td>
<td>—</td>
<td>&lt;500</td>
<td>—</td>
<td>&gt;1600</td>
<td>Ω</td>
</tr>
</tbody>
</table>
4.5. AC Specifications

Table 4.8. Analog Front-end Electrical Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>Input Capacitance</td>
<td>—</td>
<td>—</td>
<td>5</td>
<td>—</td>
<td>pF</td>
</tr>
<tr>
<td>$V_{FSR}$</td>
<td>Analog Input Range</td>
<td>—</td>
<td>0.3</td>
<td>1.2</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>—</td>
<td>Clamp Level</td>
<td>—</td>
<td>0.25</td>
<td>0.85</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OAR}$</td>
<td>Offset Adjustment Range</td>
<td>—</td>
<td>−0.5</td>
<td>—</td>
<td>+0.5</td>
<td>V</td>
</tr>
<tr>
<td>—</td>
<td>Offset Adjustment Resolution</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>Bits</td>
</tr>
<tr>
<td>BW</td>
<td>Input Analog Filter Bandwidth</td>
<td>—</td>
<td>50</td>
<td>—</td>
<td>600</td>
<td>MHz</td>
</tr>
<tr>
<td>—</td>
<td>Gain Adjustment Range</td>
<td>—</td>
<td>−6</td>
<td>—</td>
<td>+ 6</td>
<td>dB</td>
</tr>
</tbody>
</table>

**A/D Converters**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>Conversion Rate</td>
<td>—</td>
<td>—</td>
<td>25</td>
<td>—</td>
<td>170</td>
</tr>
<tr>
<td>N</td>
<td>ADC Resolution</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>Bits</td>
</tr>
<tr>
<td>INL</td>
<td>Integral Nonlinearity</td>
<td>580 mVpp, 2.8 kHz Ramp Wave Sampling Rate: 55 MHz PGA Gain: 0 dB LPF Bandwidth: 50 MHz</td>
<td>—</td>
<td>—</td>
<td>4</td>
<td>—</td>
</tr>
<tr>
<td>DNL</td>
<td>Differential Nonlinearity</td>
<td>300 mVpp, 1.1 MHz Sine Wave Sampling Rate: 165 MHz PGA Gain: 0 dB LPF Bandwidth: 400 MHz</td>
<td>—</td>
<td>—</td>
<td>1</td>
<td>—</td>
</tr>
<tr>
<td>NMC</td>
<td>No Missing Codes</td>
<td>—</td>
<td>—</td>
<td>Guaranteed</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>ENOB</td>
<td>Effective Number Of Bits</td>
<td>300 mVpp, 1.1 MHz Sine Wave Sampling Rate: 165 MHz PGA Gain: 0 dB LPF Bandwidth: 400 MHz</td>
<td>—</td>
<td>7.5</td>
<td>—</td>
<td>Bits</td>
</tr>
</tbody>
</table>

**PLL**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>Clock Frequency Range</td>
<td>—</td>
<td>—</td>
<td>25</td>
<td>—</td>
<td>170</td>
</tr>
<tr>
<td>—</td>
<td>Period Jitter</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>450</td>
<td>ps</td>
</tr>
<tr>
<td>—</td>
<td>Phase Adjustment</td>
<td>—</td>
<td>—</td>
<td>11.25</td>
<td>—</td>
<td>Degree/Step</td>
</tr>
<tr>
<td>—</td>
<td>Duty Cycle</td>
<td>—</td>
<td>—</td>
<td>45</td>
<td>50</td>
<td>55</td>
</tr>
</tbody>
</table>

**Video Buffer**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>DP</td>
<td>Differential Phase</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>4</td>
<td>Degrees</td>
</tr>
<tr>
<td>DG</td>
<td>Differential Gain</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>4</td>
<td>%</td>
</tr>
<tr>
<td>THD</td>
<td>Total Harmonic Distortion</td>
<td>700 mVpp, 4 MHz Sine Wave Load = 37.5 Ω Internal Clamp: OFF</td>
<td>—</td>
<td>−48</td>
<td>—</td>
<td>dB</td>
</tr>
</tbody>
</table>
### Table 4.9. HDMI/MHL Output AC Timing Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>FMHL</td>
<td>Link Clock Frequency</td>
<td>—</td>
<td>25</td>
<td>—</td>
<td>75</td>
<td>MHz</td>
</tr>
<tr>
<td>FPPIXEL</td>
<td>Pixel Clock Frequency</td>
<td>—</td>
<td>25</td>
<td>—</td>
<td>75</td>
<td>MHz</td>
</tr>
<tr>
<td>TMHL</td>
<td>Link Clock Period</td>
<td>—</td>
<td>13.33</td>
<td>—</td>
<td>40</td>
<td>ns</td>
</tr>
<tr>
<td>TBIT</td>
<td>Bit Time on Link</td>
<td>—</td>
<td>—</td>
<td>0.444</td>
<td>—</td>
<td>1.33</td>
</tr>
<tr>
<td>TR_DF</td>
<td>Differential Swing LOW-to-HIGH Transition Time</td>
<td>$R_{\text{LOAD}} = 100 \Omega$ Differential Mode</td>
<td>75</td>
<td>—</td>
<td>—</td>
<td>ps</td>
</tr>
<tr>
<td>TF_DF</td>
<td>Differential Swing HIGH-to-LOW Transition Time</td>
<td>$R_{\text{LOAD}} = 100 \Omega$ Differential Mode</td>
<td>75</td>
<td>—</td>
<td>—</td>
<td>ps</td>
</tr>
<tr>
<td>TR_CM</td>
<td>Common Mode Clock Swing LOW-to-HIGH Transition Time</td>
<td>$R_{\text{LOAD}} = 30 \Omega$ Common Mode</td>
<td>600</td>
<td>—</td>
<td>2500</td>
<td>ps</td>
</tr>
<tr>
<td>TF_CM</td>
<td>Common Mode Clock Swing HIGH-to-LOW Transition Time</td>
<td>$R_{\text{LOAD}} = 30 \Omega$ Common Mode</td>
<td>600</td>
<td>—</td>
<td>2500</td>
<td>ps</td>
</tr>
<tr>
<td>TSKEW_DF</td>
<td>Differential Intrapair Skew</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td>ps</td>
</tr>
<tr>
<td>TSKEW_CM</td>
<td>Common Mode Intrapair Skew</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td>ps</td>
</tr>
<tr>
<td>%TMHL</td>
<td>Clock Duty Cycle</td>
<td>—</td>
<td>35</td>
<td>—</td>
<td>65</td>
<td>%</td>
</tr>
<tr>
<td>TMJIT</td>
<td>MHL Clock Jitter</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>0.25T_{\text{BIT}}+200</td>
<td>ps</td>
</tr>
</tbody>
</table>

### Table 4.10. CBUS Timing Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>T_RISE</td>
<td>Rise Time</td>
<td>CL = 560 pF</td>
<td>5</td>
<td>—</td>
<td>200</td>
<td>ns</td>
<td>—</td>
</tr>
<tr>
<td>T_FALL</td>
<td>Fall Time</td>
<td>CL = 560 pF</td>
<td>5</td>
<td>—</td>
<td>200</td>
<td>ns</td>
<td>—</td>
</tr>
<tr>
<td>ΔT_{RF}</td>
<td>Rise-to-Fall Time Difference</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>ns</td>
<td>—</td>
</tr>
<tr>
<td>T_BIT</td>
<td>Bit Time (1 MHz)</td>
<td>—</td>
<td>0.8</td>
<td>—</td>
<td>1.2</td>
<td>µsec</td>
<td>—</td>
</tr>
<tr>
<td>T_SRC_PULSE_WIDTH</td>
<td>Discovery Pulse Width (High Time, Float Time)</td>
<td>—</td>
<td>80</td>
<td>100</td>
<td>120</td>
<td>µsec</td>
<td>—</td>
</tr>
<tr>
<td>T_SRC_CONN</td>
<td>CBUS HIGH detect to connected state</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>240</td>
<td>µsec</td>
<td>1</td>
</tr>
<tr>
<td>T_CBUS_SRC_ON</td>
<td>Connected State to ZCBUS_SRC_ON enabled</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>120</td>
<td>µsec</td>
<td>—</td>
</tr>
<tr>
<td>T_ARB</td>
<td>Connected state to First CBUS Packet allowed</td>
<td>—</td>
<td>500</td>
<td>—</td>
<td>—</td>
<td>µsec</td>
<td>2</td>
</tr>
<tr>
<td>N_SRC_PULSE_COUNT</td>
<td>Discovery Pulse Count attempted</td>
<td>—</td>
<td>6</td>
<td>—</td>
<td>20</td>
<td>pulses</td>
<td>3</td>
</tr>
<tr>
<td>T_BIT_VARY_PACKET</td>
<td>Bit Time variation within the packet</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>1%</td>
<td>T_{\text{BIT}}</td>
<td>4</td>
</tr>
</tbody>
</table>

**Notes:**

1. This parameter is the length of time from when the source detects a HIGH on CBUS (held HIGH by the sink at the end of a discovery drive-and-float pulse), to when the source switches CBUS impedance to ZCBUS\_SRC\_ON and CBUS becomes active. *Active* means ready to receive the first packet.
2. Source and sink must wait at least this long before beginning first arbitration on CBUS.
3. A sink that detects at least $N_{\text{SRC\_PULSE\_COUNT}}$ changes its pull-down resistance on CBUS from ZCBUS\_SINK\_DISCOVER to ZCBUS\_SINK\_ON.
4. Bits driven by the initiator within one packet should match the mean bit time in the packet by this limit.
Table 4.11. I2S Audio Input Port Timing Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td>FS_I2S</td>
<td>Sample Rate</td>
<td>—</td>
<td>32</td>
<td>—</td>
<td>192</td>
<td>kHz</td>
<td>—</td>
</tr>
<tr>
<td>TSCKCYC</td>
<td>I2S Cycle Time</td>
<td>—</td>
<td>—</td>
<td>1.0</td>
<td>—</td>
<td>UI</td>
<td>Figure 5.4</td>
</tr>
<tr>
<td>TSCKDUTY</td>
<td>I2S Duty Cycle</td>
<td>—</td>
<td>90</td>
<td>—</td>
<td>110</td>
<td>%UI</td>
<td>Figure 5.4</td>
</tr>
<tr>
<td>T12SSU</td>
<td>I2S Setup Time</td>
<td>—</td>
<td>15</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>Figure 5.4</td>
</tr>
<tr>
<td>T12SHD</td>
<td>I2S Hold Time</td>
<td>—</td>
<td>1</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>Figure 5.4</td>
</tr>
</tbody>
</table>

Notes:
1. Proportional to unit time (UI), according to the sample rate. Refer to the I2S or S/PDIF Specifications.
2. Audio pipeline delay measured from transmitter input signals to TMDS output. The video path delay is insignificant.

Table 4.12. S/PDIF Input Port Timing Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Figure</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>FS_SPDIF</td>
<td>Sample Rate</td>
<td>—</td>
<td>32</td>
<td>—</td>
<td>192</td>
<td>kHz</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>TSPCYC</td>
<td>S/PDIF Cycle Time</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>2.0</td>
<td>UI</td>
<td>—</td>
<td>1</td>
</tr>
<tr>
<td>TSPDUTY</td>
<td>S/PDIF Duty Cycle</td>
<td>—</td>
<td>90</td>
<td>—</td>
<td>110</td>
<td>%UI</td>
<td>Figure 5.5</td>
<td>1</td>
</tr>
<tr>
<td>TAUDDLY</td>
<td>Audio Pipeline Delay</td>
<td>—</td>
<td>—</td>
<td>30</td>
<td>70</td>
<td>μs</td>
<td>—</td>
<td>2</td>
</tr>
</tbody>
</table>

Notes:
1. All standard-mode (100 kHz) I2C timing requirements are guaranteed by design. These timings apply to the slave I2C port (signals LSDA and LSCL).
2. Operation of I2C signals above 100 kHz is defined by LVTTL levels V\text{IH}, V\text{IL}, V\text{OH}, and V\text{OL} (see Table 4.4 on page 26). For these levels, I2C speeds up to 400 kHz are supported.
3. Reset on RESET\_N signal can be LOW as CVCC10 and VDDIO33 become stable, or pulled LOW for at least T\_RESET.

4.6. Control Signal Timing Specifications

Table 4.13. Control Signal Timing Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Figure</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>T_DCDVO</td>
<td>SDA Data Valid Delay from SCL</td>
<td>CL = 400pF</td>
<td>—</td>
<td>—</td>
<td>700</td>
<td>ns</td>
<td>Figure 5.1</td>
<td>1, 2</td>
</tr>
<tr>
<td>T_RESET</td>
<td>RESET_N Signal LOW Time required</td>
<td>—</td>
<td>—</td>
<td>5000</td>
<td>—</td>
<td>ns</td>
<td>Figure 5.2, 5.3</td>
<td>3</td>
</tr>
</tbody>
</table>

Notes:
1. All standard-mode (100 kHz) I2C timing requirements are guaranteed by design. These timings apply to the slave I2C port (signals LSDA and LSCL).
2. Operation of I2C signals above 100 kHz is defined by LVTTL levels V\text{IH}, V\text{IL}, V\text{OH}, and V\text{OL} (see Table 4.4 on page 26). For these levels, I2C speeds up to 400 kHz are supported.
3. Reset on RESET\_N signal can be LOW as CVCC10 and VDDIO33 become stable, or pulled LOW for at least T\_RESET.
5. Timing Diagrams

5.1. I²C Bus Timing Diagrams

5.2. Reset Timing Diagram

All power rails must be stable between its limits for Normal Operating Conditions for \( T_{\text{RESET}} \) before \( \text{RESET}_N \) is HIGH. \( \text{RESET}_N \) must be pulled LOW for \( T_{\text{RESET}} \) before accessing registers. This can be done by holding \( \text{RESET}_N \) LOW until \( T_{\text{RESET}} \) after stable power (Figure 5.2) or by pulling \( \text{RESET}_N \) LOW from a HIGH state (Figure 5.3) for at least \( T_{\text{RESET}} \).
5.3. Audio Timing Diagrams

![Audio Timing Diagrams](image)

**Figure 5.4. I^2S Timings**

![S/PDIF Timings](image)

**Figure 5.5. S/PDIF Timings**
6. Pin Diagram and Description

6.1. Pin Diagram

Figure 6.1 shows the pin diagram of the SiI8784 device. Individual pin functions are described in the Pin Descriptions section on the next page. The package is an 88-pin 10 mm × 10 mm, 0.9 mm pitch QFN with ePad, which must be connected to ground.

![SiI8784 Pin Diagram](image_url)
6.2. Pin Descriptions
The following tables provide the pin descriptions for the SiI8784 device.

6.2.1. AFE Pins

Table 6.1. AFE Input/Output Pins

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin</th>
<th>Type</th>
<th>Direction</th>
<th>Description</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>RED0</td>
<td>23</td>
<td>Analog</td>
<td>Input</td>
<td>RED Input 0.</td>
<td>1</td>
</tr>
<tr>
<td>RED1</td>
<td>24</td>
<td>Analog</td>
<td>Input</td>
<td>RED Input 1.</td>
<td>1</td>
</tr>
<tr>
<td>RED2</td>
<td>26</td>
<td>Analog</td>
<td>Input</td>
<td>RED Input 2.</td>
<td>1</td>
</tr>
<tr>
<td>REDN</td>
<td>27</td>
<td>Analog</td>
<td>Input</td>
<td>RED Negative Input.</td>
<td>2</td>
</tr>
<tr>
<td>BLU0</td>
<td>29</td>
<td>Analog</td>
<td>Input</td>
<td>BLUE Input 0.</td>
<td>1</td>
</tr>
<tr>
<td>BLU1</td>
<td>30</td>
<td>Analog</td>
<td>Input</td>
<td>BLUE Input 1.</td>
<td>1</td>
</tr>
<tr>
<td>BLU2</td>
<td>32</td>
<td>Analog</td>
<td>Input</td>
<td>BLUE Input 2.</td>
<td>1</td>
</tr>
<tr>
<td>BLUN</td>
<td>33</td>
<td>Analog</td>
<td>Input</td>
<td>BLUE Negative Input.</td>
<td>2</td>
</tr>
<tr>
<td>GRN0</td>
<td>34</td>
<td>Analog</td>
<td>Input</td>
<td>GREEN Input 0.</td>
<td>1</td>
</tr>
<tr>
<td>GRN1</td>
<td>35</td>
<td>Analog</td>
<td>Input</td>
<td>GREEN Input 1.</td>
<td>1</td>
</tr>
<tr>
<td>GRN2</td>
<td>37</td>
<td>Analog</td>
<td>Input</td>
<td>GREEN Input 2.</td>
<td>1</td>
</tr>
<tr>
<td>GRNN</td>
<td>38</td>
<td>Analog</td>
<td>Input</td>
<td>GREEN Negative Input.</td>
<td>2</td>
</tr>
<tr>
<td>CVBS0</td>
<td>40</td>
<td>Analog</td>
<td>Input</td>
<td>CVBS Input 0.</td>
<td>1</td>
</tr>
<tr>
<td>CVBS1</td>
<td>41</td>
<td>Analog</td>
<td>Input</td>
<td>CVBS Input 1.</td>
<td>1</td>
</tr>
<tr>
<td>CVBSN</td>
<td>43</td>
<td>Analog</td>
<td>Input</td>
<td>CVBS Negative Input.</td>
<td>2</td>
</tr>
<tr>
<td>AFE_REXT</td>
<td>44</td>
<td>Analog</td>
<td>Passive</td>
<td>External Bias Resistor.</td>
<td></td>
</tr>
<tr>
<td>SOG0</td>
<td>45</td>
<td>Analog</td>
<td>Input</td>
<td>SOG Input 0.</td>
<td></td>
</tr>
<tr>
<td>SOG1</td>
<td>46</td>
<td>Analog</td>
<td>Input</td>
<td>SOG Input 1.</td>
<td></td>
</tr>
<tr>
<td>FS_LINE1</td>
<td>47</td>
<td>Analog</td>
<td>Input</td>
<td>FS (SCART) or LINE1 (D-Terminal) Input.</td>
<td></td>
</tr>
<tr>
<td>FB_LINE2</td>
<td>51</td>
<td>Analog</td>
<td>Input</td>
<td>FB (SCART) or LINE2 (D-Terminal) Input.</td>
<td></td>
</tr>
<tr>
<td>LINE3</td>
<td>50</td>
<td>Analog</td>
<td>Input</td>
<td>LINE3 (D-Terminal) Input.</td>
<td></td>
</tr>
<tr>
<td>H50</td>
<td>52</td>
<td>Analog</td>
<td>Input</td>
<td>HSync Input.</td>
<td></td>
</tr>
<tr>
<td>VS0</td>
<td>59</td>
<td>LVTTL Schmitt Trigger 5 V Tolerant Pull-down</td>
<td>Input</td>
<td>VSync Input.</td>
<td></td>
</tr>
<tr>
<td>CVBS_OUT</td>
<td>48</td>
<td>Analog</td>
<td>Output</td>
<td>CVBS Output. Connect a 75 Ω resistor to ground when CVBS output is enabled.</td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. A 47nF couple capacitor is required when this pin is used.
2. Must connect a 0.1μF capacitor to ground when the corresponding input channel is used.
### 6.2.2. Audio Input Pins

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin</th>
<th>Type</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCK</td>
<td>72</td>
<td>LVTTL Schmitt Trigger 5 V Tolerant</td>
<td>Input</td>
<td>I²S Bit Clock Input.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pull-down</td>
<td></td>
<td></td>
</tr>
<tr>
<td>WS</td>
<td>74</td>
<td>LVTTL Schmitt Trigger 5 V Tolerant</td>
<td>Input</td>
<td>I²S Word Select Signal Input.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pull-down</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SDO_SPDIF</td>
<td>73</td>
<td>LVTTL Schmitt Trigger 5 V Tolerant</td>
<td>Input</td>
<td>I²S Data Input or SPDIF Input.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pull-down</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MCLK</td>
<td>75</td>
<td>LVTTL Schmitt Trigger 5 V Tolerant</td>
<td>Input</td>
<td>Master Clock Input.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pull-down</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### 6.2.3. Configuration and Control Pins

Table 6.3. Configuration and Control Pins

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin</th>
<th>Type</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INT</td>
<td>16</td>
<td>LVTTL Open Drain 5 V Tolerant</td>
<td>Output</td>
<td>Interrupt Pin.</td>
</tr>
<tr>
<td>RESET_N</td>
<td>15</td>
<td>LVTTL Schmitt Trigger 5 V Tolerant</td>
<td>Input</td>
<td>External Reset Signal. Active LOW.</td>
</tr>
<tr>
<td>LSCL</td>
<td>17</td>
<td>Open Drain Schmitt Trigger 5 V Tolerant</td>
<td>IO</td>
<td>Local I2C Bus Clock. Compatible with 5V and 3.3V I2C standard.</td>
</tr>
<tr>
<td>LSDA</td>
<td>18</td>
<td>Open Drain Schmitt Trigger 5 V Tolerant</td>
<td>IO</td>
<td>Local I2C Bus Data. Compatible with 5V and 3.3V I2C standard.</td>
</tr>
<tr>
<td>TMODE</td>
<td>84</td>
<td>Test Pin</td>
<td>Input</td>
<td>Reserved for test. This pin must be tied low during the normal operation.</td>
</tr>
<tr>
<td>GPIO0_CI2CA</td>
<td>85</td>
<td>LVTTL Schmitt Trigger 5 V Tolerant Pull-down</td>
<td>IO</td>
<td>General GPIOs. It also is used to select local I2C slave address during reset when the internal 8051 is not used.</td>
</tr>
<tr>
<td>GPIO1</td>
<td>86</td>
<td>LVTTL Schmitt Trigger 5 V Tolerant Pull-up</td>
<td>IO</td>
<td>General GPIOs.</td>
</tr>
<tr>
<td>GPIO2</td>
<td>19</td>
<td>LVTTL Schmitt Trigger 5 V Tolerant Pull-up</td>
<td>IO</td>
<td>General GPIOs.</td>
</tr>
<tr>
<td>GPIO3</td>
<td>20</td>
<td>LVTTL Schmitt Trigger 5 V Tolerant Pull-up</td>
<td>IO</td>
<td>General GPIOs.</td>
</tr>
<tr>
<td>GPIO4</td>
<td>21</td>
<td>LVTTL Schmitt Trigger 5 V Tolerant Pull-up</td>
<td>IO</td>
<td>General GPIOs.</td>
</tr>
<tr>
<td>HDMI_MHL_N</td>
<td>22</td>
<td>LVTTL Schmitt Trigger 5 V Tolerant Pull-up</td>
<td>Input</td>
<td>MHL and HDMI Select. High – HDMI Low – MHL</td>
</tr>
</tbody>
</table>
### 6.2.4. HDMI/MHL Data Pins

**Table 6.4. HDMI/MHL Data Pins**

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin</th>
<th>Type</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX0P_MHLD</td>
<td>6</td>
<td>TMDS</td>
<td>Output</td>
<td>TMDS Output Data Pairs for HDMI output. It is also used as MHL data pairs for MHL output.</td>
</tr>
<tr>
<td>TX0N_MHLDB</td>
<td>5</td>
<td>TMDS</td>
<td>Output</td>
<td>TMDS Output Data Pairs for HDMI output.</td>
</tr>
<tr>
<td>TX1P</td>
<td>8</td>
<td>TMDS</td>
<td>Output</td>
<td>TMDS Output Data Pairs for HDMI output.</td>
</tr>
<tr>
<td>TX1N</td>
<td>7</td>
<td>TMDS</td>
<td>Output</td>
<td>TMDS Output Data Pairs for HDMI output.</td>
</tr>
<tr>
<td>TX2P</td>
<td>11</td>
<td>TMDS</td>
<td>Output</td>
<td>TMDS Output Data Pairs for HDMI output.</td>
</tr>
<tr>
<td>TX2N</td>
<td>10</td>
<td>TMDS</td>
<td>Output</td>
<td>TMDS Output Data Pairs for HDMI output.</td>
</tr>
<tr>
<td>TXCP</td>
<td>3</td>
<td>TMDS</td>
<td>Output</td>
<td>TMDS Output Data Pairs for HDMI output.</td>
</tr>
<tr>
<td>TXCN</td>
<td>2</td>
<td>TMDS</td>
<td>Output</td>
<td>TMDS Output Data Pairs for HDMI output.</td>
</tr>
<tr>
<td>DSDA</td>
<td>80</td>
<td>Open Drain Schmitt Trigger 5 V Tolerant</td>
<td>IO</td>
<td>DDC Signals for HDMI output. Compatible with 5 V PC standard. Must connect pullup resistor to make sure DDC functions normal for both of HDMI and MHL output modes.</td>
</tr>
<tr>
<td>DSCL</td>
<td>81</td>
<td>LV TTL Schmitt Trigger 5 V Tolerant</td>
<td>Input</td>
<td>Hot Plug Detect Input. It is recommended to connect a 47 K pulldown resistor to ground for HDMI output.</td>
</tr>
<tr>
<td>HPD</td>
<td>79</td>
<td>LV TTL Schmitt Trigger 5 V Tolerant</td>
<td>Input</td>
<td>Hot Plug Detect Input. It is recommended to connect a 47 K pulldown resistor to ground for HDMI output.</td>
</tr>
<tr>
<td>CEC</td>
<td>83</td>
<td>CEC Pull-up</td>
<td>IO</td>
<td>CEC Port.</td>
</tr>
<tr>
<td>CBUS</td>
<td>87</td>
<td>Analog 5 V Tolerant</td>
<td>IO</td>
<td>CBUS Port. It can be connected to HPD pin in the case of outputting MHL over HDMI Type-A connector.</td>
</tr>
</tbody>
</table>

### 6.2.5. SPI Interface Pins

**Table 6.5. SPI Interface Pins**

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin</th>
<th>Type</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCLK</td>
<td>61</td>
<td>LV TTL Schmitt Trigger 5 V Tolerant Pull-down</td>
<td>Output</td>
<td>SPI clock output. Keep HiZ when RESET_N is low.</td>
</tr>
<tr>
<td>SDI</td>
<td>62</td>
<td>LV TTL Schmitt Trigger 5 V Tolerant Pull-down</td>
<td>Input</td>
<td>SPI Data Input.</td>
</tr>
<tr>
<td>SDO</td>
<td>63</td>
<td>LV TTL Schmitt Trigger 5 V Tolerant Pull-down</td>
<td>Output</td>
<td>SPI Data Output. Keep HiZ when RESET_N is low.</td>
</tr>
<tr>
<td>SCS</td>
<td>64</td>
<td>LV TTL Schmitt Trigger 5 V Tolerant Pull-down</td>
<td>Output</td>
<td>SPI Chip Enable. Keep HiZ when RESET_N is low.</td>
</tr>
</tbody>
</table>
6.2.6. Power and Ground Connections

Table 6.6. Power and Ground Connections

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin</th>
<th>Type</th>
<th>Description</th>
<th>Supply</th>
</tr>
</thead>
<tbody>
<tr>
<td>VP2VSA</td>
<td>25, 31, 36, 42</td>
<td>Power</td>
<td>Analog power for ADC.</td>
<td>2.5 V</td>
</tr>
<tr>
<td>VP2VSD</td>
<td>28, 39</td>
<td>Power</td>
<td>Digital power for ADC.</td>
<td>2.5 V</td>
</tr>
<tr>
<td>VP2V5_SPLICER</td>
<td>49</td>
<td>Power</td>
<td>Analog power for SOG Slicer.</td>
<td>2.5 V</td>
</tr>
<tr>
<td>VP1V0_PLL</td>
<td>53</td>
<td>Power</td>
<td>Power for PLL.</td>
<td>1.0 V</td>
</tr>
<tr>
<td>VCC10_TPLL</td>
<td>54</td>
<td>Power</td>
<td>Power for TCI PLL.</td>
<td>1.0 V</td>
</tr>
<tr>
<td>AVCC_PLL</td>
<td>12</td>
<td>Power</td>
<td>Analog power for HDMI/MHL TX PLL.</td>
<td>1.0 V</td>
</tr>
<tr>
<td>AVCC</td>
<td>4, 9</td>
<td>Power</td>
<td>Digital power for HDMI/MHL TX.</td>
<td>1.0 V</td>
</tr>
<tr>
<td>AVCC3V3_CBUS</td>
<td>1</td>
<td>Power</td>
<td>Analog power for CBUS.</td>
<td>3.3 V</td>
</tr>
<tr>
<td>CVCC10</td>
<td>13, 60, 65, 69, 82</td>
<td>Power</td>
<td>Power for Digital Core.</td>
<td>1.0 V</td>
</tr>
<tr>
<td>VDDIO33</td>
<td>14, 67, 78</td>
<td>Power</td>
<td>Power for Digital I/O.</td>
<td>3.3 V</td>
</tr>
<tr>
<td>XTALVCC33</td>
<td>55</td>
<td>Power</td>
<td>Power for XTAL.</td>
<td>3.3 V</td>
</tr>
<tr>
<td>XTALGND</td>
<td>58</td>
<td>Ground</td>
<td>Ground for XTAL.</td>
<td>0 V</td>
</tr>
<tr>
<td>AVSS</td>
<td>88</td>
<td>Ground</td>
<td>Ground for CBUS.</td>
<td>0 V</td>
</tr>
</tbody>
</table>

6.2.7. Crystal Pins

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin</th>
<th>Type</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>XTALIN</td>
<td>56</td>
<td>Analog</td>
<td>I</td>
<td>Input for Crystal.</td>
</tr>
<tr>
<td>XTALOUT</td>
<td>57</td>
<td>Analog</td>
<td>O</td>
<td>Output for Crystal.</td>
</tr>
</tbody>
</table>

6.2.8. Reserved Pins

Table 6.7. Reserved Pins

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D22_RSV</td>
<td>68</td>
<td>RSVD</td>
<td>Reserved.</td>
</tr>
<tr>
<td>D23_RSV</td>
<td>66</td>
<td>RSVD</td>
<td>Reserved.</td>
</tr>
<tr>
<td>D12_RSV</td>
<td>77</td>
<td>RSVD</td>
<td>Reserved.</td>
</tr>
<tr>
<td>D13_RSV</td>
<td>76</td>
<td>RSVD</td>
<td>Reserved.</td>
</tr>
<tr>
<td>D14_RSV</td>
<td>71</td>
<td>RSVD</td>
<td>Reserved.</td>
</tr>
<tr>
<td>D15_RSV</td>
<td>70</td>
<td>RSVD</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>
7. Design Recommendations

7.1. Typical Connections

Representative circuits for applications of the SiI8784 chip are shown in Figure 7.1 and Figure 7.2. For a detailed review of your intended circuit implementation, contact Lattice Semiconductor.

![Figure 7.1. Typical Connection Diagram (MHL Output)](image-url)
Figure 7.2. Typical Connection Diagram (HDMI Output)
7.2. Power Supplies Decoupling

Designers should include the decoupling and bypass capacitors at each power signal in the layout. These are shown schematically in Figure 7.3. Place these components as close as possible to the input processor differential signals, and avoid routing the differential signals through vias. Figure 7.4 is the representative of the various types of power connections on the input processor.

![Figure 7.3. Decoupling and Bypass Schematic](image)

![Figure 7.4. Decoupling and Bypass Capacitor Placement](image)

Connections in one group (such as CVCC10) can share C2, C3, and the ferrite, with each ball having a separate C1 placed as close to the ball as possible.
7.3. High-speed HDMI/MHL TMDS Signals

7.3.1. Source Termination
Source termination suppresses the signal reflection and overshoot, and at the same time allows strong input processor drive for longer cable support. The SiI8784 input processor has 100 Ω internal source terminations on the HDMI/MHL differential signal. The common mode clock signal does not have source termination.

7.3.2. ESD Protection
The SiI8784 input processor chip is designed to withstand electrostatic discharge during manufacturing. In applications where higher protection levels are required in the finished product, ESD limiting components can be placed on the differential lines coming out of the chip. These components typically have a capacitive effect, reducing the signal quality at higher clock frequencies on the link. Use the lowest capacitance devices, if possible. In no case should the capacitance value exceed 1 pF.

7.3.3. Layout Guidelines
The layout guidelines below help to ensure signal integrity. Lattice Semiconductor strongly encourages the board designer to follow the guidelines below.

- Place the input and output connectors that carry the TMDS signals as close as possible to the chip
- Route the differential lines as directly as possible from the connector to the device when using industry-standard HDMI connectors
- Route the two traces of each differential pair together
- Minimize the number of VIAs through which the signal lines are routed
- Layout the MHL input pin traces with a controlled differential impedance of 100 Ω and a common mode impedance of 30 Ω. The differential impedance of the HDMI output pins must be designed within ±15% of 100 Ω
- Serpentine traces are not recommended to compensate for inter-pair trace skew

7.4. EMI Considerations
Electromagnetic interference is a function of board layout, shielding, receiver component operating voltage, frequency of operation, and so on. When attempting to control emissions, do not place any passive components on the differential signal lines (except for the ESD protection and common mode choke described earlier). Lattice Semiconductor recommends the use of a metal shielding can over the SiI8784 chip and the traces going to the connector. The PCB ground plane should extend unbroken under as much of the input processor chip and associated circuitry as possible, with all ground signals of the chip using a common ground.
8.  Packaging

8.1.  ePad Requirements

The SiI8784 input processor chip is packaged in 88-pin QFN package with an exposed pad (ePad) that is used for the electrical ground of the device and for improved thermal transfer characteristics. The ePad dimensions are 5.60 mm × 5.60 mm ± 0.15 mm. Soldering the ePad to the ground plane of the PCB is required to meet package power dissipation requirements at full speed operation, and to correctly connect the chip circuitry to electrical ground. A clearance of at least 0.25 mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid the possibility of electrical shorts.

The thermal land area on the PCB may use thermal vias to improve heat removal from the package. These thermal vias also double as the ground connections of the chip and must attach internally in the PCB to the ground plane. An array of vias should be designed into the PCB beneath the package. For optimum thermal performance, the via diameter should be 12 mils to 13 mils (0.30 mm to 0.33 mm) and the via barrel should be plated with 1-ounce copper to plug the via. This design helps to avoid any solder wicking inside the via during the soldering process, which may result in voids in solder between the pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be tented with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 4 mils (0.1 mm) larger than the via diameter.

Package stand-off when mounting the device also needs to be considered. For a nominal stand-off of approximately 0.1 mm the stencil thickness of 5 mils to 8 mils should provide a good solder joint between the ePad and the thermal land.

Figure 8.1 on the next page shows the package dimensions of the SiI8784 device.
8.2. Package Dimensions

**JEDEC Package Code MO-2206**

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
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<td>0.85</td>
<td>0.90</td>
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<tr>
<td>A1</td>
<td>Stand-off</td>
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<td>0.02</td>
<td>0.05</td>
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<tr>
<td>A2</td>
<td>Body thickness</td>
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<td>0.65</td>
<td>0.70</td>
</tr>
<tr>
<td>A3</td>
<td>Base thickness</td>
<td>0.20 REF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>Footprint</td>
<td>9.90</td>
<td>10.00</td>
<td>10.10</td>
</tr>
<tr>
<td>E</td>
<td>Footprint</td>
<td>9.90</td>
<td>10.00</td>
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<tr>
<td>D1</td>
<td>Body size</td>
<td>9.75 BSC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>E1</td>
<td>Body size</td>
<td>9.75 BSC</td>
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</table>

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
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<tbody>
<tr>
<td>D2</td>
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<td>5.60</td>
<td>5.75</td>
</tr>
<tr>
<td>E2</td>
<td>ePad</td>
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<td>5.60</td>
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<tr>
<td>b</td>
<td>Lead width</td>
<td>0.15</td>
<td>0.20</td>
<td>0.25</td>
</tr>
<tr>
<td>e</td>
<td>Lead pitch</td>
<td>0.40 BSC</td>
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<td></td>
</tr>
<tr>
<td>L</td>
<td>Lead foot length</td>
<td>0.30</td>
<td>0.40</td>
<td>0.50</td>
</tr>
<tr>
<td>Ø</td>
<td>Mold angle</td>
<td>0°</td>
<td>—</td>
<td>14°</td>
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<tr>
<td>R</td>
<td>Lead radius, inside</td>
<td>0.075</td>
<td>—</td>
<td>—</td>
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<tr>
<td>K</td>
<td>ePad clearance</td>
<td>0.20</td>
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</table>

**Note:** Dimensions in mm.

Figure 8.1. 88-Pin QFN Package Diagram
9. Marking Specification

Figure 9.1 and Figure 9.2 show the markings of the SiI8784 package. These drawings are not to scale.

![Marking Diagram](image)

Figure 9.1. Marking Diagram

![Alternate Topside Marking](image)

Figure 9.2. Alternate Topside Marking

9.1. Ordering Information

<table>
<thead>
<tr>
<th>Production Part Numbers:</th>
<th>Device</th>
<th>Part Number</th>
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<tr>
<td>Analog Front End Video Processor with HDMI1.4/MHL2.1 Transmitter</td>
<td>SiI8784CNUC</td>
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</table>

The universal package can be used in lead-free and ordinary process lines.
References

Standards Documents

This is a list of the standards abbreviations appearing in this document.

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Standards publication, organization, and date</th>
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<tbody>
<tr>
<td>HDMI</td>
<td><em>High Definition Multimedia Interface</em>, Revision 1.4, HDMI Consortium.</td>
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<td>HCTS</td>
<td><em>HDMI Compliance Test Specification</em>, Revision 1.4, HDMI Consortium.</td>
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<tr>
<td>MHL</td>
<td><em>MHL (Mobile High-definition Link) Specification</em>, Revision 2.1, MHL, LLC.</td>
</tr>
<tr>
<td>HDCP</td>
<td><em>High-bandwidth Digital Content Protection</em>, Revision 1.4, Digital-Content Protection, LLC.</td>
</tr>
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<td>DVI</td>
<td><em>Digital Visual Interface</em>, Revision 1.0, Digital Display Working Group; April 1999.</td>
</tr>
<tr>
<td>CEA-861-D</td>
<td><em>A DTV Profile For Uncompressed High Speed Digital Interfaces</em>, EIA/CEA; July 2006.</td>
</tr>
<tr>
<td>EDDC</td>
<td><em>Enhanced Display Data Channel Standard</em>, Version 1, VESA; September 1999.</td>
</tr>
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</table>

For information on the specifications that apply to this document, contact the responsible standards groups appearing on this list.

<table>
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<tr>
<th>Standards Group</th>
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<td><a href="http://www.vesa.org">http://www.vesa.org</a></td>
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<td><a href="http://www.hdmi.org">http://www.hdmi.org</a></td>
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<td>MHL</td>
<td><a href="http://www.mhlconsortium.org">http://www.mhlconsortium.org</a></td>
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Lattice Semiconductor Documents

The following are available from your Lattice Semiconductor sales representative. *The Programmer’s Reference requires an NDA with Lattice Semiconductor.*

<table>
<thead>
<tr>
<th>Document</th>
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<tr>
<td>SiI-AN-0129</td>
<td>PCB Layout Guidelines: Designing with Exposed Pads</td>
</tr>
<tr>
<td>SiI-PR-0041</td>
<td>CEC Programming Interface (CPI) Programmer’s Reference</td>
</tr>
<tr>
<td>SiI-AN-1108</td>
<td>SiI8784 and SiI8788 Supported SPI Flash Memories</td>
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Revision History

Revision C, June 2017
Figure 9.2. Alternate Topside Marking added per PCN13A16.

Revision B, March 2016
Updated to latest template.

Revision B, September 2014
Summary of changes:
Removed the mentioning of Sil8784 and Sil8788 Analog Video Process Programmer Reference.
Details of changes:
Removed the reference to Programmer Reference from Section 3.5.2 Registers, 3.5.4 Interrupt, and Lattice Semiconductor Documents.

Revision A, September 2014
First production release.