ORSPI4 PCB Design Guidelines for SPI4.2 and QDR Memory Controller Interfaces

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Introduction

The ORSPI4 has several electrical interfaces for high-speed data transfer to other components. This note will discuss and highlight the system design considerations when implementing board designs using the ORSPI4. This document covers suggested PCB design guidelines while avoiding lengthy theoretical discussions. Many excellent text books have been published which can be referenced to understand the reasons supporting these design guidelines. This note will provide recommendations about the following board design issues:

- Routing PCB signals
- Generating and supplying reference voltages
- Terminating signals

General Power and Ground Recommendations

The electrical connections between the ORSPI4 and other devices must provide a solid pathway to the power system to guarantee a high degree of signal integrity. The primary function of the power plane is to provide a low-impedance path between the power source to the device. The power plane must have low resistance to ensure minimum voltage drop to the device. This can be aided by keeping via connections to a minimum. When vias cannot be avoided use large vias for power and ground connections. Power and ground vias should connect to all of the layers associated with a particular plane. To summarize:

- Keep via usage to minimum
- Use large power and ground vias
- Connect power and ground vias to all power and ground layers

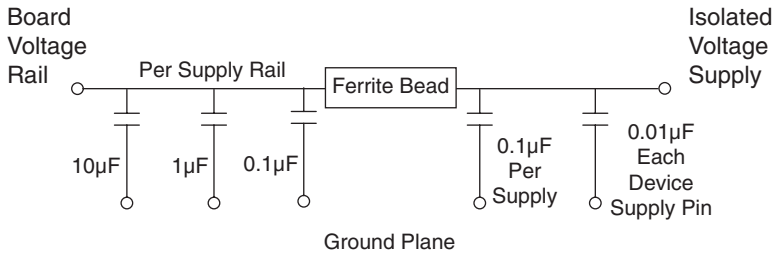
The power traces and vias should also be thoughtfully designed. The noise generated by the ORSPI4 can be minimized by having the power trace pass from the via to a decoupling capacitor pad and then to the device. Using this connection sequence, the resistance and inductance of the trace and via will help isolate the component noise. Keep the trace between ORSPI4 and the bypass capacitor as short as possible. A short, wide trace will produce a lower inductance and resistance.

Decoupling Recommendations

It is always a good design philosophy to provide RF bypassing of power and DC control lines to the ORSPI4. This is indeed the case when the ORSPI4 is located some distance away from the power supply. RF chokes and good-bypassing capacitors of approximately 1000 pf to 0.1 µF are recommended at the DC supply lines. If the ORSPI4 is powered from a regulated power supply, the regulator noise will increase depending upon the external load current drawn from the regulator. The noise performance of the ORSPI4 may degrade depending upon the type of regulator used, and also upon the load current drawn from the regulator. To improve the noise performance of the ORSPI4 under external load conditions, place a low ESR electrolytic capacitor of about 10µF on the voltage line. In addition to the 10 µF capacitor, the decoupling of the voltage line can be enhanced further by including a choke about 4 - 10 µH in series with the voltage source.

The ORSPI4 interfaces have several independent device supplies that have common voltage values. These supplies can share the common voltage rail if the board design can guarantee that the supplies are isolated. This can be accomplished with simple LC filtering schemes to prohibit device supplies from being influenced by power supply fluctuations. An inductor with good current carrying characteristics and low resistance should be placed in series with the device to choke off the high frequency noise that may be caused by other shared supplies. Figure 1 illustrates the suggested isolation and decoupling scheme.

Figure 1. Suggested Isolation and Decoupling Scheme



Decoupling or bypass capacitors play a large role in device performance. The main role of bypass capacitors is to act as a local DC power supply to meet the demands of fluctuating power rails and block unwanted noise going into or coming from the power plane, as well as the ORSPII generated switching noise and capacitive and inductive coupling from adjacent board level planes and traces. Decoupling must consider many frequency bands. Below is a simple stated list of guidelines for proper decoupling when using the ORSPI4:

- One .001 (or .0001) µF for ORSPI4 core in order to widen the spectral distribution.
- Bypass capacitor usage must take into account both a low ESR as well as the self-resonant frequency.
- One 0.01µF capacitor per device power pin is a good rule of thumb.
- Locate de-coupling capacitors as close as possible to the device power pins and run short, wide traces to vias when they are required.
- Distribute some bulk capacitance throughout the layout to help eliminate low frequency coupling and maintain a low impedance power system.
- Maintain isolation between device supplies using isolation scheme in Figure 1.
- Utilize different types of capacitors across the PCB. This will provide decoupling coverage across a larger frequency spectrum.
- EMI discrete filter components provide quality isolation from digital supplies.

PCB Considerations for the SPI4.2 Interface

The SPI-4 specification requires signal amplitudes of 100mV minimum at the receiver, and the differential driver needs to provide between 250mV and 400mV signal swing. The SPI4.2 interface is a source synchronous bus that is comprised of a unidirectional differential bus that is physically routed point-to-point. The ORSPI4 requires closely matched differential P & N trace skew. For the static alignment option, the skew between data and clock is also very important. ORSPI4 alignment features allow margins with channel-to-channel skew when used in the dynamic alignment mode. The following list provides recommendations for printed circuit board layout using the SPI4.2 interface:

- Recommended maximum length for the SPI4 phase 2 bus is 12 inches.
- All differential pair bus routing should be done in controlled impedance strip-line or micro-strip layers maintaining a controlled impedance of 100 ohms +/- 10% per pair.
- Keep P and N traces closely matched.
- Use minimum spacing on P and N pins to provide closely coupled differential signal pairs.
- A solid ground reference plane must be maintained under all SPI4 bus signals. Cuts or slots in planes degrade performance.
- Do not jump from layer to layer through vias. Route high speed signals in one layer as much as possible.
- Keep at least 2x minimum spacing between high-speed clock signals and all other board signal lines.
- Use 0.01µF SMT capacitors for the center tap termination pins LVCTAP.
- Bypass capacitors should be no greater than .2” from the device power pin if possible, and should be attached in series between any via and device, if a via is used.

The LVDS I/Os are powered from 3.3V supplied from the VDD33_SPI4 pins. These power pins should be properly isolated and decoupled from the 3.3V board supply. The analog circuitry of the SPI4 core is supplied from 1.5V via the VDDA_SPI[A:D] pins.

PCB Considerations for the QDR Memory Interface

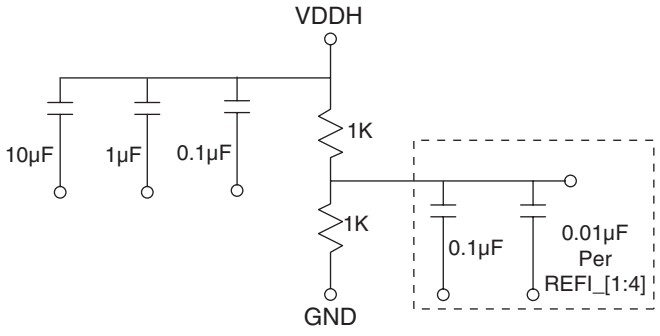
The ORSPI4 QDR memory interface incorporates the separate data inputs, outputs, control, and clock pins needed to connect to the latest industry standard memory devices. This interface utilizes the simultaneous operation of separate data write and read buses that introduces many system level considerations. Because the control and address signals are synchronized with the clock, it is important to match the lengths of these traces. A critical design goal of the interface is to maintain a consistent path delay time and impedance across the interface traces. Proper routing of all of the signals is absolutely essential. The following layout guidelines help ensure that designs operate at the highest possible frequencies:

- Maximum trace length between SRAM device and ORSPI4 should no more than 3 inches for 175 MHz operation or no more than 2 inches for 200 MHz operation.
- Keep the trace lengths as closely matched as possible.
- Route signals only on layers that are directly adjacent to a common reference plane.
- When using multiple routing planes, the planes should be equidistant from the power and ground planes to maintain impedance matching.
- If vias are used, keep the same number of vias on all traces of the bus.
- No signal traces adjacent to high-speed traces should be run parallel for longer than 1", and traces should be routed with 30- or 45 degree bends if possible. 90 degree bends are not permitted when routing high-speed signals on a printed circuit board.
- Keep 30 ml separation between clocks K, K# and CQ, CQ# and other signals.
- K, K#, and CQ, CQ# should be routed as single-ended traces (not differential).

The HSTL I/O interface standard used with QDR SRAM memories relies on a reference voltage (VREF). The ORSPI4 HSTL input buffers uses a reference voltage supplied to the REFI_[1:4] pins. It is recommended that the input receiver reference voltage should be isolated from other nets, decoupled from all power supply rails and VSS with proper decoupling capacitors and routed away from other signals.

Simply, a resistor divider network can be used to generate this low power reference (see Figure 2). VREF can be generated most accurately from a single distributed circuit. However, some attention should be paid to the routing of VREF, since the HSTL specification requires dynamic noise to be maintained to less than 2% of the VREF DC level. The voltage offset of 50% of VDDH can easily be achieved with 2% accuracy using inexpensive discrete resistor networks. This topology provides excellent tracking to the 50% point over changes in voltage and temperature.

Figure 2. Suggested VREF Generation Scheme

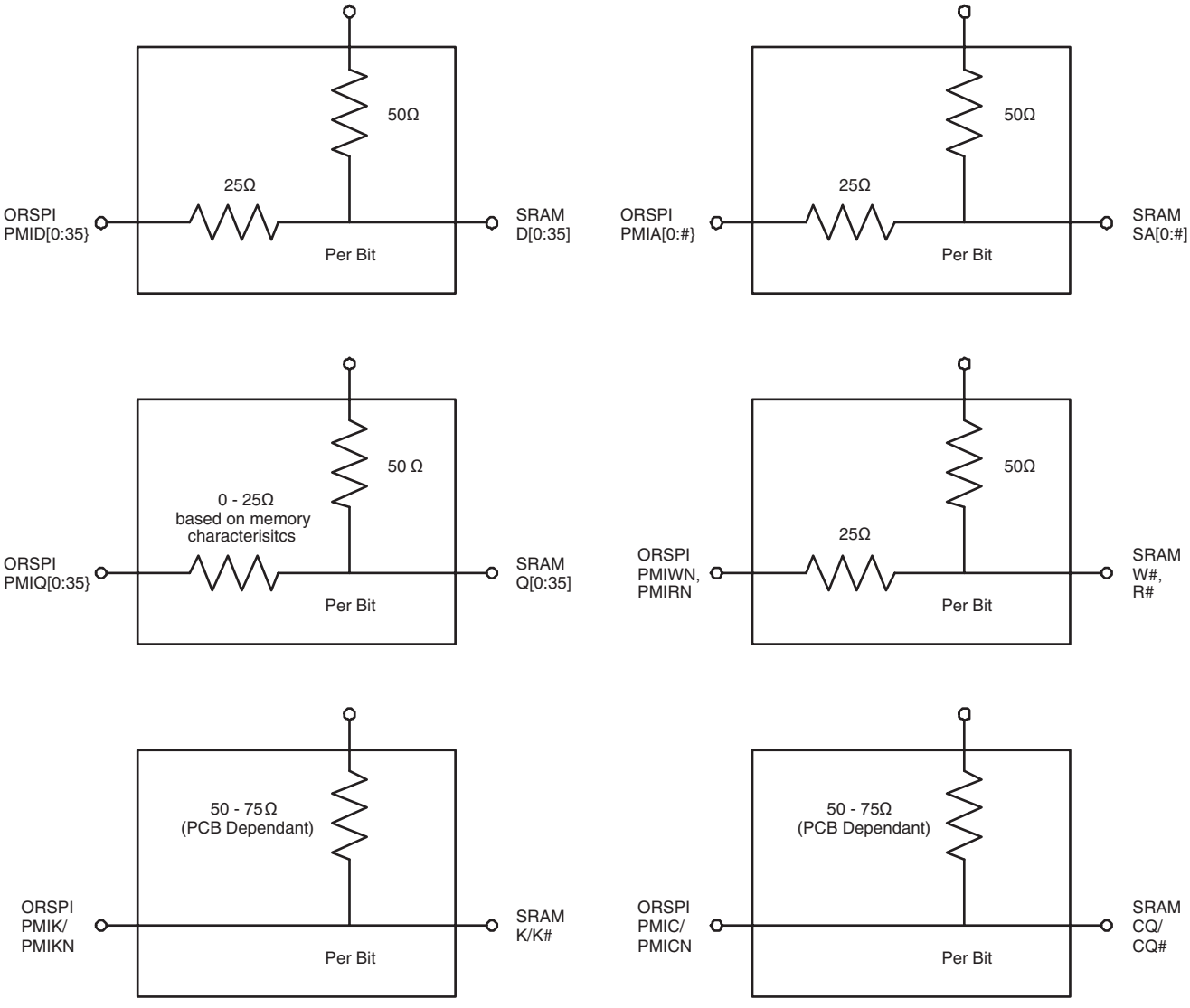


- VREF must be isolated from other nets. Typically at least 20 mm apart from other signals
- VREF must track the midpoint of the signal voltage swing (generally VDDH/2) within 2% over all valid voltage, temperature, and noise conditions.
- Use a distributed decoupling scheme to minimize the transient currents and returns.
- VREF must be decoupled from both VDDH and VSS with balanced decoupling capacitors.
- Shield VREF using VSS and VDDH.

The QDR memory interface terminates the signals involved. The type of termination depends on the design and memory device. The HSTL I/O of the ORSPI4 supports several approved methods. The HSTL terminations require resistors or resistor packs on the PCB trace. Discrete resistors or resistor packs are typically used for this termination. Resistor packs are specifically designed to meet this requirement and are widely available.

For most applications, a single-series/single-parallel termination scheme serves well (see Figure 3).This approach minimizes cost and permits simpler signal routing, while reducing reflections sufficiently and improving signal bandwidth and settling. The HSTL specifications recommend a 25-ohm series resistor and a 50-ohm parallel termination. While other termination schemes may provide superior noise margin, this configuration reduces noise on the ORSPI4 device. The series resistors, placed as close as possible to the ORSPI4 driver, will reduce the amount of noise by limiting any line mismatches. The value of the series resistor should be from 0-ohm to 25-ohms depending on the characteristics of the memory chosen. Placement of the parallel terminations connected directly to a VTT plane will guarantee good signal terminations for use with the QDR memory device when the resistor is placed as close as possible to the receiver.

Figure 3. ORSPI4 QDR Memory Address and Data Termination Scheme



To facilitate a quad data rate, all data is carried by separate read and write ports. By using a DDR clock with two ports, information can be transferred at four data items per clock (assuming four operations are needed, two read

and two write). The K and K# signals created by the ORSPI4 are HSTL inverted signals. These signals must be routed as independent traces that are decoupled from one another, as they are not to be treated as coupled differential traces. Both K, K# and CQ, CQ# should be routed a minimum of 30mls away form other interface signals. The PMIRN and PMIWN signals are also HSTL signals and should be treated as such.

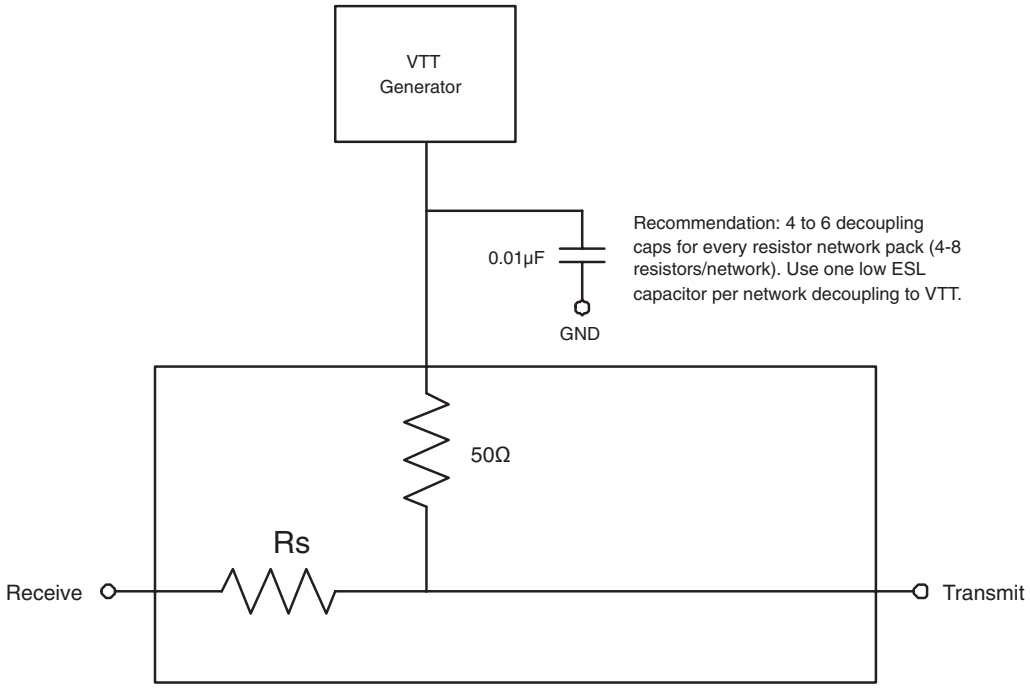
The parallel termination voltage (VTT) must also track half the supply voltage (VDDH). Unlike VREF, that will not have much current drawn from it, several amps of current could be drawn from the VTT rail. VTT circuitry should be placed very close to the termination resistors. Since the termination resistors are placed on the top layer, a suggested VTT plane should also be localized to the top plane (see Figure 4).

The current sink and source requirements for a proper VTT requires some special consideration. Few component options are available to provide the required voltages for VTT for QDR devices. Several manufacturers are introducing step-down dc/dc converters that provide a tracking-termination voltage for HSTL applications. These devices can provide the adequate VTT voltage with high current output. Linear Technology (www.linear.com) offers the LTC3718 DC/DC controller that operates with a very low Vin of 1.5V - 1.8V. National Semiconductor offers the LP2995 linear regulator that provides a good source for active termination. Output for both devices tracks to 50% of the Vin which meets both power and voltage tolerances for VTT.

QDR memory devices have recently been introduced using 1.5V and 1.8V specifications. Both of these operating conditions are supported with the ORSPI4 memory interface. The ORSPI4 is 1.8V tolerant by accepting 1.8V HSTL input levels with VDDH= 1.5V.

- VTT is typically 50% of the VDDH supply.
- Use a VTT generator with symmetrical sink and source current capabilities.
- Place the VTT generator as close as possible to the termination resistors.
- Use VTT ”islands” rather than routing traces. Distribute decoupling across entire “island”.
- Use one 0.1μF capacitor for every two parallel terminations.

Figure 4. Recommended Parallel Termination (VTT) for QDR Memory Interface



A separate supply VDDA_PLL is used to supply the analog supply of the QDR PLL. This 3.3V supply should be isolated from board noise and properly decoupled. The EXT_1K pin on the ORSPI4 device must be connected to a 1Kohm, 1/16 W, 1% precision resistor.

Summary

PCB factors such as noise generation, signal reflection, crosstalk, and ground bounce can interfere with a signal, especially with the high speed interfaces supported by the ORSPI4 devices. The signal routing, termination schemes, and power distribution techniques discussed in this application note can help designers insure first-time system success when designing in the ORSPI4 device. The ORSPI4 also includes a quad channel 3.7G SERDES. System level design guidelines are documented in Lattice Semiconductor application note (TN-1033) High-Speed PCB Design Considerations. This document will also provide more in-depth information concerning high-speed board design.

References

1. High-Speed Digital Design: A Handbook of Black Magic by Dr. Howard Johnson and Martin Graham
2. Digital Design for Interference Specifications (2nd Edition) by David Terrell and R. Kenneth Keenan
3. High Speed PCB Design by Lee W. Ritchey and James C. Blankenhorn
4. ORCA® ORSPI4 Data Sheet

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