CrossLink Hardware Checklist

Preliminary **Technical Note**

FPGA-TN-02013 Version 1.0

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Contents

Tables

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
DDR	Double Data Rate
I^2C	Inter-Integrated Circuit
LVDS	Low-Voltage Differential Signaling
NVCM	Non-Volatile Configuration Memory
PCB	Printed Circuit Board
PLL	Phase Locked Loop
SPI	Serial Peripheral Interface
WLCSP	Wafer Level Chip Scale Package

1. Introduction

When designing complex hardware using the Lattice Semiconductor CrossLink™ FPGA, designers must pay special attention to critical hardware configuration requirements. This technical note steps through these critical hardware implementation requirements related to the CrossLink device. The document does not provide detailed step-by-step instructions but gives a high-level summary checklist to assist in the design process.

This technical note assumes that the reader is familiar with the CrossLink device features as described in FPGA-DS-02007, CrossLink Family Data Sheet.

The critical hardware areas covered in this technical note include:

- Power supplies as they relate to the CrossLink power supply rails and how to connect them to the PCB and the associated system
- Configuration mode selection for proper power-up behavior
- Device I/O interface and critical signals

The data sheet includes the functional specification and electrical characteristics for the device.

Topics covered in the data sheet include but are not limited to the following:

- High-level functional overview
- Pinouts and packaging information
- Signal descriptions
- Device-specific information about peripherals and registers
- Electrical specifications

Important: Refer to the following documents for detailed recommendations.

- FPGA-TN-02012, CrossLink High-Speed I/O Interface
- FPGA-TN-02014, CrossLink Programming and Configuration Usage Guide
- FPGA-TN-02015, CrossLink sysCLOCK PLL/DLL Design and Usage Guide
- FPGA-TN-02016, CrossLink sysI/O Usage Guide
- FPGA-TN-02017, CrossLink Memory Usage Guide
- FPGA-TN-02018, Power Management and Calculation for CrossLink Devices
- FPGA-TN-02019, CrossLink I2C Hardened IP Usage Guide
- FPGA-TN-02020, Advanced CrossLink I2C Hardened IP Reference Guide
- TN1068, Power Decoupling and Bypass Filtering for Programmable Devices

2. Power Supplies

The CrossLink internal Power Good condition is determined by the V_{CC}, $V_{CCAUX25VPP}$ and V_{CCIO0} power supplies. These supplies need to be at a valid and stable level before the device becomes operational. Several other supplies including V_{CC_DPHY}, V_{CCA_DPHY}, V_{CCPLL_DPHY}, V_{CCMU_DPHY} are used in conjunction with on-board D-PHYs on CrossLink devices. Table 2.1 describes the power supplies and the appropriate voltage levels for each supply.

Table 2.1. CrossLink FPGA Power Supplies

Supply	Voltage (Nominal Value)	Description
V_{CC}	1.2 V	FPGA core power supply. Required for Power Good condition.
V_{CCGPLL}	1.2 V	General Purpose PLL Supply Voltage. Should be isolated from excessive noise.
$V_{CCAUX25VPP}$	2.5 V	Auxiliary Supply Voltage for Bank 1, 2 and NVCM Programming. Required for Power Good condition.
$V_{CCIO[2, 1, 0]}$	1.2 V to 3.3 V	I/O Driver Supply Voltage for Bank 0, 1, or 2. Each bank has its own V_{CCIO} supply: V_{CCIO0} is used in conjunction with pins dedicated and shared with device configuration, and is required for Power Good condition.
$V_{CC\_DPHY[1,0]}$	1.2 V	Digital Supply Voltage for D-PHY. Should be isolated from excessive noise.
$V_{CCA\_DPHY[1,0]}$	1.2 V	Analog Supply Voltage for D-PHY. Should be isolated from excessive noise.
$V_{CCPLL\_DPHY[1,0]}$	1.2 V	PLL Supply voltage for D-PHY. Should be isolated from excessive noise.
V_{CCMU_DPHY1}	1.2 V	WLCSP36 package only: V_{CC_DPHY1}, V_{CCA_DPHY1} and V_{CCPLL_DPHY1} ganged together. Should be isolated from excessive noise.

The CrossLink FPGA device has a power-on-reset state machine that depends on several of the power supplies.

These supplies should come up monotonically. A power-on-reset counter begins to count after V_{CC}, $V_{CCAUX25VPP}$ and V_{CCIO0} reach the levels defined in the Power-On-Reset Voltage Levels section of FPGA-DS-02007, CrossLink Family Data Sheet. Initialization of the device does not proceed until the last power supply has reached its minimum operating voltage.

3. CrossLink MIPI D-PHY and PLL Power Supplies

Supplies dedicated to the operation of the CrossLink MIPI® D-PHY include V_{CCA_DPHYx}, V_{CCPLL_DPHYx}, and V_{CCMU_DPHY1}. These pins are also paired with dedicated ground pins including GNDA_DPHYx and GNDPLL_DPHYx. These supplies should be decoupled with adequate bypass capacitors between these pins, close to the device package.

The V_{CCGPLL} provides a quiet supply for the general purpose PLL while the V_{CCPLL_DPHYx} and V_{CCA_DPHYx} provide a quiet supply for the critical MIPI D-PHY blocks. For the best jitter performance, careful pin assignment will keep noisy I/O pins away from sensitive functional pins. The leading causes of PCB related MIPI D-PHY crosstalk is related to FPGA outputs located in close proximity to the sensitive MIPI D-PHY power supplies. These supplies require cautious board layout to ensure noise immunity to the switching noise generated by FPGA outputs. Guidelines are provided to build quiet filtered supplies for the analog supplies, however robust PCB layout is required to ensure that noise does not infiltrate into these analog supplies. See the list of recommended documents in the Introduction section for more details.

4. Power Estimation

After deciding the CrossLink, package and logic implementation, power estimation for the system environment should be determined based on the software Power Calculator provided as part of the Lattice Diamond® design tool. When estimating power, the designer should keep two goals in mind:

- Power supply budgeting should be based on the maximum of the power-up in-rush current, configuration current or maximum DC and AC current for the given system's environmental conditions.
- The ability for the system environment and CrossLink device packaging to be able to support the specified maximum operating junction temperature. By determining these two criteria, the CrossLink device power requirements are considered early in the design phase.

5. Configuration Considerations

The CrossLink device includes provisions to configure the FPGA from a processor via Slave I^2C or Slave SPI, Master SPI from an external SPI Flash, or internally from NVCM.

The use of external resistors is always needed if the configuration signals are being used to handshake to other devices. For Master SPI mode, the MCK pin must be connected to a serial 30 Ω resistor placed close to the CrossLink device package, to prevent reflections or glitches during Master SPI configuration. Recommended 4.7K pull-up resistors to V_{CCIO0} and pull-down to board ground should be used on the following pins.

Table 5.1. Required Pull-up/Pull-down Resistors for Configuration Pins

Pin	PCB Connection
CRESET_B	4.7K Pull-up to V_{CCIO0}
CDONE	4.7K Pull-up to V_{CCIO0}
SDA	Strong Pull-up (Open Drain Signal)*
SCL	Strong Pull-up (Open Drain Signal)*
SPI_SS	4.7K Pull-up to V_{CCIO0} (Open Drain Signal)
MCK	30 Ω Serial Resistor close to CrossLink package

***Note**: Pull-up value on I^2C signals is dependent on the I^2C bus characteristics and programming speed. Typical values are between 2.2K and 4.7K.

Table 5.2. Configuration Pins Needed per Programming Mode

Configuration Mode	Clock		Shared Pins	Dedicated Pins
	Pin	I/O		
SSPI	SPI_SCK	Input	MISO, MOSI, SPI_SS	CRESET_B
MSPI	MCK	Output	MISO, MOSI, CSN	CRESET_B
I2C	SCL	Input	SDA	CRESET_B

6. Power Management Unit

The CrossLink device includes a dedicated Power Management Unit which may place the fabric and other on-chip resources into sleep mode. CrossLink includes a dual function pin called PMU_WKUPN. This pin is active low and may be used to wake-up the device from sleep mode. A weak pull-up resistor (10K – 100K) is recommended when the pin is assigned to the wakeup function.

7. Clock Inputs

The CrossLink device provides primary clock input pins, which are shared function pins that can also be used as general purpose I/O. When these pins are used for clocking purpose, the user needs to pay attention to minimize signal noise on these pins.

8. Pinout Considerations

The CrossLink device is designed to support high-speed video interface bridging. This includes various rule-based pinouts that need to be understood prior to implementation of the PCB design. The pinout selection must be completed with an understanding of the interface building blocks of the FPGA fabric. These include I/O Logic blocks such as DDR, clock resource connectivity and PLL usage. Refer to FPGA-TN-02012, CrossLink High-Speed I/O Interface for rules pertaining to these interface types.

8.1. LVDS Pinout Considerations

True LVDS inputs and outputs are available on I/O pins in Banks 1 and 2. These multi-function I/O pins support LVDS, LVCMOS, subLVDS, SLVS, and MIPI D-PHY receive functions. The I/O buffers are described in FPGA-TN-02016, CrossLink sysI/O Usage Guide.

8.2. MIPI D-PHY Interface Considerations

Although coupling has been reduced in the device packages of CrossLink devices so that little crosstalk is generated, the PCB board can cause significant noise injection from any I/O pin adjacent to MIPI D-PHY data, reference clock, and power pins as well as other critical I/O pins such as clock signals. PCB traces running in parallel for long distances need careful analysis. Simulate any suspicious traces using a PCB crosstalk simulation tool to determine if they can cause problems.

High-speed signaling requires careful PCB stackup and layout design. Maintaining good transmission line characteristics and impedance controlled routing is a must requirement to achieve higher bandwidth. A solid ground reference plane shall be maintained underneath of high-speed signal routing. This includes tightly matched differential routing with very few discontinuities. Matching between the D-PHY clock and data pairs is especially critical. Refer to TN1033, High-Speed PCB Design Considerations, for suggested methods and guidance.

9. Checklist Table

Table 9.1. Checklist Table

	Item	OK	NA
1	**FPGA Power Supplies**		
1.1	V_{CC} core voltage @ 1.2 V ±5%		
1.1.1	Use a PCB plane for V_{CC} core voltage with proper decoupling.		
1.1.2	V_{CC} core supply sized to meet power requirement calculation from software.		
1.2	V_{CCGPLL} @ 1.2 V ±5%		
1.2.1	V_{CCGPLL} isolated from excessive noise.		
1.2.2	V_{CCGPLL} pins should be ganged together and a solid PCB plane is recommended. This plane should not have adjacent non-MIPI D-PHY signals passing above or below. It should also be isolated from the V_{CC} core power plane.		
1.3	All V_{CCIO} voltages are between 1.2 V to 3.3 V		
1.3.1	V_{CCIO0} voltage matches external configuration interfaces (that is memory devices).		
1.3.2	V_{CCIO0}, V_{CCIO1}, V_{CCIO2} voltage based on user design.		
1.4	$V_{CCAUX25VPP}$ @ 2.5 V ±5%		
2	**MIPI D-PHY Power Supplies**		
2.1	V_{CCA_DPHYx} @ 1.2 V ±5%. Should be ganged together and a solid PCB plane is recommended. This plane should not have adjacent non-MIPI D-PHY signals passing above or below. It should also be isolated from the V_{CC} core power plane.		
2.2	V_{CCPLL_DPHYx} @1.2 V ±5% “clean” and “isolated”		
2.3	V_{CCMU_DPHYx} @1.2 V ±5% – follow recommendations for V_{CCA_DPHY}.		
3	**Configuration/Power Management Unit**		
3.1	Pull-ups and pull-downs on configuration specific pins as given in Table 5.1.		
3.2	V_{CCIO0} bank voltage matches sysCONFIG peripheral devices such as SPI Flash.		
3.3	PMU_WKUPN pull-up (when used to wake up the device).		
4	**MIPI D-PHY**		
4.1	Dedicated reference clock input from clock source meets the DC and AC requirements.		
4.1.1	External AC-coupling caps may be required for compatibility to common-mode levels.		
4.1.2	Reference clock termination resistors may be needed for compatible signaling levels.		
4.2	Maintain good high-speed transmission line routing.		
4.2.1	Continuous ground reference plane to serial channels.		
4.2.2	Length matched differential traces.		
4.2.3	Do not pass other signals on the PCB above or below the high-speed MIPI D-PHY signals traces without isolation.		
4.2.4	Keep non-MIPI D-PHY signal traces from passing above or below the 1.2 V V_{CCA_DPHY} power plane without isolation.		
5	**Critical Pinout Selection**		
5.1	Pinout has been chosen to address FPGA resource connections to I/O logic and clock resources per FPGA-TN-02012, CrossLink High-Speed I/O Interface.		
5.2	FPGA PLL, MIPI D-PHY PLL, and clock inputs assigned to proper pins per device FPGA-DS-02007, CrossLink Family Data Sheet.		
6	**I^2C**		
6.1	2.2K – 4.7K Pull-up on open drain signals SCL and SDA.		

References

For more information, refer to the following documents:

- FPGA-DS-02007, CrossLink Family Data Sheet
- FPGA-TN-02012, CrossLink High-Speed I/O Interface
- FPGA-TN-02014, CrossLink Programming and Configuration Usage Guide
- FPGA-TN-02015, CrossLink sysCLOCK PLL/DLL Design and Usage Guide
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- FPGA-TN-02020, Advanced CrossLink I2C Hardened IP Reference Guide
- TN1033, High-Speed PCB Design Considerations
- TN1068, Power Decoupling and Bypass Filtering for Programmable Devices

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

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July 2016	1.0	Updated document numbers.
May 2016	1.0	First preliminary release.

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