Thermal Management

October 2014

Introduction

Thermal management is recommended as part of any sound CPLD and FPGA design methodology. To properly assess the thermal characteristics of the system, Lattice Semiconductor specifies a maximum allowable junction temperature in all device data sheets. The system designer should always complete a thermal analysis of their specific design to ensure that the device and package does not exceed the junction temperature requirements.

The data shown in this Thermal Management document is relative and actual values depend on a variety of factors such as: die size, paddle size, airflow, power applied, printed circuit board design, proximity of other devices and user applications. Table 1 specifies the generic package thermal resistance for legacy GAL, CPLD, FPGA and XPLD devices. Table 2 specifies the device/package specific thermal resistance for newer FPGA products. These values are based upon JEDEC standards. If specified, the device/package specific thermal value supercedes the generic package thermal data contained in Table 1.

In addition to the device and package, the thermal characteristics of a circuit depend on the operating temperature, device power consumption, and the ability of the system to dissipate heat. The maximum junction temperature of a device can be calculated as shown:

$T_J = T_A + Power*\theta_{JA}$

or

$T_J = T_A + Power *(\theta_{JC}+R_{CS}+R_{SA})$

Where:

T_J	=	Junction Temperature of the Device
T_A	=	Ambient Temperature
R_{CS}	=	Thermal resistance of thermal interface material
R_{SA}	=	Thermal resistance of heat sink
θ_{JA}	=	Junction-to-Ambient Thermal Resistance (see Table 1 and Table 2 at the end of this section)
θ_{JC}	=	Junction-to-Case Thermal Resistance (see Table 1 and Table 2 at the end of this section)
Power	=	$I_{CC} * V_{CC}$

I_{CC} may be estimated as shown in the “Power Consumption” section of the DC and Switching Characteristics section of each individual data sheet. The parameters in the I_{CC} equation may be found in the report file from the Lattice Diamond® compiler. For predicting power, the best resource is to use Lattice Diamond design tools. For additional information on power calculations and considerations please refer to the referenced technical note in the For Further Information section of each individual data sheet.

If the calculated T_J max exceeds the specified limits, refer to the following hints to reduce the overall power dissipation and package temperature.

Ways to Reduce Junction Temperature

1. Increase airflow in the system to reduce the case or ambient temperature.

2. Reduce power in one of the following ways:

   a. Reduce overall device utilization by combining common input functions. This is especially true when using wide input CPLD blocks. Even with the narrow FPGA logic blocks, careful partitioning of logic can reduce the overall net utilization.
   b. Trade off net utilization with reducing the number of high frequency switching nets. By careful use of different encoding schemes, the high frequency switching nodes can be reduced. For example, using one-hot encoding can reduce the high frequency switching nodes compared to a binary encoding while increasing the logic utilization.
   c. Reduce the frequency of operation. High-density architectures provide flexibility to control clock polarity to potentially reduce the overall clock speed.

3. Where possible, make use of the output slew rate control to reduce the output switching current of the device.

4. Make sure that programmable pull-ups are enabled to drive unused inputs to a proper logic level.

5. Select an appropriate heat sink and thermal interface material for the package.

Table 1. Package Thermal Resistance[1]

Package	Dimension	Pin Count	θ_{JA} (0lfm) °C/W	θ_{JA} (200lfm) °C/W	θ_{JC} °C/W
PDIP	.300 wide	20	67	49	30
	.300 wide	24	64	35	25
	.300 wide	28	56	33	23
PLCC	–	20	64	58	22
	–	28	56	49	18
	–	44	35	31	16
	–	68	34	30	13
	–	84	33	29	12
QFN	4 x 4 mm	24	42	32	16 (Theta JB) [2]
	5 x 5 mm	32	40	30	15 (Theta JB) [2]
	7 x 7 mm	48	39	29	15 (Theta JB) [2]
	9 x 9 mm	64	38	27	14 (Theta JB) [2]
SSOP	–	28	105	80	25
PQFP/MQFP	14 x 20 mm	100	35	34	12
	28 x 28 mm	120	32	26	12
	28 x 28 mm	128	32	26	11
	28 x 28 mm	160	30	24	9
	28 x 28 mm	208	25	23	8
	32 x 32 mm	240	24	18	5

Table 1. Package Thermal Resistance[1]

Package	Dimension	Pin Count	θ_{JA} (0lfm) °C/W	θ_{JA} (200lfm) °C/W	θ_{JC} °C/W
TQFP (1.4 mm thick)	10 x 10 mm	44	42	36	17
	7 x 7 mm	48	48	44	19
	14 x 14 mm	100	35	29	10
	14 x 14 mm	128	35	29	10
	20 x 20 mm	144	33	27	9
	24 x 24 mm	176	33	27	8
TQFP (1.0 mm thick)	7 x 7 mm	48	49	45	19
	10 x 10 mm	44	43	37	17
ucBGA	4 x 4 mm	64	77	70	20
	6 x 6 mm	132	61	53	16
csBGA	5 x 5 mm	64	90	85	15
	6 x 6 mm	56	74	68	15
	7 x 7 mm	144	72	66	13
	8 x 8 mm	100	70	65	13
	8 x 8 mm	132	49	40	13
caBGA	7 x 7 mm	49	74	68	15
	10 x 10 mm	100	48	39	12
	14 x 14 mm	256	40	35	10
fpBGA	11 x 11 mm	100	40	32	11
	13 x 13 mm	144	29	25	11
	17 x 17 mm	208	24	20	10
	17 x 17 mm	256	20	16	10
	23 x 23 mm	388	18	15	6
	23 x 23 mm	484	18	15	6
	27 x 27 mm	416	17	14	5
	27 x 27 mm	672	16	13	5
	31 x 31 mm	516	14	12	4
	31 x 31 mm	676	14	12	4
	31 x 31 mm	900	14	12	4
	35 x 35 mm	680	14	12	3
	35 x 35 mm	1156	13	11	3
PBGA	27 x 27 mm	272	20	17	6
	35 x 35 mm	388	16	13	3
	35 x 35 mm	492	16	13	3
fpSBGA	40 x 40 mm	680	11	10	0.65
	45 x 45 mm	1036	10	9	0.65
SBGA	27 x 27 mm	256	15	12	0.65
	31 x 31 mm	320[3]	13	10	0.65
	35 x 35 mm	352	12	9	0.65
	40 x 40 mm	432[3]	11	8	0.65
	45 x 45 mm	600	10	7	0.65

Table 1. Package Thermal Resistance[1]

Package	Dimension	Pin Count	θ_{JA} (0lfm) °C/W	θ_{JA} (200lfm) °C/W	θ_{JC} °C/W
ftBGA	17 x 17 mm	256	37	33	6
	19 x 19 mm	324	37	31	6
CERDIP	–	20	62	52	10
	–	24	60	48	10
LCC	–	20	65	60	8
	–	28	62	49	7
JLCC	–	44	69	38	4
	–	68	52	30	3
CPGA	–	84	38	21	3
	–	133	26	21	2

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1. The data shown in this Thermal Management document is relative and actual values depend on a variety of factors such as: die size, paddle size, airflow, power applied, printed circuit board design, proximity of other devices and user applications. This table specifies the generic package thermal resistance for legacy GAL, CPLD, FPGA and XPLD devices. These values are based upon JEDEC standards. If specified in Table 2, the device/package specific thermal value supercedes the generic package thermal data contained in this table.
2. θJB (θJB = Junction-to-Board Thermal Resistance). θJB value shown is only applicable when the package thermal pad is soldered directly onto user PCB.
3. The 320-ball BGA and 432-ball BGA packages junction temperature must not exceed 140 °C.

Table 2. Device/Package Thermal Resistance[1]

Family	Device	Package	Dimensions	Pin Count	θ_{JA} (0lfm) °C/W	θ_{JA} (200lfm) °C/W	θ_{JA} (500lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LatticeECP™ /LatticeEC™	LFEC1	TQFP	14 x 14 mm	100	36.9	33.0	30.4	23.6	12.4
	LFEC1	TQFP	20 x 20 mm	144	28.8	26.1	24.0	19.1	9.4
	LFEC1	PQFP	28 x 28 mm	208	40.2	37.0	34.2	30.5	18.5
	LFEC3	TQFP	14 x 14 mm	100	36.9	33.0	30.4	23.6	12.4
	LFEC3	TQFP	20 x 20 mm	144	28.8	26.1	24.0	19.1	9.4
	LFEC3	PQFP	28 x 28 mm	208	30.2	27.8	25.7	22.9	13.9
	LFEC3	FPBGA	17 x 17 mm	256	28.4	24.3	21.8	16.4	5.2
	LFECP/EC6	TQFP	20 x 20 mm	144	27.8	25.0	23.1	17.8	7.2
	LFECP/EC6	PQFP	28 x 28 mm	208	30.2	27.8	25.7	22.9	13.9
	LFECP/EC6	FPBGA	17 x 17 mm	256	25.9	22.0	19.5	14.2	4.0
	LFECP/EC6	FPBGA	23 x 23 mm	484	19.6	16.9	15.3	11.3	6.5
	LFECP/EC10	PQFP	28 x 28 mm	208	30.2	27.8	25.7	22.9	13.9
	LFECP/EC10	FPBGA	17 x 17 mm	256	24.0	20.1	17.7	12.4	3.1
	LFECP/EC10	FPBGA	23 x 23 mm	484	18.0	15.4	13.7	9.3	5.0
	LFECP/EC15	FPBGA	17 x 17 mm	256	22.7	18.9	16.5	11.3	2.6
	LFECP/EC15	FPBGA	23 x 23 mm	484	17.1	14.6	12.8	8.4	4.2
	LFECP/EC20	FPBGA	23 x 23 mm	484	16.6	14.0	12.2	7.8	3.8
	LFECP/EC20	FPBGA	27 x 27 mm	672	15.2	12.8	11.0	7.0	3.2
	LFECP/EC33	FPBGA	23 x 23 mm	484	15.8	13.1	11.3	7.1	3.1
	LFECP/EC33	FPBGA	27 x 27 mm	672	14.0	11.8	10.1	6.9	2.6

Table 2. Device/Package Thermal Resistance[1]

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LatticeECP2™	LFE2-6E	TQFP	20 x 20 mm	144	28.8	26.1	24.0	19.1	9.4
	LFE2-6E	FPBGA	17 x 17 mm	256	29.1	25.0	22.5	17.1	5.7
	LFE2-12E	TQFP	20 x 20 mm	144	28.8	26.1	24.0	19.1	9.4
	LFE2-12E	PQFP	28 x 28 mm	208	30.2	27.8	25.7	22.9	13.9
	LFE2-12E	FPBGA	17 x 17 mm	256	26.7	22.7	20.2	14.9	4.3
	LFE2-12E	FPBGA	23 x 23 mm	484	20.0	17.4	15.8	11.7	7.0
	LFE2-20E	PQFP	28 x 28 mm	208	30.2	27.8	25.7	22.9	13.9
	LFE2-20E	FPBGA	17 x 17 mm	256	24.9	21.0	18.5	13.2	3.5
	LFE2-20E	FPBGA	23 x 23 mm	484	18.7	16.1	14.4	10.1	5.6
	LFE2-20E	FPBGA	27 x 27 mm	672	17.4	15.1	13.0	10.2	4.8
	LFE2-35E	FPBGA	23 x 23 mm	484	17.7	15.2	13.4	9.0	4.7
	LFE2-35E	FPBGA	27 x 27 mm	672	16.4	14.0	12.1	8.5	4.0
	LFE2-50E	FPBGA	23 x 23 mm	484	16.7	14.2	12.3	7.9	3.9
	LFE2-50E	FPBGA	27 x 27 mm	672	15.3	13.0	11.2	7.2	3.3
	LFE2-70E	FPBGA	27 x 27 mm	672	14.3	12.0	10.3	6.0	2.7
	LFE2-70E	FPBGA	31 x 31 mm	900	12.6	10.5	9.2	6.3	2.0
LatticeECP2M™	LFE2M20E	FPBGA	17 x 17 mm	256	24.2	20.2	17.8	12.6	3.2
	LFE2M20E	FPBGA	23 x 23 mm	484	18.1	15.6	13.8	9.5	5.1
	LFE2M35E	FPBGA	17 x 17 mm	256	22.4	18.5	16.2	11.0	2.5
	LFE2M35E	FPBGA	23 x 23 mm	484	16.8	14.3	12.5	8.1	4.0
	LFE2M35E	FPBGA	27 x 27 mm	672	15.5	13.0	11.1	5.9	3.1
	LFE2M50E	FPBGA	23 x 23 mm	484	15.6	13.1	11.3	6.9	3.1
	LFE2M50E	FPBGA	27 x 27 mm	672	14.2	11.9	10.2	5.9	2.6
	LFE2M50E	FPBGA	31 x 31 mm	900	12.5	10.4	9.1	6.1	1.9
	LFE2M70E	FPBGA	31 x 31 mm	900	11.7	9.5	8.1	5.3	1.5
	LFE2M70E	FPBGA	35 x 35 mm	1152	13.7	12.0	11.0	6.5	2.0
	LFE2M100E	FPBGA	31 x 31 mm	900	10.8	8.6	7.1	4.5	1.2
	LFE2M100E	FPBGA	35 x 35 mm	1152	13.2	11.2	9.8	5.7	1.5

Table 2. Device/Package Thermal Resistance[1]

Family	Device	Package	Dimensions	Pin Count	θ_{JA} (0lfm) °C/W	θ_{JA} (200lfm) °C/W	θ_{JA} (500lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LatticeECP3™	LFE3-17	FTBGA	17 x 17 mm	256	24.5	20.6	18.2	12.9	3.3
	LFE3-17	CSBGA	10 x 10 mm	328	30.8	27.8	25.5	12.5	6.1
	LFE3-17	FPBGA	23 x 23 mm	484	18.4	15.8	14.1	9.8	5.4
	LFE3-35	FTBGA	17 x 17 mm	256	24.5	20.6	18.2	12.9	3.3
	LFE3-35	FPBGA	23 x 23 mm	484	18.4	15.8	14.1	9.8	5.4
	LFE3-35	FPBGA	27 x 27 mm	672	17.1	14.7	12.7	9.5	4.5
	LFE3-70	FPBGA	23 x 23 mm	484	15.7	13.2	11.4	7	3.2
	LFE3-70	FPBGA	27 x 27 mm	672	14.3	12	10.3	6	2.7
	LFE3-70	FPBGA	35 x 35 mm	1156	12.9	11.5	10.6	7.3	2.3
	LFE3-95	FPBGA	23 x 23 mm	484	15.7	13.2	11.4	7	3.2
	LFE3-95	FPBGA	27 x 27 mm	672	14.3	12	10.3	6	2.7
	LFE3-95	FPBGA	35 x 35 mm	1156	12.9	11.5	10.6	7.3	2.3
	LFE3-150	FPBGA	27 x 27 mm	672	13.2	10.9	9.3	4.8	2.1
	LFE3-150	FPBGA	35 x 35 mm	1156	12.2	10.5	9.2	6	1.6
LatticeSC™ /LatticeSCM™	LFSC/SCM15	FPBGA	17 x 17 mm	256	21.1	17.4	15.1	10.0	2.1
	LFSC/SCM15	FPBGA	31 x 31 mm	900	12.9	10.8	9.6	6.6	2.1
	LFSC/SCM25	FPBGA	31 x 31 mm	900	11.5	9.3	7.9	5.1	1.5
	LFSC/SCM25	FFBGA	33 x 33 mm	1020	10.1	8.1	6.7	5.1	1.1
	LFSC/SCM40	FFBGA	33 x 33 mm	1020	10.1	8.1	6.7	3.7	0.4
	LFSC/SCM40	FCBGA	35 x 35 mm	1152	9.5	6.8	5.1	2.7	0.6
	LFSC/SCM80	FCBGA	35 x 35 mm	1152	7.9	5.7	4.2	2.2	0.5
	LFSC/SCM80	FCBGA	42.5 x 42.5 mm	1704	7.7	5.5	4.0	3.0	0.5
	LFSC/SCM115	FCBGA	35 x 35 mm	1152	7.9	5.7	4.2	2.2	0.5
	LFSC/SCM115	FCBGA	42.5 x 42.5 mm	1704	7.7	5.5	4.0	3.0	0.5

Table 2. Device/Package Thermal Resistance[1]

Family	Device	Package	Dimensions	Pin Count	θ_{JA} (0lfm) °C/W	θ_{JA} (200lfm) °C/W	θ_{JA} (500lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LatticeECP5™	LFE5U-25F	CSFBGA	10 x 10 mm	285	33.1	26.8	24.3	20.7	12.5
	LFE5U-25F	CABGA	17 x 17 mm	381	21.5	15.8	13.9	11.7	6.8
	LFE5UM-25F	CSFBGA	10 x 10 mm	285	33.1	26.8	24.3	20.7	12.5
	LFE5UM-25F	CABGA	17 x 17 mm	381	21.5	15.8	13.9	11.7	6.8
	LAE5UM-25F	CSFBGA	10 x 10 mm	285	33.1	26.8	24.3	20.7	12.5
	LAE5UM-25F	CABGA	17 x 17 mm	381	21.5	15.8	13.9	11.7	6.8
	LFE5UM-45F	CSFBGA	10 x 10 mm	285	29.6	23.2	20.8	17.2	9.6
	LFE5UM-45F	CABGA	17 x 17 mm	381	20.5	14.6	12.8	10.6	5.7
	LFE5UM-45F	CABGA	23 x 23 mm	554	20.3	15.1	13.4	9.3	2.9
	LAE5UM-45F	CSFBGA	10 x 10 mm	285	29.6	23.2	20.8	17.2	9.6
	LAE5UM-45F	CABGA	23 x 23 mm	554	20.3	15.1	13.4	9.3	2.9
	LFE5U-45F	CSFBGA	10 x 10 mm	285	29.6	23.2	20.8	17.2	9.6
	LFE5U-45F	CABGA	17 x 17 mm	381	20.5	14.6	12.8	10.6	5.7
	LFE5U-45F	CABGA	23 x 23 mm	554	20.3	15.1	13.4	9.3	2.9
	LFE5U-85F	CSFBGA	10 x 10 mm	285	26.2	21.9	19.8	12.5	6.7
	LFE5U-85F	CABGA	17 x 17 mm	381	19.0	13.5	11.7	9.4	4.1
	LFE5U-85F	CABGA	23 x 23 mm	554	18.6	13.3	11.6	8.3	3.8
	LFE5U-85F	CABGA	27 x 27 mm	756	17.1	11.8	10.2	8.1	2.1
	LFE5UM-85F	CSFBGA	10 x 10 mm	285	26.2	21.9	19.8	12.5	6.7
	LFE5UM-85F	CABGA	17 x 17 mm	381	19.0	13.5	11.7	9.4	4.1
	LFE5UM-85F	CABGA	23 x 23 mm	554	18.6	13.3	11.6	8.3	3.8
	LFE5UM-85F	CABGA	27 x 27 mm	756	17.1	11.8	10.2	8.1	2.1
	LAE5UM-85F	CABGA	27 x 27 mm	756	17.1	11.8	10.2	8.1	2.1

Table 2. Device/Package Thermal Resistance[1]

Family	Device	Package	Dimensions	Pin Count	θ_{JA} (0lfm) °C/W	θ_{JA} (200lfm) °C/W	θ_{JA} (500lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
iCE40™	iCE40-LP384	QFN	5x5 mm	32	67.75	64.2	62.3	29.9	18.2
	iCE40-LP384	UCBGA	2.5 x 2.5 mm	36	138.1	128.1	123.2	57.2	35.7
	iCE40-LP384	UCBGA	3 x 3 mm	49	121.0	110.9	106.4	53.7	33.5
	iCE40-LP640	UCBGA	2.5 x 2.5 mm	36	116.2	106.6	102.1	51.9	32.5
	iCE40-LP640	UCBGA	3 x 3 mm	49	98.5	90.3	86.5	44.0	27.5
	iCE40-LP640	UCBGA	4 x 4 mm	81	83.9	72.6	69.9	33.6	24.6
	iCE40-HX640	TQFP	14 x 14 mm	100	45.5	41.7	39.1	26.7	14.2
	iCE40-LP1K	UCBGA	2.5 x 2.5 mm	36	119.3	109.7	105.2	51.9	32.5
	iCE40-LP1K	UCBGA	3 x 3 mm	49	108.5	100.3	96.5	44.0	27.5
	iCE40-LP1K	UCBGA	4 x 4 mm	81	83.9	72.6	69.9	33.6	24.6
	iCE40-LP1K	CSBGA	5 x 5 mm	81	72.7	60.1	56.3	32.5	20.3
	iCE40-LP1K	QFN	7 x 7 mm	84	46.7	43.9	42.4	15.6	14.3
	iCE40-LP1K	UCBGA	5 x 5 mm	121	79.6	74.3	71.9	45.2	22.0
	iCE40-LP1K	CSBGA	6 x 6 mm	121	70.6	64.7	60.7	61.6	18.0
	iCE40-HX1K	TQFP	14 x 14 mm	100	44.2	40.4	37.8	26.7	14.2
	iCE40-HX1K	CSBGA	8 x 8 mm	132	67.7	61.2	59.2	55.5	27.3
	iCE40-HX1K	TQFP	20 x 20 mm	144	38.5	35.4	33.3	19.8	10.0
	iCE40-LP4K	UCBGA	4 x 4 mm	81	77.0	64.3	60.6	32.8	20.5
	iCE40-LP4K	UCBGA	5 x 5 mm	121	70.7	63.1	59.8	31.6	19.7
	iCE40-LP4K	UCBGA	7 x 7 mm	225	66.7	61.1	57.4	58.0	16.9
	iCE40-HX4K	CSBGA	8 x 8 mm	132	60.2	55.2	51.8	52.3	15.3
	iCE40-HX4K	TQFP	20 x 20 mm	144	38.3	35.2	33.1	19.7	9.9
	iCE40-LP8K	UCBGA	5 x 5 mm	121	60.9	52.7	48.3	27.8	17.4
	iCE40-LP8K	UCBGA	7 x 7 mm	225	55.1	49.3	47.3	46.5	16.5
	iCE40-HX8K	CSBGA	8 x 8 mm	132	54.3	50.1	47.4	42.8	12.5
	iCE40-HX8K	UCBGA	7 x 7 mm	225	55.1	49.3	47.3	46.5	16.5
	iCE40-HX8K	CABGA	14 x 14 mm	256	42.8	38.3	36.4	39.5	11.6
iCE40 Ultra™	iCE5LP-SWG20	WLCSP	1.71 x 2.06 mm	20	76.0	70.6	67.6	55.5	16.1
	iCE5LP-UWG36	WLCSP	2.078 x 2.078 mm	36	68.2	63.1	60.4	47.8	12.7

Table 2. Device/Package Thermal Resistance[1]

Family	Device	Package	Dimensions	Pin Count	θ_{JA} (0lfm) °C/W	θ_{JA} (200lfm) °C/W	θ_{JA} (500lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
MachXO™	LCMXO256C/E	CSBGA	8 x 8 mm	100	85.4	79.4	74.4	62.8	31.9
	LCMXO256C/E	TQFP	14 x 14 mm	100	36.9	33.0	30.4	23.6	12.4
	LCMXO640C/E	CSBGA	8 x 8 mm	100	75.1	69.5	65.9	57.5	18.5
	LCMXO640C/E	TQFP	14 x 14 mm	100	36.9	33.0	30.4	23.6	12.4
	LCMXO640C/E	CSBGA	8 x 8 mm	132	67.6	62.3	58.5	50.4	16.7
	LCMXO640C/E	TQFP	20 x 20 mm	144	28.8	26.1	24.0	19.1	9.4
	LCMXO640C/E	CABGA	14 x 14 mm	256	47.8	43.8	41.1	46.1	15.1
	LCMXO640C/E	FTBGA	17 x 17 mm	256	44.9	40.3	37.8	39.0	11.4
	LCMXO1200C/E	TQFP	14 x 14 mm	100	36.9	33.0	30.4	23.6	12.4
	LCMXO1200C/E	CSBGA	8 x 8 mm	132	55.7	51.0	48.0	37.1	9.7
	LCMXO1200C/E	TQFP	20 x 20 mm	144	28.8	26.1	24.0	19.1	9.4
	LCMXO1200C/E	CABGA	14 x 14 mm	256	43.1	39.1	36.5	35.8	9.5
	LCMXO1200C/E	FTBGA	17 x 17 mm	256	41.8	36.9	34.3	33.2	7.7
	LCMXO2280C/E	TQFP	14 x 14 mm	100	36.9	33.0	30.4	23.6	12.4
	LCMXO2280C/E	CSBGA	8 x 8 mm	132	48.4	44.1	41.6	33.7	6.6
	LCMXO2280C/E	TQFP	20 x 20 mm	144	28.8	26.1	24.0	19.1	9.4
	LCMXO2280C/E	CABGA	14 x 14 mm	256	40.9	34.9	32.3	32.5	6.5
	LCMXO2280C/E	FTBGA	17 x 17 mm	256	40.0	34.9	32.3	28.7	5.1
	LCMXO2280C/E	FTBGA	19 x 19 mm	324	37.3	31.2	29.5	25.0	6.2

Table 2. Device/Package Thermal Resistance[1]

Family	Device	Package	Dimensions	Pin Count	θ_{JA} (0lfm) °C/W	θ_{JA} (200lfm) °C/W	θ_{JA} (500lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
MachXO2™	LCMXO2-256	QFN	5 x 5 mm	32	41.3	37.3	35.1	22.2	20.4
	LCMXO2-256	UCBGA	4 x 4 mm	64	71.6	59.2	55.5	32.0	20.0
	LCMXO2-256	TQFP	14 x 14 mm	100	40.8	35.5	33.3	23.6	12.4
	LCMXO2-256	CSBGA	8 x 8 mm	132	90.3	82.8	79.4	62.8	31.9
	LCMXO2-640	TQFP	14 x 14 mm	100	36.9	33.0	30.4	23.6	12.4
	LCMXO2-640	CSBGA	8 x 8 mm	132	79.8	72.3	68.9	62.8	31.9
	LCMXO2-640U	TQFP	20 x 20 mm	144	34.1	29.7	27.7	19.1	9.4
	LCMXO2-1200	WLCSP	2.5 x 2.5 mm	25	42.4	36.8	33.5	30.5	5.8
	LCMXO2-1200	TQFP	14 x 14 mm	100	36.9	33.0	30.4	23.6	12.4
	LCMXO2-1200	CSBGA	8 x 8 mm	132	69.8	62.3	59.1	62.8	31.9
	LCMXO2-1200	TQFP	20 x 20 mm	144	34.1	29.7	27.7	19.1	9.4
	LCMXO2-1200U	FTBGA	17 x 17 mm	256	43.3	38.6	36.1	36.1	9.5
	LCMXO2-2000	TQFP	14 x 14 mm	100	36.9	33.0	30.4	23.6	12.4
	LCMXO2-2000	CSBGA	8 x 8 mm	132	60.7	55.8	52.5	57.5	18.5
	LCMXO2-2000	TQFP	20 x 20 mm	144	28.8	26.1	24.0	19.1	9.4
	LCMXO2-2000	FTBGA	17 x 17 mm	256	43.3	38.6	36.1	36.1	9.5
	LCMXO2-2000	CABGA	14 x 14 mm	256	47.7	43.7	41.0	46.1	15.1
	LCMXO2-2000U	FPBGA	23 x 23 mm	484	25.2	21.5	19.5	19.9	10.3
	LCMXO2-4000	CSBGA	8 x 8 mm	132	52.8	48.3	45.5	37.1	9.7
	LCMXO2-4000	TQFP	20 x 20 mm	144	28.8	26.1	24.0	19.1	9.4
	LCMXO2-4000	FTBGA	17 x 17 mm	256	40.9	36.0	33.4	25.1	4.4
	LCMXO2-4000	CABGA	14 x 14 mm	256	42.6	38.7	36.0	32.5	6.5
	LCMXO2-4000	CABGA	17 x 17 mm	332	35.1	31.3	29.1	30.4	6.6
	LCMXO2-4000	FPBGA	23 x 23 mm	484	25.2	21.5	19.5	19.9	10.3
	LCMXO2-7000	TQFP	20 x 20 mm	144	28.8	26.1	24.0	19.1	9.4
	LCMXO2-7000	FTBGA	17 x 17 mm	256	38.7	33.8	31.0	28.4	4.4
	LCMXO2-7000	CABGA	14 x 14 mm	256	40.3	36.3	33.6	30.1	6.1
	LCMXO2-7000	CABGA	17 x 17 mm	332	33.3	29.5	27.3	26.9	5.5
	LCMXO2-7000	FPBGA	23 x 23 mm	484	23.4	19.8	17.8	18.6	7.5

Table 2. Device/Package Thermal Resistance[1]

Family	Device	Package	Dimensions	Pin Count	θ_{JA} (0lfm) °C/W	θ_{JA} (200lfm) °C/W	θ_{JA} (500lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
MachXO3™	LCMXO3L-640E	CSFBGA	6 x 6 mm	121	52.4	49.5	46.8	35.4	18.3
	LCMXO3L-1300E	WLCSP	2.487 x 2.541 mm	36	41.7	36.3	33.0	30.2	5.8
	LCMXO3L-1300E	CSFBGA	6 x 6 mm	121	52.4	49.5	46.8	35.4	18.3
	LCMXO3L-1300E	CSFBGA	9 x 9 mm	256	36.2	33.8	31.5	23.8	11.6
	LCMXO3L-1300C	CABGA	14 x 14 mm	256	47.0	43.0	40.3	44.1	13.9
	LCMXO3L-2100E	WLCSP	3.106 x 3.185 mm	49	31.4	27.6	25.5	24.5	4.8
	LCMXO3L-2100E	CSFBGA	6 x 6 mm	121	45.1	40.4	37.7	28.2	13.7
	LCMXO3L-2100E	CSFBGA	9 x 9mm	256	36.2	33.8	31.5	23.8	11.6
	LCMXO3L-2100E	CSFBGA	10 x 10mm	324	31.2	28.7	26.6	19.3	8.7
	LCMXO3L-2100C	CABGA	14 x 14 mm	256	47.0	43.0	40.3	44.1	13.9
	LCMXO3L-2100C	CABGA	15 x 15 mm	324	34.8	31.0	28.8	29.9	6.4
	LCMXO3L-4300E	WLCSP	3.797 x 3.693 mm	81	21.6	19.4	18.3	19.1	3.8
	LCMXO3L-4300E	CSFBGA	6 x 6 mm	121	39.1	34.9	32.1	22.0	10.3
	LCMXO3L-4300E	CSFBGA	9 x 9mm	256	33.2	30.9	28.5	20.9	9.5
	LCMXO3L-4300E	CSFBGA	10 x 10mm	324	31.2	28.7	26.6	19.3	8.7
	LCMXO3L-4300C	CABGA	14 x 14 mm	256	42.2	38.3	35.6	32.1	6.4
	LCMXO3L-4300C	CABGA	15 x 15 mm	324	34.8	31.0	28.8	29.9	6.4
	LCMXO3L-4300C	CABGA	17 x 17 mm	400	33.0	29.2	27.0	26.3	5.3
	LCMXO3L-6900E	CSFBGA	9 x 9mm	256	30.5	28.0	25.7	18.1	7.7
	LCMXO3L-6900E	CSFBGA	10 x 10mm	324	29.1	26.7	24.4	17.1	7.3
	LCMXO3L-6900C	CABGA	14 x 14 mm	256	39.9	35.9	33.2	29.7	6.0
	LCMXO3L-6900C	CABGA	15 x 15 mm	324	33.1	29.5	27.4	29.8	6.0
	LCMXO3L-6900C	CABGA	17 x 17 mm	400	33.0	29.2	27.0	26.3	5.3
LatticeXP™	LFXP3C/E	TQFP	14 x 14 mm	100	31.0	27.1	24.6	16.9	8.1
	LFXP3C/E	TQFP	20 x 20 mm	144	28.8	26.1	24.0	19.1	9.4
	LFXP3C/E	PQFP	28 x 28 mm	208	29.5	27.0	24.7	21.5	13.2
	LFXP6C/E	TQFP	20 x 20 mm	144	27.8	25.0	23.1	17.8	7.2
	LFXP6C/E	PQFP	28 x 28 mm	208	30.2	27.8	25.7	22.9	13.9
	LFXP6C/E	FPBGA	17 x 17 mm	256	25.7	21.6	19.4	14.1	5.3
	LFXP10C/E	FPBGA	17 x 17 mm	256	23.4	19.5	17.2	11.9	2.9
	LFXP10C/E	FPBGA	23 x 23 mm	388	17.6	15.0	13.2	8.9	4.6
	LFXP15C/E	FPBGA	17 x 17 mm	256	21.6	18.1	15.6	11.6	1.5
	LFXP15C/E	FPBGA	23 x 23 mm	388	16.1	13.5	11.9	7.6	3.8
	LFXP15C/E	FPBGA	23 x 23 mm	484	16.3	14.0	12.0	7.3	3.7
	LFXP20C/E	FPBGA	17 x 17 mm	256	21.9	17.8	15.6	9.6	2.8
	LFXP20C/E	FPBGA	23 x 23 mm	388	16.2	13.7	11.8	7.4	3.5
	LFXP20C/E	FPBGA	23 x 23 mm	484	16.2	13.7	11.8	7.4	3.5

Table 2. Device/Package Thermal Resistance[1]

Family	Device	Package	Dimensions	Pin Count	θ_{JA} (0lfm) °C/W	θ_{JA} (200lfm) °C/W	θ_{JA} (500lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LatticeXP2™	LFXP2-5E	CSBGA	8 x 8 mm	132	47.2	43.0	40.5	32.7	6.1
	LFXP2-5E	TQFP	20 x 20 mm	144	28.8	26.1	24.0	19.1	9.4
	LFXP2-5E	PQFP	28 x 28 mm	208	30.2	27.8	25.7	22.9	13.9
	LFXP2-5E	FTBGA	17 x 17 mm	256	39.1	34.1	31.4	29.4	6.1
	LFXP2-8E	CSBGA	8 x 8 mm	132	41.9	38.0	35.8	28.4	4.4
	LFXP2-8E	TQFP	20 x 20 mm	144	28.8	26.1	24.0	19.1	9.4
	LFXP2-8E	PQFP	28 x 28 mm	208	30.2	27.8	25.7	22.9	13.9
	LFXP2-8E	FTBGA	17 x 17 mm	256	37.2	32.3	29.5	27.0	5.1
	LFXP2-17E	PQFP	28 x 28 mm	208	30.2	27.8	25.7	22.9	13.9
	LFXP2-17E	FTBGA	17 x 17 mm	256	33.9	29.1	26.2	23.7	4.3
	LFXP2-17E	FPBGA	23 x 23 mm	484	18.6	16.0	14.3	10.0	5.5
	LFXP2-30E	FTBGA	17 x 17 mm	256	32.0	27.1	24.2	20.7	3.0
	LFXP2-30E	FPBGA	23 x 23 mm	484	17.3	14.8	13.0	8.6	4.4
	LFXP2-30E	FPBGA	27 x 27 mm	672	16.0	13.6	11.7	7.9	3.7
	LFXP2-40E	FPBGA	23 x 23 mm	484	16.5	14.0	12.1	7.7	3.7
	LFXP2-40E	FPBGA	27 x 27 mm	672	15.1	12.7	10.9	6.8	3.1
Platform Manager™	LPTM10-1247	TQFP	14 x 14 mm	128	33.7	29.5	27.0	17.7	15.5
	LPTM10-12107	FTBGA	17 x 17 mm	208	37.7	34.3	31.8	24.2	18.3

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1. The data shown in this Thermal Management document is relative and actual values depend on a variety of factors such as: die size, paddle size, airflow, power applied, printed circuit board design, proximity of other devices and user applications. This table specifies the device/package specific thermal resistance for newer FPGA products. These values are based upon JEDEC standards.

Revision History

Date	Version	Change Summary
October 2014	2.6	Updated Table 2 Device/Package Thermal Resistance. Included ECP5 packages.
September 2014	2.5	Updated Table 2 Device/Package Thermal Resistance. Included MachXO3L packages.
June 2014	2.4	Updated Table 2 Device/Package Thermal Resistance. Included iCE40 Ultra packages.
May 2014	02.3	Updated Table 2, Device/Package Thermal Resistance. Changed LCMXO2-1200 TQFP package dimensions to 20x20 mm.
May 2014	02.2	Added Platform Manager information.
August 2013	02.1	Added iCE40 and MachXO2 information.
August 2012	02.0	Added iCE40 information.
March 2012	01.9	Updated MachXO2 and LatticeECP3 families to reflect current product availability.
February 2012	01.8	Updated document with new corporate logo.
February 2011	01.7	Added MachXO2 information.
July 2009	01.6	Added new caBGA packaging.
		Added LatticeECP3 information.
		Added θ_{JB} column in Device/Package Thermal Resistance table.
April 2009	01.5	Added new QFNS, ucBGA, csBGA, and caBGA packaging.
October 2008	01.4	Added units (°C/W) to Thermal Resistance tables.
April 2008	01.3	Added 64-ball csBGA and 144-ball csBGA packaging to Table 1.
March 2008	01.2	Corrected equation on page 1.
January 2008	01.1	Updated Table 1 with information for ftBGA 256 packaging.
September 2007	01.0	Updated Table 1 and added Table 2: Device/Package Thermal Resistance.
–	–	Previous Lattice releases.