ispLEVER 5.0 Release Notes for Windows

Windows XP
Windows 2000

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Check the Lattice Semiconductor Web site or ispUPDATE for updates to this software release. The Web site is available at:

`www.latticesemi.com/software`

To access ispUPDATE, choose ispUPDATE from the Lattice Semiconductor program group in the Windows Start Menu.

New Features

This section describes the new device support, applications, and features that are available in the ispLEVER 5.0 software.

Upgrade of HDL-BASE Software Installation Option

This release marks a significant upgrade of the HDL-BASE software installation to support all Lattice devices, eliminating the HDL-ADVANCED and ADVANCED SYSTEM installation options. All users with current maintenance will be updated to HDL-BASE in the Lattice database.

New Device Support

Preliminary Device Support

This release adds preliminary support for the following devices:

- LatticeXP 10

Silicon timing delay models for devices with preliminary support are subject to change.

Note

Designs targeting the LatticeECP/EC FPGA families will be automatically migrated to production devices. ES versions of the LatticeECP/EC FPGAs are no longer available.

Precision RTL Synthesis to Replace LeonardoSpectrum

ispLEVER 5.0 marks the full integration of Mentor Graphics's Precision RTL Synthesis 2005a.122 into the ispLEVER software suite. Precision RTL Synthesis is a more powerful and designer-friendly synthesis tool from Mentor Graphics, replacing LeonardoSpectrum as the preferred Mentor Graphics synthesis tool in ispLEVER. LeonardoSpectrum 2004b Update 1 is included for use with ispLEVER 5.0. A final release of LeonardoSpectrum for use with ispLEVER will be made available by July, 2005. Lattice will continue to support LeonardoSpectrum until December, 2005 and encourages you to make the transition to Precision RTL Synthesis in ispLEVER 5.0 in order to harness the new features and improved performance of this synthesis software in your Lattice device designs.

Module/IP Manager

For LatticeECP/EC and LatticeXP devices, the True Dual Port RAM (RAM_DP_TRUE) module and the Single Port RAM (RAM_DQ) module support read-before-write memory configurations in x9, x18, and x36 data width. Set the data width to match this requirement.

Timing-Driven Flow

This release supports a timing-driven flow for ispMACH4000, ispLSI5000VE, ispMACH5000B, ispMACH5000VG, and ispXPLD5000MX device families. From the Constraint Editor Timing Constraints sheet, you can define the maximum frequency (F_{max}) for each clock domain or for all clock domains. You can also define it as a clock period, in nanoseconds. You can choose from a list of available clocks in your design. You also can define the pin-to-pin delay, Tpd, in nanoseconds.

After you define the goals, the software fits the design to satisfy them. After the design is fit, you can view the timing report to check whether your timing goals were met.

Place and Route

The Place and Route (PAR) process has added the following command-line options.

In general, the syntax of all options is in the following format:

```
par -exp option=value
```

- `parPlcInLimit`

The input sharing option sets the input limitation for the PLC during placement.

The syntax of this option is as follows:

```
parPlcInLimit=off|low|high
```

- `off`

  Specifies no limits. You can use a very high input number, as long as the total does not exceed the hardware limit.

- `low`

  Specifies a low usage of PLC inputs.

- `high`

  Specifies a relatively high usage of PLC inputs.

If the design has poor routablity, you can try `parPlcInLimit=high`. If the design is severely congested, try `parPlcInLimit=low`. This setting normally has an impact on the maximum frequency.

- `parClkNetWeight`

  The performance-driven clock selection option sets the weight factor between the fanouts and the performance constraints. The default clock selection approach is based on the net fanouts.

  The syntax of this option is as follows:

  `parClkNetWeight=`*`value`*

  `Value` can be any number. If it is 150, the weight for the critical net will be fanout * 1.5, so the critical net will be more likely selected as the primary clock. If *`value`* is less than 100, the weight for the critical net will be equivalent to 100, which is the default.

- `M5GRipUp`

  The M5G-specific ripup option determines whether the router uses the LatticeEC- or LatticeXP-specific ripup method, which usually improves the routability of the design.

  The syntax of this option is as follows:

  ```
  M5GRipUp=ON|OFF
  ```

  When you set this option to `ON`, the router uses the LatticeEC- or LatticeXP-specific ripup method. When you set it to `OFF`, the router does not use this method. The default is `ON`.

- `M5GRoutingOrder`

The M5G-specific routing order option determines whether the router uses the LatticeEC- or LatticeXP-specific routing order.

The syntax of this option is as follows:

```
M5GRoutingOrder=0|1
```

When you set this option to `0`, the router uses the rgular routing order. When you set it to `1`, the router uses the LatticeEC- or LatticeXP-specific routing order, which usually improves the timing of short connects. The default is `0`.

Enhancements

This section describes feature enhancements that are available in the ispLEVER 5.0 software.

FPGAs

The following features have been added to Lattice's FPGA design software in this release.

Top-Level Schematic

Top-level schematic support with underlying HDL has been added to LatticeECP/EC, and LatticeXP device families.

Note

The schematic file must be the top-level source in the design hierarchy.

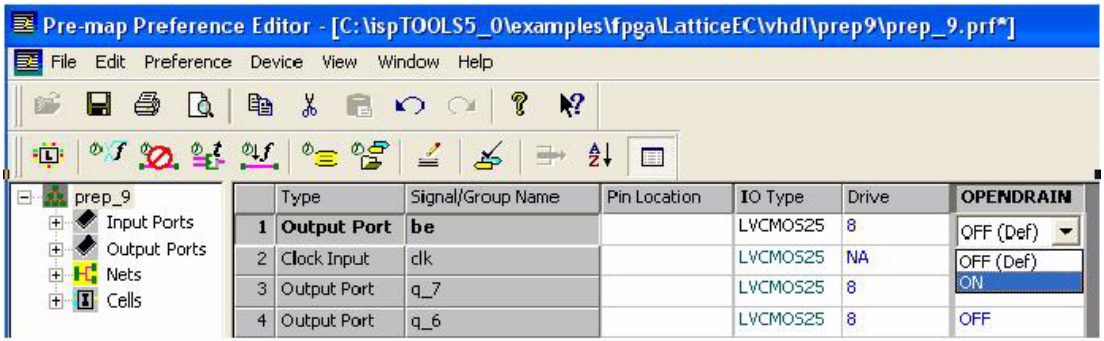
Pin attributes should be assigned at the HDL level or in the Preference Editor.

Programmable Open Drain Support

The ispLEVER software now supports programmable open drains for the LatticeECP/EC and LatticeXP device families through the Pre-Map Preference Editor.

Select the input or output pin that needs open drain support in the Preference Sheet Pane. The PAD Report (`.pad`) file, which contains a listing of all PICs

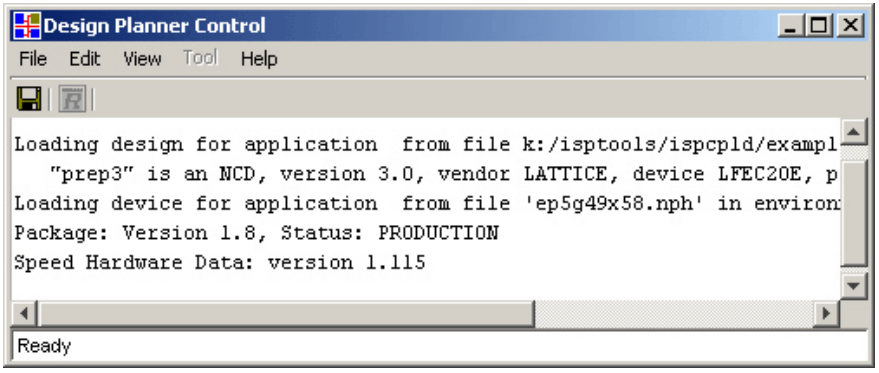
used in the design and their associated primary pins, reports the signals that have been implemented as open drains.



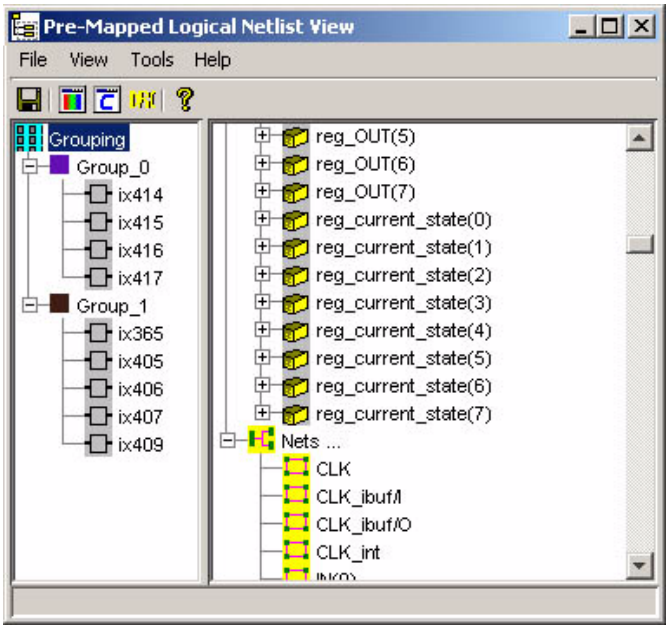
Floorplanner

The FPGA Floorplanner has been enhanced with a new Design Planner Control and separate Pre-mapped, Package, Post-mapped, Floorplan, and Physical views. Each of these views contains its own toolbar and menu bar and allows you to examine mapping, placement, and routing in a graphical, color-coded format. Each view enables you to cross-locate design elements in other views, run design rule check (DRC), and save changes to the design file.

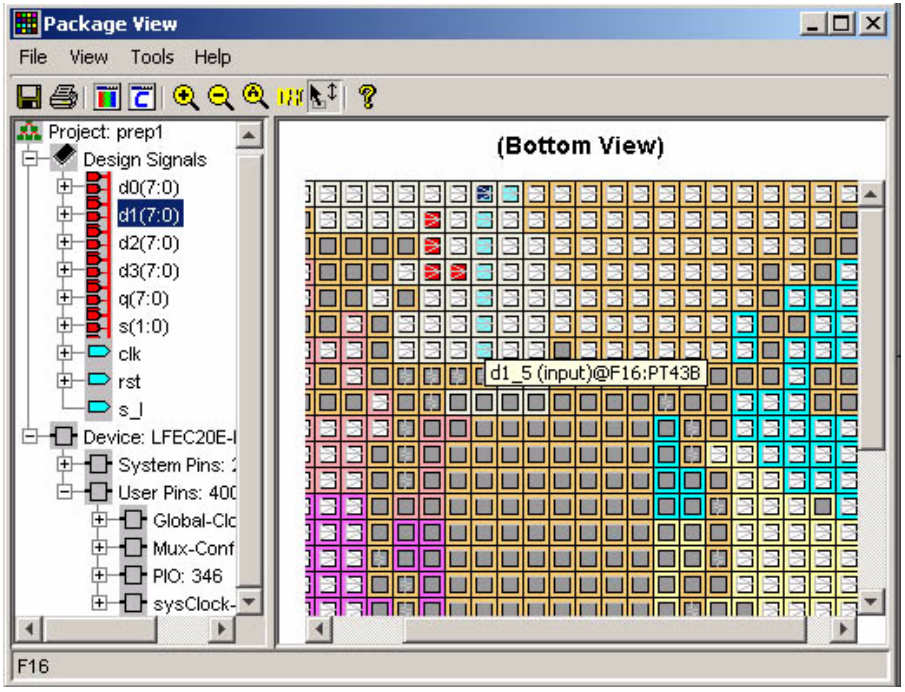
Design Planner Control The Design Planner Control serves as the gateway to the Floorplanner. It remains open as you work, giving you menu access to all Floorplanner views and the Undo and Redo commands.



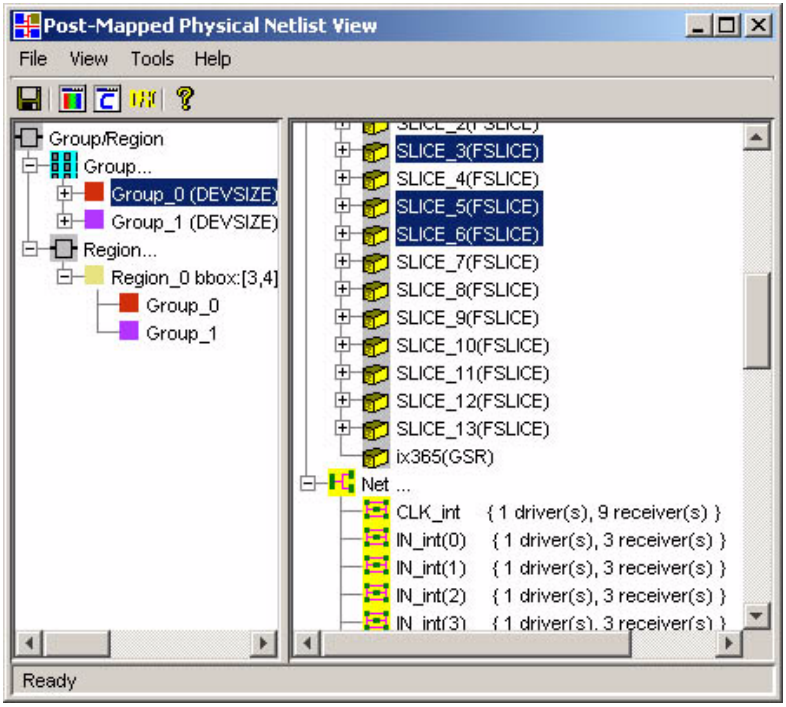
Pre-Mapped View The Pre-Mapped Logical Netlist View displays the logical components of your design and allows you to create logical groups (UGROUPs) of instances that you want mapped in close proximity. It also displays a list of all nets.



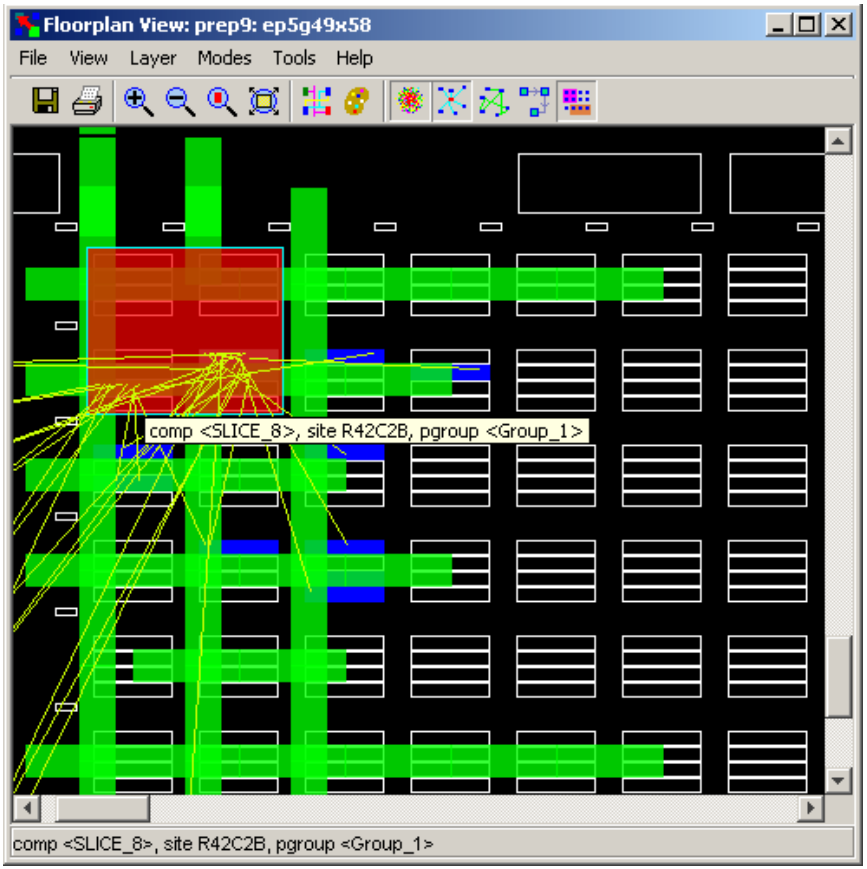
Package View The Package View shows how device pins are utilized. It provides a design tree listing of signals and pins and a design pin layout with color-coded I/O banks. You can assign I/Os in this view.



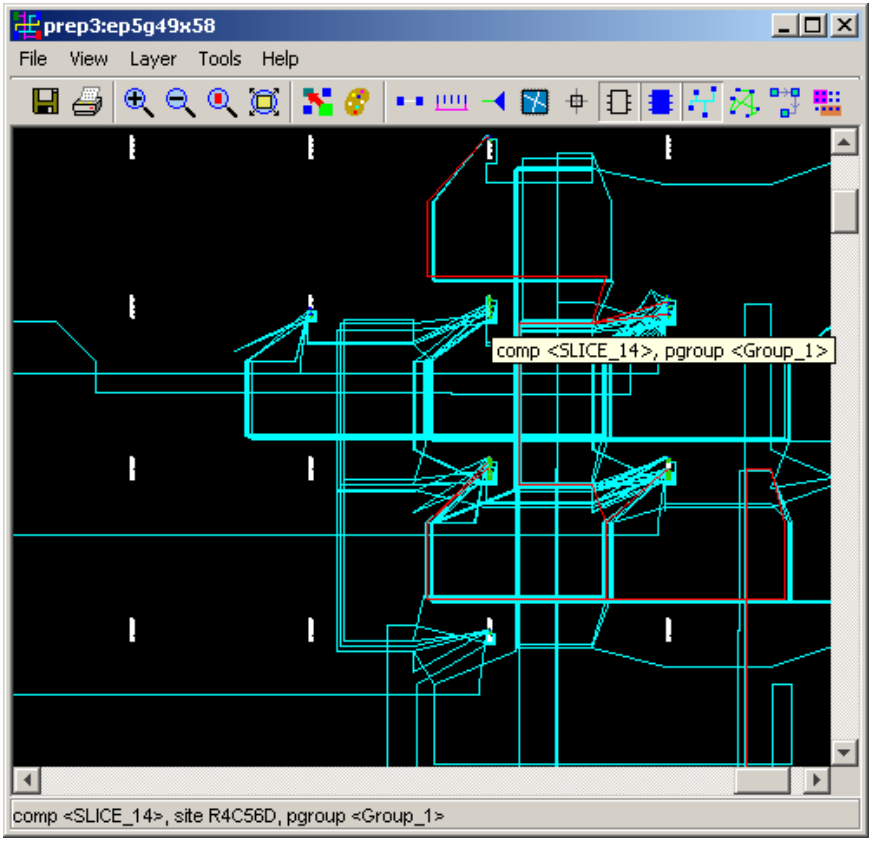
Post-Mapped Physical Netlist View The Post-Mapped Physical Netlist View displays the mapped components of your design and allows you to create and edit physical groups (PGROUPs) and regions.



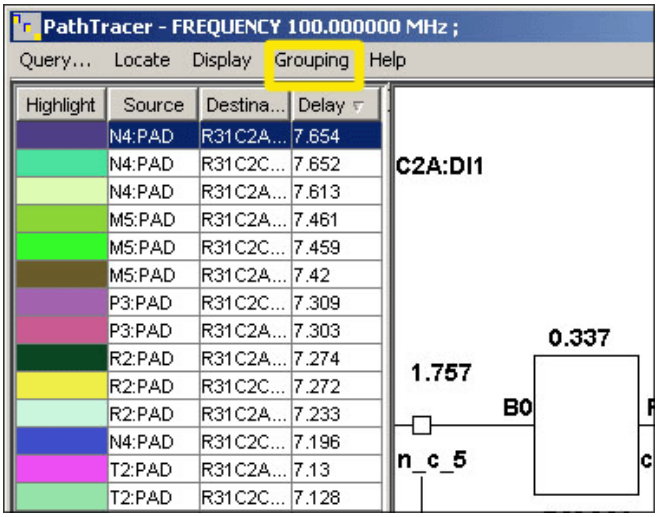
Floorplan View The Floorplan View provides a convenient large-component design layout. It shows placement and routing and provides toolbar and menu commands for displaying PGROUPS and REGIONs, utilized and reserved resources, channel congestion, and connections. For each component, it provides an interactive Detailed Logic View of configuration and logic.



Physical View The Physical View provides a more detailed small-component layout of your design and enables you to view components such as switch boxes and pin wires.



Path Tracer The Path Tracer now includes a Grouping button, allowing you to create a physical group from components in selected paths. It also includes a highlighting feature that color-codes selected paths as they are cross-located in the Floorplan View.



Power Calculator

The following enhancements were added to the Power Calculator in this release.

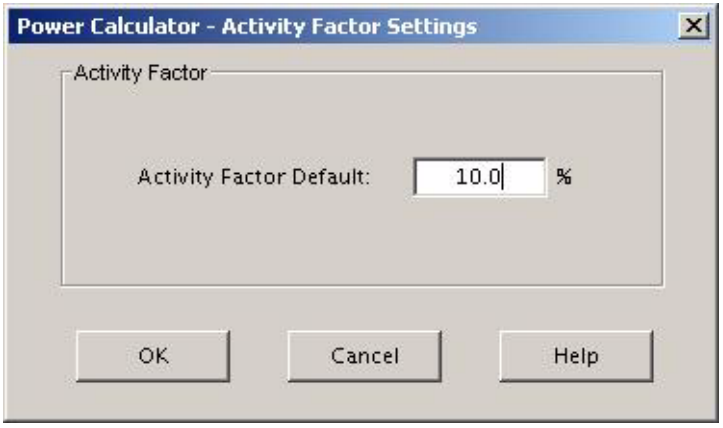
Power Consumed at Power Up The Power View, Icc View, and Report tabs now display the amount of power or current consumed by the device when the power is first turned on. This figure is not included in the total estimated power for the design. It is also shown separately under Power Up DC Power and Power Up DC Icc in the text or HTML report in the Report tab.

Drive Included in I/O Type The I/O row in the Power View and Icc View tabs specify the type of I/O, including the drive. The drive is preceded by an underscore.

Trace Report (TWR) File You can import a trace report (TWR) file into the Power Calculator. This file is an FPGA timing report file produced by the TRACE Report process in the Project Navigator. It enables you to determine to what extent the timing constraints for a design have been met. When you import this file, the Power Calculator uses the frequencies from it to populate the Frequency fields on the main window spreadsheet. However, to obtain frequencies from a TWR file, you must have a frequency constraint on the

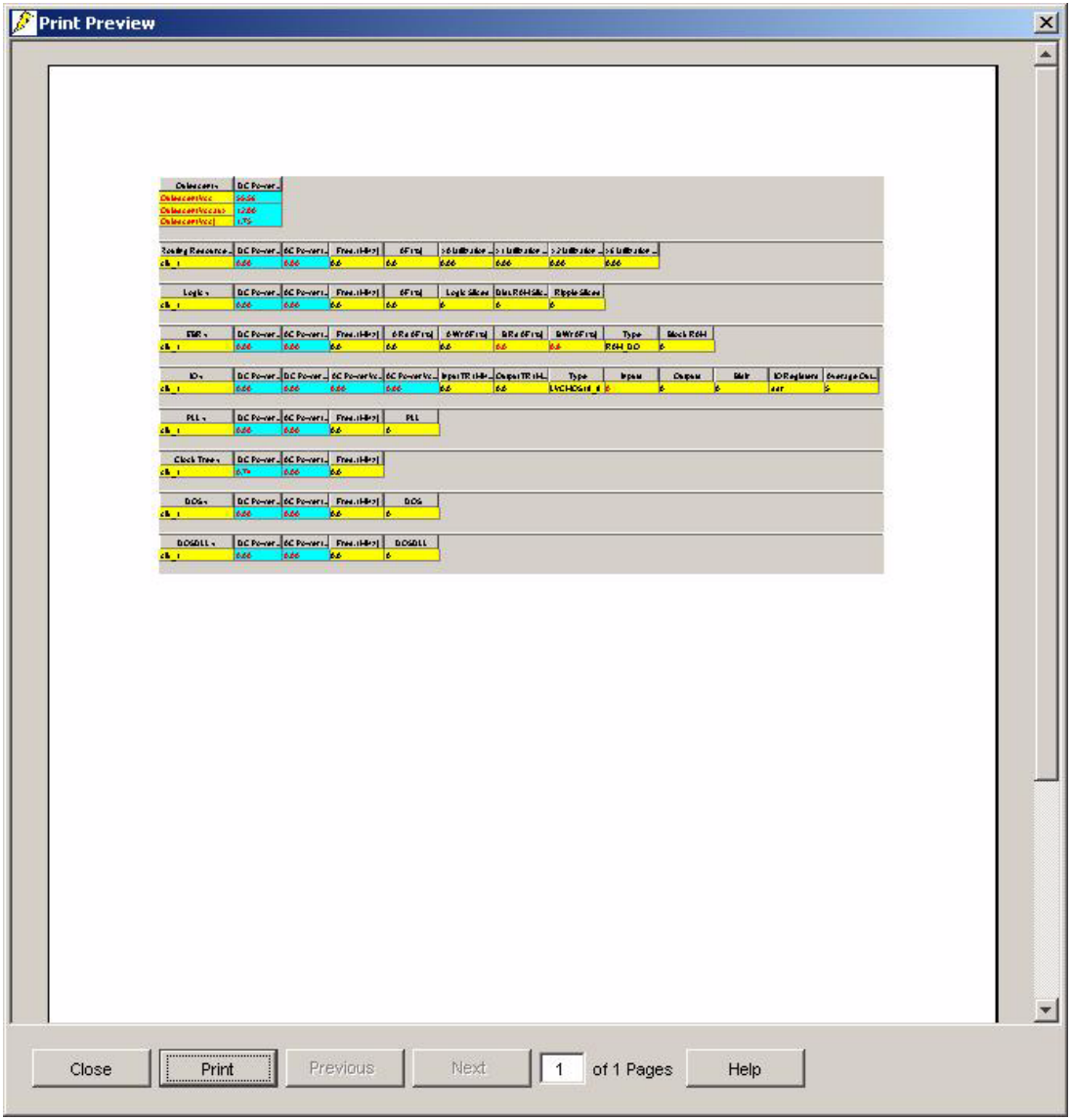
clock net; otherwise, no frequencies will be entered into the Power Calculator. You can import the TWR file by selecting File > Open Trace Report File.

Activity Factor Settings Command The Power Calculator automatically assigns a default activity factor of 10 percent in the fields of the Power View tab and the Icc View tab that display an activity factor, such as AF (%), or that use an activity factor in calculations, such as Input TR (MHz). These default values appear in blue font. However, you can globally change this default activity factor by selecting the new **Edit > New Activity Factor Settings** command. This command activates the Activity Factor Settings dialog box. Enter the new activity factor in the **Activity Factor Default** box, and click **OK**.

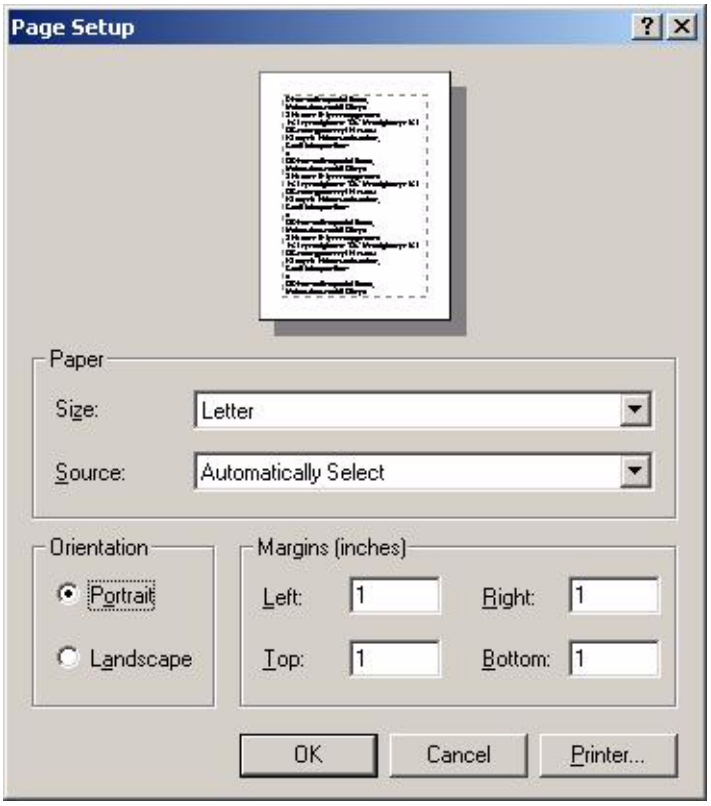


All the default activity factors appearing in blue font on the Power View and Icc View tabs are changed to the new activity factor. The Power Calculator automatically saves the new default.

Previewing Multiple-Page Report The File > Print Preview command now activates a dialog box that can display reports with multiple pages. When the report has multiple pages, you can use the Next and Previous buttons to navigate through them.


Print Preview
Close
Print
Previous
Next
1
of 1 Pages
Help

New Page Setup Command The new File > Page Setup command activates the Page Setup dialog box so that you can specify the layout of the report file to be printed and the printer on which it will be printed.



ispTRACY IP Manager

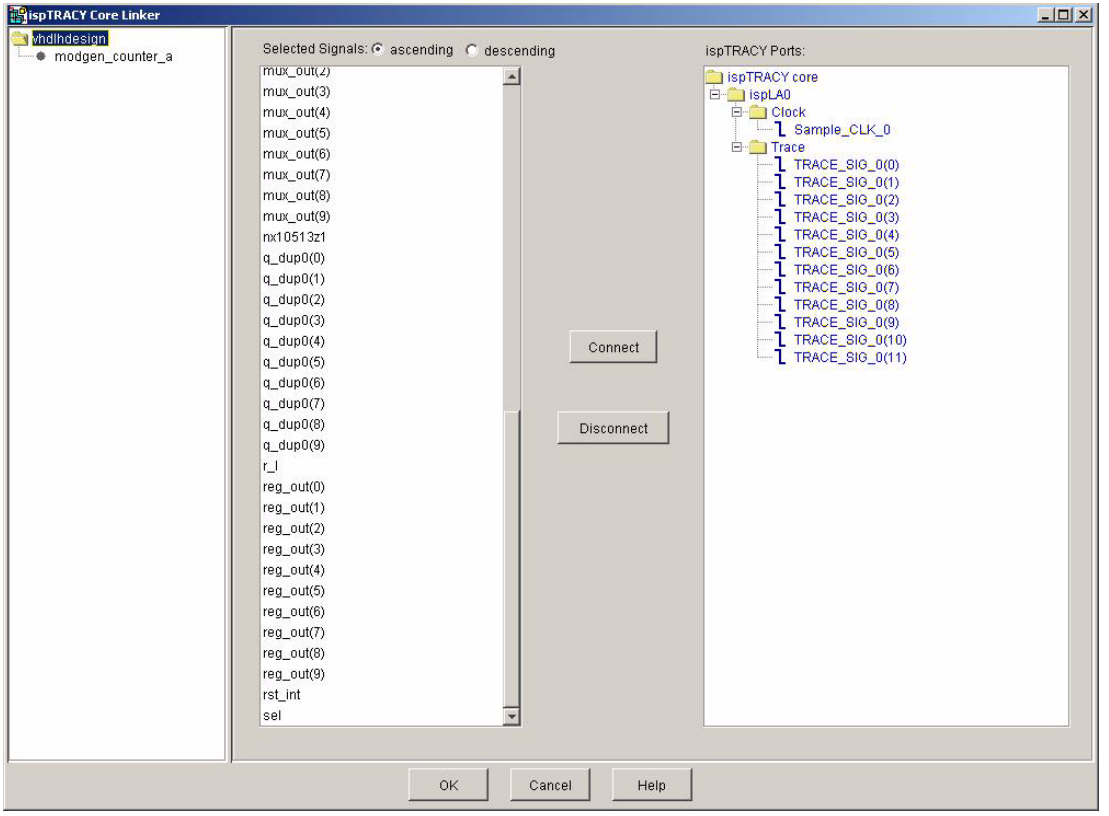
The ispTRACY IP Manager has added the following new functionality in this release.

FPGA Device Support The ispTRACY IP Manager can now be used with LatticeECP/EC, LatticeXP, and ispXPGA devices.

EDIF Netlist Flow In addition to instantiating a logic analysis core in the RTL code of your design, you can now instantiate logic analysis, or debugging, ispTRACY cores in an NGO file derived from the EDIF netlist. The Core Linker reads the input EDIF netlist and generates an NGO file containing a top-level module with the ispTRACY information. The EDIF flow automates the inclusion of the core logic into your design and eliminates a second

synthesis process in merging the original design logic with the core logic. This flow is faster and involves less effort.

Core Linker Window for the EDIF Netlist Flow The ispTRACY IP Manager features a new Core Linker window for the EDIF netlist flow. It performs the same function as the Core Linker in the RTL instantiation flow.



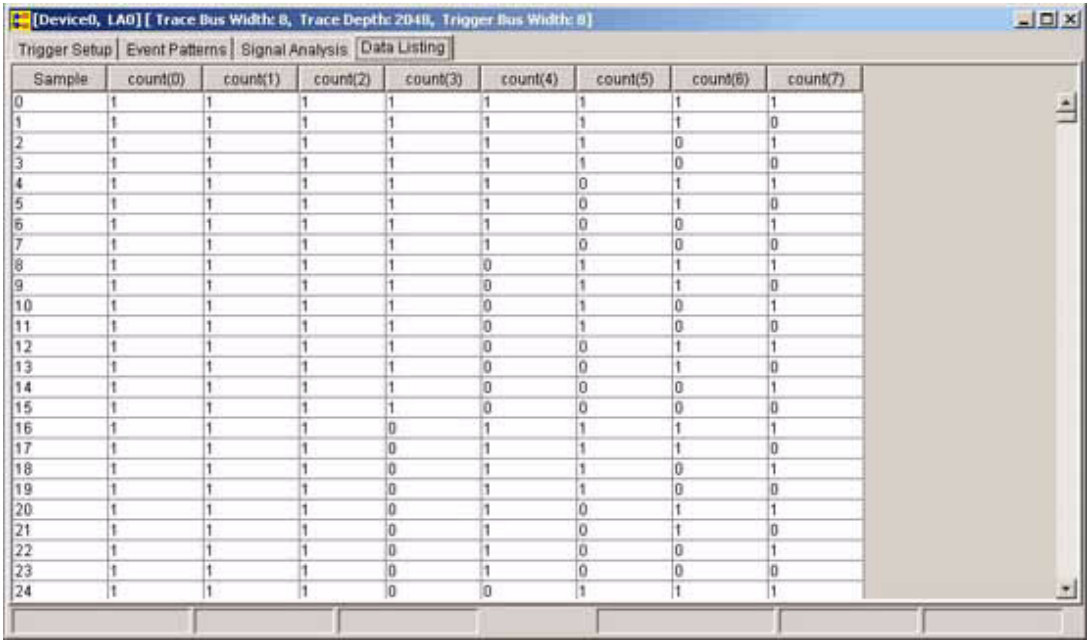
Multiple Modules You can create multiple modules in the EDIF flow and use the new Set Active button in the Core Entry window to designate which module should be used in the design flow. First you assign the name of the module in the Module Name box, then click Customize to customize the cores in that module. Next you use the Core Linker to link the cores to the signals in the design. Repeat this process for each module that you want to configure. When you have finished all module configurations, use the Set Active button to select the module to be used by the downstream tools. The name of the active module now appears in the Active Module in ispLEVER field.

ispTRACY Logic Analyzer

The ispTRACY Logic Analyzer now includes the following features.

FPGA Device Support The ispTRACY Logic Analyzer can be used with FPGA devices.

Data Listing Tab A new tab called the Data Listing tab shows the state of each signal or bus in each data sample. The data corresponds to the points on the waveforms shown in the Signal Analysis tab.



Sample	count(0)	count(1)	count(2)	count(3)	count(4)	count(5)	count(6)	count(7)
0	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	0
2	1	1	1	1	1	1	0	1
3	1	1	1	1	1	1	0	0
4	1	1	1	1	1	0	1	1
5	1	1	1	1	1	0	1	0
6	1	1	1	1	1	0	0	1
7	1	1	1	1	1	0	0	0
8	1	1	1	1	0	1	1	1
9	1	1	1	1	0	1	1	0
10	1	1	1	1	0	1	0	1
11	1	1	1	1	0	1	0	0
12	1	1	1	1	0	0	1	1
13	1	1	1	1	0	0	1	0
14	1	1	1	1	0	0	0	1
15	1	1	1	1	0	0	0	0
16	1	1	1	0	1	1	1	1
17	1	1	1	0	1	1	1	0
18	1	1	1	0	1	1	0	1
19	1	1	1	0	1	1	0	0
20	1	1	1	0	1	0	1	1
21	1	1	1	0	1	0	1	0
22	1	1	1	0	1	0	0	1
23	1	1	1	0	1	0	0	0
24	1	1	1	0	0	1	1	1

XCF File No Longer Required The ispTRACY Logic Analyzer no longer requires an XCF file as input. It obtains the information that it requires directly from the device on your board.

Demonstration Design Although a board using a Lattice FPGA device is normally required to run the ispTRACY Logic Analyzer, the ispTRACY Logic Analyzer now includes a demonstration design that you can run without the board so that you can learn how to use the tool.

Token File You can now use a token (TOK) file to assign labels to bus values. These labels identify all bus values the same way for clarity, without regard to the radix notation in which the values appear. You can create a token file, which is an ASCII file, with a text editor. To use a token file, highlight a bus or a signal in the Signal Analysis tab in an ispLA window and click the

right mouse button to activate a popup menu. The Set Token File command on this menu instructs the ispTRACY Logic Analyzer to use a token file.

New File Menu Commands Two new commands have been added to the File menu:

- The File menu now lists the four most recently opened files.
- The File > Print Preview command has been added to enable you to view the waveforms before printing them.

New Data Menu Commands Four new commands have been added to the Data menu to help you manage X and O markers in the waveform display:

- Data > Snap to Edge, which snaps the X, O, and T markers to the edge of the time interval
- Data > Snap to Center, which snaps the X, O, and T markers to the center of the time interval
- Data > Zoom > Zoom Previous, which undoes the last zoom on a waveform and reverts to the previously zoomed view
- Data > Zoom > Zoom to X-O, which zooms the area between the X and O markers on the waveform view

T Marker In the Signal Analysis tab, the ispTRACY Logic Analyzer automatically places a T marker to indicate the position of the trigger on the waveform. You can view the state of the signal at the point marked by the T marker in the T column on the Signal Analysis tab. When you use One Shot mode on the Trigger Setup tab, you can locate the T marker, but you cannot place it or move it. When you use Sample Around Trigger Mode, more than one trigger appears in the waveform, and you can only move the T marker to these triggers. Use the [<-T] and [T->] buttons to move the T marker in this mode.

Sample Around Trigger Option The Sample Around Trigger option has been added to the Trace Mode section of the Trigger Setup tab. With this option, the ispTRACY core captures and stores data only near a trigger point that you specify. You can specify how many samples before the trigger and how many samples after the trigger you would like to examine. In this mode, the sampled trace bus data is stored to a trace buffer. When the trigger condition is met, the contents of the trace buffer are placed in the trace memory. The size of this trace buffer is defined by the number of samples before the trigger. After the trigger condition is met, the trace control block keeps storing the sampled trace bus data in the trace memory until the user-defined number of samples is stored. The trace stops only when the trace memory is full or you force it to stop. The number of samples before the

trigger and the number of samples after the trigger are independent. Sampling before the trigger is not yet supported in some FPGA families.

The Sample Around Trigger option is enabled when the Sample_Around_Trigger Mode Logic option is set in the ispTRACY IP Manager Core dialog box.

The Samples box specifies how many total samples to capture into the trace memory before and after the trigger condition matches that set in the Trigger Condition section of the Trigger Setup tab.

The Samples Before Trigger box specifies how many samples to capture into the trace memory before the trigger condition matches that set in the Trigger Condition section of the Trigger Setup tab.

The number of samples captured after the trigger condition is matched is assumed to be the total number of samples minus the number of samples captured before the trigger condition matches.

MAP Report File Enhancement

LatticeXP devices include new reporting features. The map report (`.mrp`) file has been enhanced to include LUT counts within slices. Refer to topics in the help system on the map report file for more details and example files.

Minimum/Maximum Timing Analysis in TRACE

The minimum and maximum delay provides more accurate setup- and hold-time checks in TRACE.

The default speed grade for the setup-time analysis is the selected speed grade of the chosen device. However, you can specify a different speed grade by using the Override Speed Grade field in the dialog box activated by the Tools > Trace Option menu command.

The default speed grade for the hold-time analysis is `-m`, which represents the best process, lowest temperature, and highest voltage. However, you can specify a different speed grade by using the Override Speed Grade field in the dialog box activated by the Tools > Trace Option menu command. The `-m` speed grade is only available for timing analysis, and you can only select it through the Override Speed Grade field in the dialog box activated by the Tools > Trace Option menu command. You cannot select it through the device selector.

New preferences are supported to provide the junction temperature and voltage information for derating. The same preferences are supported in the

Post-Map and Post-Par Preference Editor. The only preference that is not supported in the Post-Map Preference Editor is VREF_DERATE.

The following is the derating preferences syntax:

```
TEMPERATURE <temp_value>;
VCC_DERATE <volt_spec_vcc>;
VCCAUX_DERATE <volt_spec_vccaux>;
VCCIO_DERATE [BANK] <bank_id> <volt_spec_vccio>;
VREF_DERATE <vccref_signal_name> <volt_spec_vref>;
```

This syntax contains the following parameters:

- The TEMPERATURE keyword defines the junction temperature. The *temp_value* value specifies the junction temperature in degrees Celsius.
- The VCC_DERATE keyword defines the core voltage.

  volt_spec_vcc := NOMINAL|PERCENT (+*number*|-*number*)

  - NOMINAL is the nominal VCC core voltage value.
  - PERCENT (+*number* | -*number*) is the nominal VCC value, plus *number*% of VCC value or nominal VCC value, minus *number*% of VCC value. The legal range is +5 to –5 in increments of 1.
- The VCCAUX_DERATE keyword defines the VCCAUX I/O voltage.

  volt_spec_vccaux := NOMINAL|PERCENT (+*number*|-*number*)

  - NOMINAL is the nominal VCCAUX voltage value.
  - PERCENT (+*number* | -*number*) is the nominal VCCAUX value, plus *number*% of VCCAUX value or nominal VCCAUX value, minus *number*% of VCCAUX value. The legal range is +5 to –5 in increments of 1.
- The VCCIO_DERATE keyword defines the VCCIO bank voltage. The BANK keyword is optional. The *bank_id* value specifies the bank number of an I/O bank.

  volt_spec_vccio := NOMINAL|PERCENT (+*number*|-*number*)

  - PERCENT (+*number*| -*number*) is the nominal VCCIO value, plus *number*% VCCIO value of the buffer type placed in a particular I/O bank or nominal VCCIO value, minus *number*% VCCIO value of the buffer type placed in a particular I/O bank. The legal range is +5 to –5 in increments of 1.
- The VREF_DERATE keyword defines VREF bank voltage. The *vccref_signal_name* value specifies the VREF signal name for an I/O

bank. The *vccref_signal_name* is an I/O signal configured as VREF. Each I/O bank can have up to two VREF voltages defined.

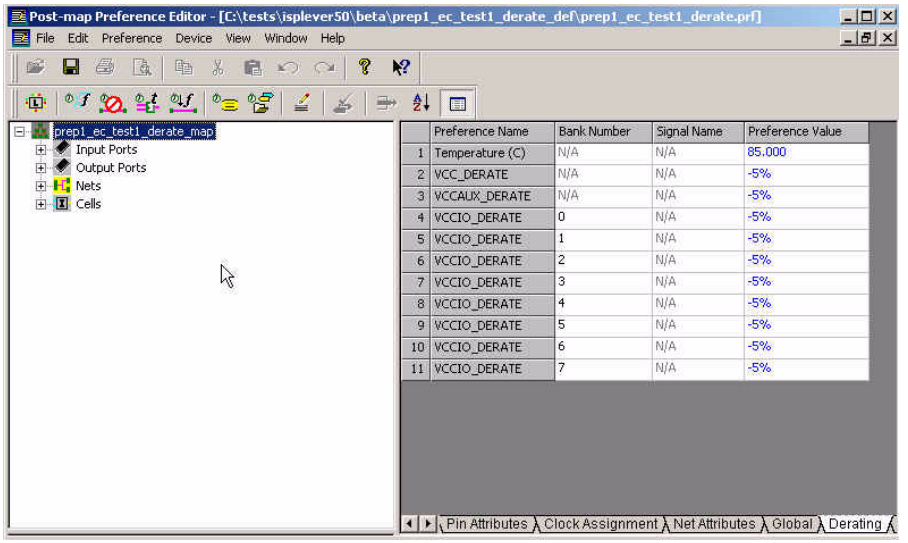
volt_spec_vref := NOMINAL|PERCENT (+*number*|-*number*)

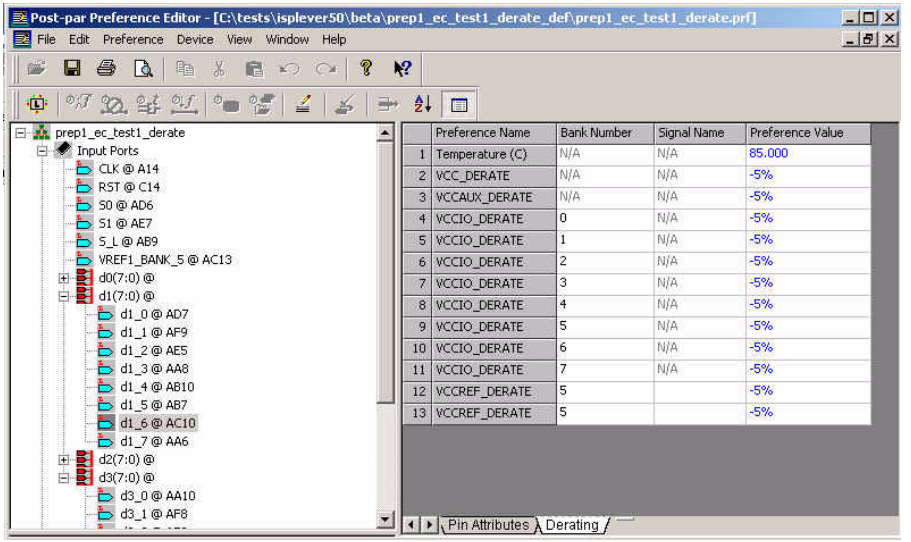
- NOMINAL is the nominal VREF value of the buffer type placed in a particular I/O bank.
- PERCENT (+*number*| -*number*) is the nominal VREF value, plus *number*% VREF value of the buffer type placed in a particular I/O bank or nominal VREF value, minus *number*% VREF value of the buffer type placed in a particular I/O bank. The legal range is +5 to –5 in increments of 1.

Here is an example:

```
TEMPERATURE 25C;
VCC_DERATE NOMINAL;
VCCAUX_DERATE NOMINAL;
VCCIO_DERATE BANK 0 NOMINAL;
VCCIO_DERATE BANK 1 NOMINAL;
VCCIO_DERATE BANK 2 NOMINAL;
VCCIO_DERATE BANK 3 NOMINAL;
VCCIO_DERATE BANK 4 NOMINAL;
VCCIO_DERATE BANK 5 NOMINAL;
VCCIO_DERATE BANK 6 NOMINAL;
VCCIO_DERATE BANK 7 NOMINAL;
VREF_DERATE ref_sig1 NOMINAL;
VREF_DERATE ref_sig2 NOMINAL;
```

The Derating tab in the Preference Editor that supports the derating commands is shown in the following illustrations.





The following sample trace report illustrates the changes related to minimum-maximum derating:

```
Lattice TRACE Report, Version ispLever_v50_Production_Build
(28)
Thu Mar 24 18:05:09 2005
```

```
Copyright (c) 1991-1994 by NeoCAD Inc. All rights reserved.
Copyright (c) 1995 AT&T Corp.   All rights reserved.
Copyright (c) 1995-2001 Lucent Technologies Inc.  All rights
reserved.
Copyright (c) 2001 Agere Systems   All rights reserved.
Copyright (c) 2002-2005 Lattice Semiconductor Corporation,  All
rights reserved.

Report Information
------------------
Command line:    trce.exe -o prep1_ec_test1_derate_nom.twr
prep1_ec_test1_derate_nom.ncd prep1_ec_test1_derate_nom.prf
Design file:     prep1_ec_test1_derate_nom.ncd
Preference file: prep1_ec_test1_derate_nom.prf
Device,speed:    LFEC20E,5
Report level:    verbose report, limited to 1 item per
preference
--------------------------------------------------------------------

Derating parameters
-------------------
Temperature:   25 C
VCC percentage set: +0 % of NOMINAL
VCCIO percentage set for bank 0: +0 % of NOMINAL
VCCIO percentage set for bank 1: +0 % of NOMINAL
VCCIO percentage set for bank 2: +0 % of NOMINAL
VCCIO percentage set for bank 3: +0 % of NOMINAL
VCCIO percentage set for bank 4: +0 % of NOMINAL
VCCIO percentage set for bank 5: +0 % of NOMINAL
VCCIO percentage set for bank 6: +0 % of NOMINAL
VCCIO percentage set for bank 7: +0 % of NOMINAL

====================================================================
Preference: FREQUENCY NET "CLK_c" 100.000000 MHz ;
            48 items scored, 0 timing errors detected.
--------------------------------------------------------------------

Passed:  The following path meets requirements by 7.571ns

 Logical Details: Cell type  Pin type Cell name (clock net +/-)

   Source:         Port       Pad            d1_1
   Destination:    FF         Data in     q_reg_1  (to CLK_c +)

   Delay: 2.321ns  (41.0% logic, 59.0% route), 2 logic levels.
```

I/O Timing Report

A new feature for timing verification called the I/O Timing Report has been added to the FPGA process flow. It enables you to generate a report file to analyze timing. Specifically, for each input data port in your design, the I/O Timing Report process or the IOTIMING command-line program will generate the setup- and hold-time requirements and the minimum and maximum clock-to-out delay for every output port. By default, it analyzes the timing using the same set of temperatures and voltages and reports the worst-case I/O timing for all speed grades. Timing analysis also automatically determines the clocks and their associated data ports.

Map Register Re-Timing

The Map Register Re-timing Property is now documented fully in the FPGA Flow Help and in the Project Navigator. This property is available for LatticeECP/EC and LatticeXP devices. It moves the registers across combinational logic to balance the timing according to the tSU, tCO, or fMAX constraints in the preference (`.prf`) file. This feature is a typical logic optimization technique to balance combinational logic across register pairs to maximize fMAX clock frequency. The fMAX constraint activates re-timing around all registers. The tSU and tCO constraints may affect the retiming on I/O registers, depending on the balancing of tSU and fMAX, and tCO and fMAX.

By default, the re-timing affects PFU registers only and leaves I/O registers alone. However, you can attach the NORETIME attribute in Verilog or VHDL to I/O registers to enable re-timing or to PFU registers to disable re-timing.

Refer to the Map Register Re-timing property in the FPGA Flow Help system for more information.

IBIS Support

The ispLEVER 5.0 release supports I/O Buffer Information Specification (IBIS) models for the LatticeECP/EC and LatticeXP device families. IBIS models provide a standardized way of representing the electrical characteristics of a digital IC's pins (input, output, and I/O buffers). They are located in the *install_dir*`/cae_library/ibis` path. For more information on these models, see the “Lattice IBIS Models” topic in the ispLEVER Help system.

A conventional IBIS model is not design-specific. You can download it from the Lattice Web site. It includes I/O characteristics for all the different I/O types, as well as all possible I/O constraints like slew rate, pull, and drive strength. By running the IBIS Model process, you can obtain a design-specific IBIS model that only contains the I/O information used in your current design.

The IBIS Model process generates a design-specific IBIS model file (*project_name*.ibs). You can view this file by right-clicking the IBIS Model process and then choosing View from the popup menu.

BBOX Keyword Enhanced for New Lattice Device PGROUP Definitions

Unlike older ORCA FPGA architectures, whose programmable logic cells are identical, the new Lattice series FPGA architectures contain some logic cells in their internal matrixes that are dissimilar, such as sites dedicated to embedded block RAM or DSP blocks. The physical preference syntax for PGROUP and REGION has been altered to include BBOX keyword values PFUSIZE and DEVSIZE, which accommodate the grouping of contiguous PFUs across a dimension, ignoring dissimilar cell types in a grouping. See the "PGROUP" and "REGION" help topics in the FPGA Flow Help for complete syntax and usage information.

Heterogeneous PGROUPs

Lattice FPGAs can contain heterogeneous PGROUPs, which are PGROUP placement preferences that contain a mixture of vacant PFU site locations and EBR (embedded block RAM) and DSP (digital signal processing) sites. In older device families, all sites were identical, or homogeneous, so there was no need to have this capability.

Currently, you can mix PFU and EBR sites in a PGROUP definition. You cannot mix a DSP site with the other types of sites.

The following is an example of a heterogeneous PGROUP definition that includes both PFU component slices and EBR sites:

```
PGROUP "ebr" BBOX 2 10  DEVSIZE

COMP "rx_gearbox_regs_0/INST/ram512x64_port0/
ram512x64_syn0_0_3/ebr512x36_0"

COMP "rx_gearbox_regs_0/INST/ram512x64_port0/
ram512x64_syn0_2_1/ebr512x36_0"

COMP "rx_gearbox_regs_0/INST/ram512x64_port1/
ram512x64_syn0_2_1/ebr512x36_0"

COMP "rx_gearbox_regs_0/INST/ram512x64_port1/
ram512x64_syn0_0_3/ebr512x36_0"

COMP "SLICE_1160"
COMP "SLICE_1155"
COMP "SLICE_1154"
```

```
COMP "SLICE_1163"
COMP "SLICE_1164"
COMP "SLICE_2177"
COMP "SLICE_1157"
COMP "SLICE_1158"
COMP "SLICE_1159"
COMP "SLICE_1166";

LOCATE PGROUP "ebr" SITE "R31C25D";
```

The following example contains only EBR sites:

```
PGROUP "ebr1"  BBOX 1 4

COMP "tx_gearbox_0/INST/ram512x66_port1/ram512x66_syn0_2_1/
ebr512x36_0"

COMP "tx_gearbox_0/INST/ram512x66_port0/ram512x66_syn0_2_1/
ebr512x36_0"

COMP "tx_gearbox_0/INST/ram512x66_port1/ram512x66_syn0_0_3/
ebr512x36_0"

COMP "tx_gearbox_0/INST/ram512x66_port0/ram512x66_syn0_0_3/
ebr512x36_0";

LOCATE PGROUP "ebr1" SITE "EBR_R23C25";
```

CPLDs

This section describes the features added to Lattice's CPLD devices.

Bidirectional Open Drain (Pin Feedback) Support

This release supports pin feedback with open drain pins for ispMACH 4000, ispLSI 5000VE, ispMACH 5000B, and ispMACH 5000VG device families. To implement pin feedback, this release introduced a new source constraint, Pin_Feedback. You can specify this constraint in your ABEL design source.

The Pin_Feedback constraint is used with the Open Drain constraint to implement bidirectional signals. Bidirectional signals usually have output enable extensions. If a signal has no output enable, you can assign both Open Drain and Pin_Feedback to it. The signal can therefore be used as a bidirectional signal with the pin feedback path for the input and the open drain for the output.

For information on how to add Pin_Feedback to your source files, refer to Process Flow Help > CPLD Flow > Design Constraints > Pin_Feedback.

Fitter Report Enhancement

LVL Column in GLB_Cluster Tables A new column called LVL was added to the GLB_cluster tables in the fitter report. The LVL column lists the logic levels for signals in the specific GLB/MFB (not the worst-case logic level for the design). The HTML fitter report links the value in the LVL column to the logic equation, making it easier to follow the logic tree and see why two or three levels of logic are being implemented.

Fitter Report Number Option A new option, Fitter Report Number, was added to the Fit Design process. The Fit Design process includes a few different partition attempts. When a successful partition attempt is found, the software fits your design and displays the results in the fitter report.

If you want to view the results of the intermediate partition attempts, you can specify a number for this property. The software will then save the specified number of intermediate partition reports, if any. These reports are saved in project folders called `partition01.rpt`, `partition02.rpt`, `partition03.rpt`, and so forth. After each run, you can go to the project folder to view them in any text editor.

Note

These intermediate reports are overwritten when you start a new run.

To access the Fitter Report Number option, do the following:

1. In the Project Navigator, highlight the part name, select the **Fit Design** process, and click the right mouse button.
2. From the popup menu, select **Properties**.
3. In the Properties dialog box, highlight the **Fitter Report Number** option.
4. Click in the field next to the X at the top of the dialog box, and type in the desired number. Valid values are integers from 1 to 5.
5. Click on **Close** to apply the setting.

HDL Source Constraint COUNTER_OPT for CPLD Counter Implementation

The HDL (VHDL/Verilog) source constraint COUNTER_OPT is supported in the ispLEVER 5.0 release for CPLD counter implementation. This constraint directs the software to produce the best counter performance. You can assign this constraint to output, bidirectional, or node signals. The software optimizes these signals to provide counters with better performance.

You can add COUNTER_OPT to VHDL or Verilog source files. For detailed information, refer to Process Flow Help > CPLD Flow (ispXPLD Flow) > Design Constraints > COUNTER_OPT.

ispGDX2

The ispLEVER software for ispGDX2 devices now includes the following features.

New ispGDX2 SERDES and FIFO Design Examples

Two new design examples were added to the `example\ispgdx\ispgdx2` directory to show you how SERDES and FIFO are used.

New Global Constraints for ispGDX2/ispGDX2-E

Two new global fitting constraints are now supported by the ispGDX2/ispGDX2-E device families. You can set them in the Global Constraints sheet of the Constraint Editor.

- best_resources_usage

  This constraint defaults to No. When it is set to Yes, the software fits your design using the fewest device resources.

- implement_mux_or_implement_controlarray

  This constraint controls the implementation of the logic equations for ispGDX2/ispGDX2-E designs. If it is set to Mux, which is the default, the software first tries the multiplexer cascading method to implement logic equations. If this method fails, the software uses the control array method. If you set this constraint to Controlarray, the software first tries the control array method to implement logic equations. If this method fails, the software uses the multiplexer cascading method. This constraint is ignored if best_resources_usage is set to Yes.

Project Navigator

The ispLEVER Project Navigator has been enhanced with the new features described in this section.

New Examples for FPGA and ispGDX2 Devices

New examples have been added for the new FPGA devices, such as LatticeXP. New examples have also been added for ispGDX2 devices. You can access them by going to the examples folder in the installation directory. If you installed the software in the default path, the examples folder is under isptools. You can also go to File > Open Example to access the examples.

Renaming a Revision

The software automatically generates a name for each revision. You can change this name to better identify the specific revision. To rename a revision, right-click the revision name, choose **Rename Revision** from the popup menu, and type in the new name.

Backing Up the Current Active Revision

When you change the active revision using the **Set as Active Revision** right-click menu command, some modifications that you make to the currently active revision may be lost. A dialog box prompts you if you want to back up the currently active revision. Choose **Yes** to back it up. The backup revision is created in the revision window. If you want to restore the backup later, right-click the backup revision and choose **Restore Backup**. The backup revision is restored as the active revision.

Revision Control Defaults to Off

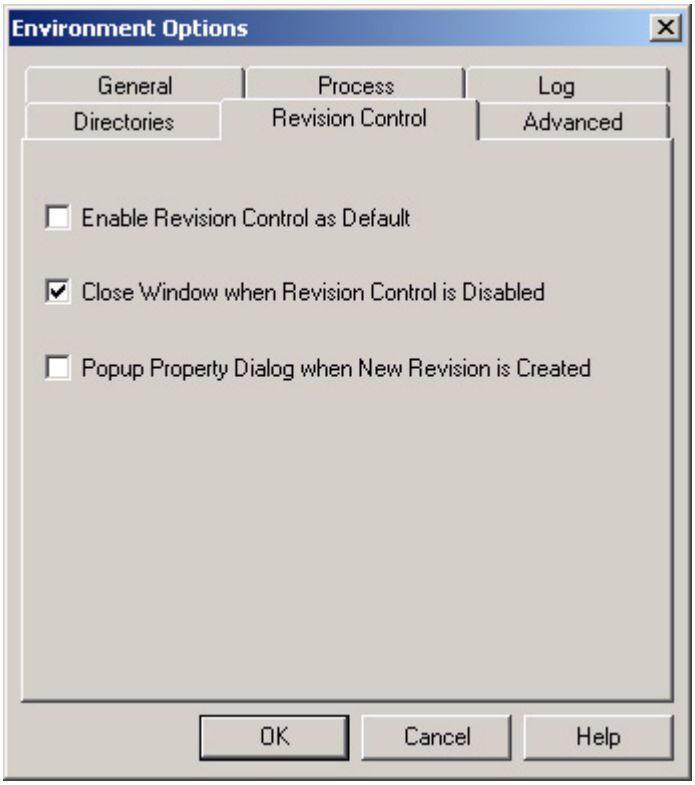
In this release, the ispLEVER software turns off revision control for every design project by default. You can manually turn it on at any time during the design process.

Displaying and Hiding the Revision Window

The newly added View > Revision Panel menu command and toolbar icon  provide you an easy way to display or hide the Revision window.

Revision Control Options

The Environment Options dialog box was re-designed to include all the revision control options in the Revision Control tab.



Autosaving Your Project

This release introduces the autosave feature in the Project Navigator. Autosave automatically saves the current design every two minutes. If you want to disable the autosave feature, choose **Options > Environment** and turn off the **Save the Design Every 2 Minutes Automatically** option.

Disabling the Recommended Device Prompt

When you open a design that targets a Lattice legacy device, a prompt dialog box pops up to suggest a replacement device for you. Now you have an option to disable this prompt. To disable the prompt, choose **Options > Environment** and turn off the **Ask to Change the Unrecommended Device when Opening a Design** option in the Advanced tab.

Importing Source Type

A new option, Use for the Remaining Files with the Same File Extension, was added to the Import Source Type dialog box. When you import multiple sources into your design and select this option, the Project Navigator applies the source type selected in this dialog box to the remaining files with the same file extension, enabling you to avoid repeatedly selecting the same source type for the same type of files.

New Environment Options

In addition to the new options previously noted, the Environment Options window, which is invoked by the Options > Environment command in the Project Navigator, has added the Precision Install Path option, located in the Directories tab.

The following options have been moved from the Advanced tab in ispLEVER 4.2 to the Revision Control tab in ispLEVER 5.0:

- Enable Revision Control as Default
- Close Window when Revision Control is Disabled
- Popup Property Dialog New Revision is Created

Ignore Preference Errors Option in ispLEVER

A new feature called Ignore Preference Errors has been added to ispLEVER 5.0. This option enables the PAR process to ignore errors in the preference file. You can set Ignore Preference Errors to true or false. When you set it to true, PAR ignores errors in the preference file and continues processing. When you set it to false, PAR terminates processing and issues an error message. The default is true.

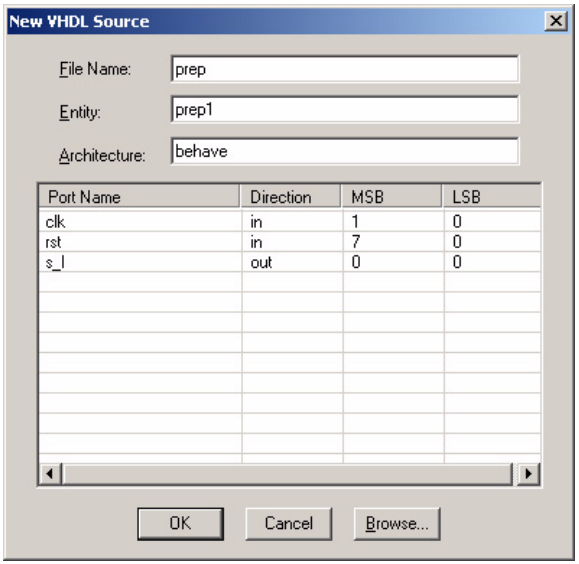
The PAR report includes the setting of the Ignore Preference Errors option and the preference errors found.

To access the Ignore Preference Errors option, do the following:

1. Highlight the part name, select the **Place and Route Design** process in the Project Navigator, and click the right mouse button.
2. From the popup menu, select **Properties**.
3. In the Properties dialog box, highlight the **Ignore Preference Errors** option.
4. Click in the field next to the X at the top of the dialog box, and select **True** or **False**.
5. Click on **Close** to apply the setting.

VHDL/Verilog Source Wizard

When you add a new VHDL or Verilog module by using the Source > New command in the Project Navigator, the Text Editor opens, along with the New VHDL Source dialog box or the New Verilog Module dialog box, respectively. You can use these dialog boxes to enter a file name, entity or module name, architecture name, and port definitions for the new source.



When you finish, click **OK**. The Text Editor opens the new file and automatically inserts a VHDL or Verilog template in it. The information that you entered in the wizard is written into the template. You can then start editing the HDL code to complete your source.

ispUPDATE Integration in Project Navigator

ispUPDATE is now integrated into the Project Navigator. You can set controls so that ispUPDATE checks for ispLEVER service pack updates when you run the ispLEVER Project Navigator. You can set this check every time you run the Project Navigator.

When you use the Auto Check feature, the ispUPDATE software notifies you whenever a new service patch has become available. The software patch is based on the ispLEVER software that you are currently using, and you receive notification when you open the Project Navigator.

To use the recommended service patch, follow this procedure:

- Click **Upgrade Now** to immediately install the service patch.

- Click **Download** to save the service patch to a directory and install it later.
- Click **Upgrade Later** if you prefer to install the service patch at a later time using the Update feature.
- To view the details of the service patch before upgrading, use the scroll bars in the Welcome window or right-click and select **Open in Web Browser**.

Documentation

The ispLEVER 5.0 release includes the following enhancements to the Lattice documentation set.

FPGA Design Guide

This release introduces the new *FPGA Design Guide*, which discusses the following aspects of designing with FPGAs:

- DSP Design Using the HDL Flow for LatticeECP-DSP FPGAs

  This chapter familiarizes you with the Digital Signal Processing (DSP) capabilities of LatticeECP-DSP devices and describes how to develop designs using the hardware description languages (HDLs).

- DSP Design with MATLAB/Simulink for LatticeECP-DSP FPGAs

  This chapter familiarizes you with the Digital Signal Processing (DSP) capabilities of LatticeECP-DSP devices and describes how to develop designs using the popular third-party tool MATLAB/Simulink.

- FPGA Design Flow for Altera Users

  If you have been an Altera device user, this chapter shows you how to start using ispLEVER to convert your designs to Lattice ispLEVER tools.

- FPGA Design Flow for Xilinx Users

  If you have been a Xilinx device user, this chapter assists you in migrating your designs to equivalent Lattice designs with emphasis on the conversion of Spartan-3 devices to LatticeEC devices. It also introduces you to the Lattice software interface and design flow, helping you to transition to Lattice tools.

- HDL Synthesis Coding Guidelines

  This chapter describes coding guidelines for HDL, using various design methodologies to successfully implement attributes in your designs.

- Successful Placement and Routing

In a straightforward seven-step process, this chapter teaches you how to use preferences, PAR settings, timing analysis, iterative processes, and floorplanning to achieve timing closure.

- Logic Analysis and Debugging Cores

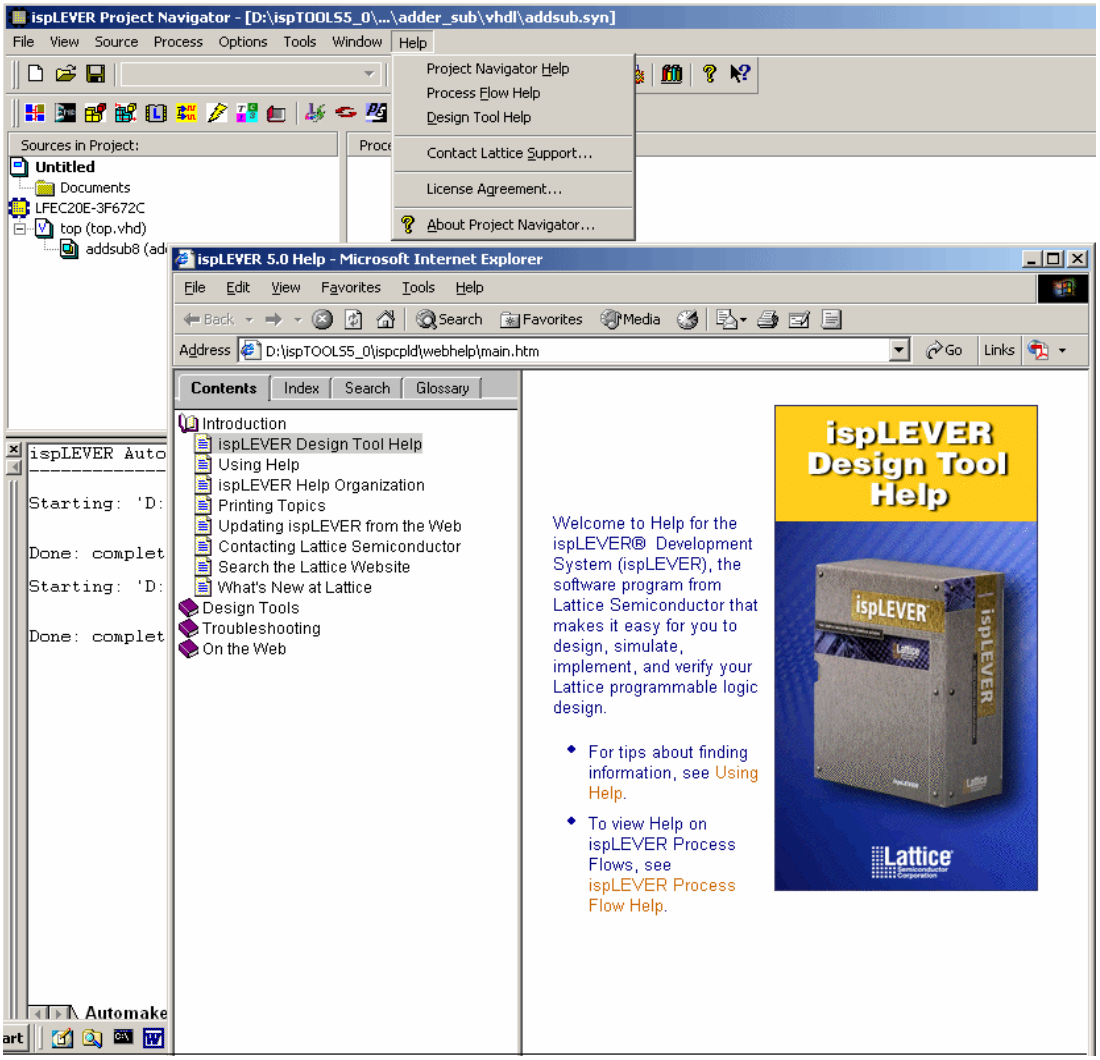
  This chapter provides explanatory information on core generation and logic analysis, then shows you in step-by-step fashion how to use the ispTRACY IP Manager to generate an ispTRACY core and integrate the core into the design. It then shows you how to use the core to perform logic analysis with the ispTRACY Logic Analyzer.

Improved Online Help and Search Capability

The ispLEVER online help has been reorganized, and the help search capability has been improved. You can quickly find help on process flows by choosing **Help > Process Flow Help** or on any ispLEVER tool by choosing **Help > Design Tools Hel**p.

As before, you can find help on any dialog box by clicking the Help button in the dialog box or by pressing F1.

In addition, you will find conveniently placed “Search the Lattice Web Site” sections throughout the online Help. These sections allow you to type in keywords and search for information on the Lattice Semiconductor corporate Web site (www.latticesemi.com). An Internet connection is required to use the “Search the Lattice Web Site” feature.



Error Messages Linked to Online Help

Error messages are now linked to online help that enables you to understand the message, determine what actions to take to resolve the error, and access information that is relevant to the task you were performing when the error message was issued.

Integration of ispLEVER Online Help into Corporate Web Site

The ispLEVER online help has been redesigned for integration into the Lattice Semiconductor corporate Web site (www.latticesemi.com), providing a seamless link between the software and pertinent documentation, such as data sheets, technical notes, and application notes. This integrated help gives you a powerful tool to quickly access the entire library of information available from Lattice.

I/O Assistant Design Step Guide

The *I/O Assistant Design Step Guide* describes the process, usage, and benefits of using I/O Assistant design methodology.

New Programming and Logic Analysis Tutorial

The new *Programming and Logic Analysis Tutorial* guides you through the process of using the ispTRACY IP Manager and ispTRACY Logic Analyzer applications in ispLEVER. The ispTRACY IP Manager adds internal logic analysis and trace buffer logic to your design as part of a functional verification strategy. The ispTRACY Logic Analyzer communicates with the cores, enabling you to perform a complete logic analysis of your design.

The tutorial helps you to understand the basic design flow, processes, and data files involved in incorporating an ispTRACY core into your design. It describes the two distinct design flows possible to integrate an ispTRACY core: RTL instantiation or EDIF netlist. It goes on to show you how to define the basic trigger logic and trace buffer dimensions for an internal logic analysis, link the internal ispTRACY logic analysis core interface to trigger and trace signals, program the standard LatticeEC board, and examine the internal signals using the ispTRACY Logic Analyzer waveform display. In addition, you learn what additional resources are required to add ispTRACY cores to your design.

Command-Line Scripting in Online Help

The documentation of command-line scripting in the process flow online help has been expanded to include more examples and instructions on how to use core FPGA implementation tools to develop scripts and command files that run repetitive tasks or long processes.

FPGA Floorplanner Online Help

The new FPGA Floorplanner online help describes each aspect of the new Floorplanner graphical user interface, including new concepts, such as `PFUSIZE` and `DEVSIZE`. It provides ample cross-references to related attribute and preference concepts.

New Online Help on Meeting Timing Requirements for CPLDs

New online help has been written on controlling timing for CPLD designs. It shows you how to define the maximum frequency and pin-to-pin delay requirements for your CPLD designs.

Updated HTML Help for MATLAB/Simulink R14

The Lattice-specific HTML help for Lattice blocksets has been updated to be compatible with updated MATLAB/Simulink R14 software. It enables you to obtain help on Lattice blocksets while you are in the newest MATLAB/Simulink environment.

Other

This section lists the remaining features added to the ispLEVER 5.0 software.

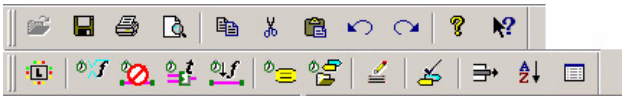
Constraint Editor/Preference Editor/Optimization Constraint Editor

The Constraint Editor, Preference Editor, and Optimization Constraint Editor have been enhanced by the features noted in this section.

Enhanced Context-Sensitive Help The context-sensitive help feature was enhanced in the Constraint Editor, Preference Editor, and Optimization Constraint Editor. You can highlight any constraint and press F1 to view the relevant help information about that constraint.

Help Information in Dialog Boxes Some help information is now displayed at the top of many dialog boxes in the Constraint Editor and Preference Editor. It enables you to learn the purpose of the dialog box without clicking the Help button.

Enhanced Toolbars in the Preference Editor The Preference Editor toolbar is now divided into two bars. The standard toolbar provides quick mouse access to some common functions like Open, Print, Cut, and Paste. Under the standard toolbar, the other toolbar includes icons specific for the Preference Editor.



ispVM System 15.0.1

This installation of ispLEVER 5.0 includes ispVM System 15.0.1, which provides programming support for LatticeXP devices and offers other features and enhancements. You can find details in the readme file included with the ispVM System installation.

Synplify 8.0

Synplicity Synplify 8.0, which you can invoke from ispLEVER 5.0, has better LUT utilization and maximum frequency than version 7.7.

Known Issues and Solutions

Project Navigator

Map and Place & Route TRACE Report Processes Issue Error Message

When you run the Map TRACE Report process and the Place & Route TRACE Report process in the Project Navigator, you will see the following error message in the Automake.log:

```
ERROR - trce: Unable to open command file "prep1.mt"
```

Devices affected: LatticeECP/EC, LatticeXP, ORCA families and FPSC

Ignore this message. It has no effect on the trace results.

Designs with FIXEDDELAY Fail in Map Process

The `FIXEDDELAY` attribute in the VHDL or Verilog file can only be applied to input signals of input registers. By default, Synplify no longer infers input registers, so when you use Synplify with a VHDL or Verilog file containing the `FIXEDDELAY` attribute, the Map Process issues an error message.

Devices affected: LatticeECP/EC, LatticeXP

For the `FIXEDDELAY` attribute to work with Synplify, you must add the `SYN_USEIOFF` attribute to the VHDL or Verilog file to infer I/O registers.

ARRAY_SIZE FPGA Attribute Topic

The ARRAY_SIZE FPGA attribute topic is currently unavailable in the ispLEVER help system. ARRAY_SIZE is an attribute used to specify an array size for a memory element. The attribute can take a numerical value or the “NOT USED” value.

Devices affected: LatticeECP/EC, LatticeXPYou can obtain more information on this topic by contacting Lattice Technical Support.

Multiple Linked Libraries Not Supported

Multiple linked libraries are not supported when a library references another library.

Devices affected: LatticeECP

Modify your design to ensure that libraries do not refer to another library.

Synthesis and VHDL Simulation

I/O Assistant Flow Does Not Work with Precision RTL

The I/O Assistant flow does not work with the Precision RTL synthesis tool.

Devices affected: LatticeECP/EC, LatticeXPUse Synplicity Synplify or Mentor Graphics Precision RTL instead.

Synplify Reports Multiple-Drive Error

If you use a 11 x 2 or 15 x 2 PFU multiplier in your design, Synplify reports a multiple-drive error.

Devices affected: LatticeECP/EC, LatticeXPUse a 2 x 11 or 2 x 15 PFU multiplier instead.

Precision RTL Incorrectly Converts Initialization Value

If an EBR is instantiated in the Verilog design input to Precision RTL and the EBR block contains memory initialization strings and the memory module definition is included in the design, Precision RTL incorrectly translates the initialization value into signed decimal values.

For example, suppose that a design contains the PDP8KA cell of a LatticeEC EBR cell:

```
320'h00000000000000000000000000000000000000000000000000
```

```
00000000000000000156331C6F001E000AAAA;
defparam m0RamBaseBlockInst0.INITVAL_01 =
```

Precision RTL processes the design without errors. But if PDP8KA has been redefined and included in the project, Precision RTL incorrectly translates the initialization value.

Devices affected: LatticeECP/EC, LatticeXP

Do not include ecp.v, ec.v, or xp.v in the Precision RTL project. Alternatively, you can redeclare the modules and include them in the design. In the example just given, you could redeclare the PDP8KA, DP8KA, and DP8KA modules and include them in the design.

Retiming Switch in Precision RTL Causes Simulation to Fail

When the retiming switch is turned on in Precision RTL, in some cases the logic connected to the primary I/O floats, so the simulation fails.

Devices affected: LatticeECP/EC, LatticeXP

Do not turn on the retiming in Precision RTL.

Precision RTL Does Not Run from Command Line or Project Navigator

On some machines, Precision RTL does not run from the command line or the ispLEVER Project Navigator and issues the following error messages:

```
Error: Unable to open file: ''.
Error: Unable to open file: 'precisionblks.ini'.
Error: Unable to open file: '.precision.ini'.
Error: invalid command name "MGS_Core::app_initialize"
```

Devices affected: all devices

Set the MGC_HOME environment variable to `$isptools5_0/precision`.

Inferring GSR in LeonardoSpectrum Produces Logic Errors

Inferring the GSR in LeonardoSpectrum sometimes produces logic errors on the polarity of the reset.

Devices affected: LatticeECP/EC, LatticeXP

To turn off the GSR inference, add the following command in the *design_tcl*.tcl script for LeonardoSpectrum:

```
set infer_gsr false
```

Floorplanner

Floorplanner Needs Internet Access

If you have a local software firewall on your machine and you try to invoke the Floorplanner, you will see a message stating that this *progam_name* is attempting to access the Internet. This message is caused by the IPC (inter-process communication) function used in these applications and the way the local software firewall is configured.

Devices affected: FPGA, ispXPGA

Configure the firewall so that the following executables are granted access automatically: `flmainapp.exe`, `flmainappw.exe`, `flmain_la.exe`, `prfEdit.exe`, `javaw.exe`.

Preference Editor

Preference Editor Needs Internet Access

If you have a local software firewall on your machine and you try to invoke the Preference Editor, you will see a message stating that this *progam_name* is attempting to access the Internet. This message is caused by the IPC (inter-process communication) function used in these applications and the way the local software firewall is configured.

Devices affected: FPGA, ispXPGA

Configure the firewall so that the following executables are granted access automatically: `flmainapp.exe`, `flmainappw.exe`, `flmain_la.exe`, `prfEdit.exe`, `javaw.exe`.

Module/IP Manager

Module/IP Manager Fails to Create Multiplier

The multiplication function fails in the Module/IP Manager.

Devices affected: LatticeECP/EC, LatticeXP

When one operand is constant, make sure the bit size is the same for the constant and for the other operand.

Module/IP Manager LPC Files Generated for Modules or IP in 4.2 Cannot Be Imported into 5.0

The Module/IP Manager Lattice Parameter Configuration (LPC) files generated in ispLEVER version 4.2 cannot be imported into ispLEVER 5.0 because the module parameters have changed.

Devices affected: LatticeECP/EC, LatticeXP

Regenerate the module in ispLEVER 5.0 Module/IP Manager.

Absolute Values Must Be Used for FIFO Flags in Module/IP Manager

In the Module/IP Manager, the FIFO Almost Full and Almost Empty flags must be specified in absolute values. In previous releases, you could use values relative to the size of the FIFO for the Almost Full flag.

Devices affected: LatticeECP/EC, LatticeXP

Dynamic Sign Signal Input Is Not Supported with DSP Modules

The Module/IP Manager block diagrams shown with DSP modules MAC, MULT, MULTADDSUM, and MULTADDSUMSUB show a “dynamic sign” signal input. Currently this feature is not supported by ispLEVER. The operation of the module is static and is configured to be signed or unsigned according to the Operation option. For more information on sysDSP modules and configuration, see “LatticeECP-DSP sysDSP Usage Guide,” TN1057.

Devices affected: LatticeECP-DSP

IBIS Model

PULLMODE Setting Generates Warning Message in IBIS Model

When you generate IBIS models for inputs and outputs with PULLMODE set to “None,” the software issues the following message:

```
Warning - IBIS model not available.
```

Devices affected: LatticeECP/EC, LatticeXP

These models are missing in the master IBIS file. Contact Lattice Technical Support to request them.

Place and Route Design Process

PAR May Violate PGROUP BBOX Specifications

The Place and Route Design process may violate heterogeneous (PFU/PFF and EBR) PGROUP BBOX specifications. This issue is specific to EBR placement where an irregularly placed EBR row, such as the topmost EBR row in some devices, is used.

Devices affected: LatticeECP/EC, LatticeXP

Use other possible EBR rows on the device.

ispTRACY

ispTRACY Core Requires Synplify Synthesis Tool

Currently, if you choose LeonardoSpectrum or Precision RTL as your synthesis tool, you must also install the Synplify synthesis tool for the ispTRACY core. ispTRACY cannot run if Synplify is not installed.

Devices affected: LatticeECP/EC, LatticeXP, ispXPGA

This issue has no workaround.

Unsupported VHDL Features in ispTRACY IP Manager

Some features that are valid in the VHDL language are not supported in the ispTRACY IP Manager Core Linker.

- Array types of two or more dimensions will not be shown in the port or node section.
- Component instances instantiated in the following statements will not be shown in the hierarchical design tree:
  - Generate statement
  - Conditional statement, such as an if-then-else statement
  - Selection statement, such as a case statement
- If function calls are used in the array declaration, the actual size of the array will be unknown to the Core Linker.
- Entity and architecture of the same design cannot be in different files.

Devices affected: ispXPGA, LatticeECP/EC

This issue has no workaround.

Connecting VHDL Signals to ispTRACY Core

The types of inputs and outputs used in the ispTRACY IP Manager core template restrict the types of signals or ports that can be used in VHDL designs to connect to the ispTRACY IP core.

Devices affected: ispXPGA, LatticeECP/EC, LatticeXP

In VHDL designs, use only `std_logic_vector` and `std_logic` for the types of signals or ports or their array to connect to the ispTRACY IP core.

MATLAB/Simulink

Longer Simulation Time Needed to Propagate Datatypes

A simulation mismatch may result if the datatypes have not been propagated through the design with sufficient simulation time. A warning message appears if the system detects that all datatypes have not been resolved through simulation.

Devices affected: LatticeECP-DSP

Increase your simulation sample times.

Simulation Mismatch Occurs When Downsample Block Drives Parallel-to-Serial Block

A simulation mismatch may result if you drive a parallel-to-serial block with a downsample block.

Devices affected: LatticeECP-DSP

This issue has no workaround.

Simulink Block Supports More Single-Port RAM Data Widths Than Hardware Does

A Simulink block supports more single-port RAM data widths than the hardware does.

Devices affected: ECP-DSP

When setting port widths for the single-port RAM block, use only multiple data widths of 9, that is, x9, x18, and x36. Failure to use these settings will result in a `module generator failed` error when you generate the netlist.

Device Support

RSDS Fuse Setting Incorrect

The RSDS fuse setting is incorrect.

Devices affected: LatticeECP/EC

Use LVDS25E to implement the RSDS standard.

LVDS25 Not Supported as Bidirectional I/O

The LVDS25 is not supported as a bidirectional I/O.

Devices affected: LatticeECP/EC, LatticeXP

Do not use the LVDS25 as a bidirectional I/O.

PULLMODE Fuses Incorrect When PCICLAMP On

PULLMODE fuses set to UP or KEEPER are not correct when PCICLAMP is set to ON.

Devices affected: LatticeECP/EC, LatticeXP

Do not use PULLMODE and PCICLAMP simultaneously.

Documentation

Disabled Hyperlinks in a Few FPGA Flow Help Topics

A few topics in the FPGA Flow Help contain disabled hyperlinks. These hyperlinks cross-reference other HTML files in the `<install_dir>/ispcpld/webhelp/mergedProjects` path, either concerning options that can be set for various FPGA flow processes in the Project Navigator Help system or for interlinking between Design Tool help systems.

If you encounter these disabled hyperlinks, you can also access the linked information in the appropriate help system in the path just given. Options or “properties” for the FPGA processes are documented in the Project Navigator Help and are readily accessible from the dialog box Help buttons or by clicking specific properties in the dialog box and pressing the F1 key.

The following topics in FPGA Flow Help contain certain links that do not access their target files:

- Schematic Design Entry
- I/O Assistant Design Overview
- Clock Boosting Options
- Place and Route Options
- Timing Driven Place & Route