Lattice Sentry I2C Monitor IP

IP Version: v1.1.0

User Guide

FPGA-IPUG-02108-1.1

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Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
APB	Advanced Peripheral Bus
FPGA	Field-Programmable Gate Array
I2C	Inter-Integrated Circuit
RTL	Register Transfer Language

1. Introduction

The Lattice Semiconductor Sentry™ I2C Monitor IP for MachXO3D™ and MachXO4™ monitors the traffic on the I2C bus to identify potential illegal traffic based on a pre-defined library. Once illegal traffic is detected, this IP informs the host through the status flag and/or interrupt. With user option, the current communication is disrupted by disabling the I2C bus.

The design is implemented in Verilog HDL. It can be configured and generated using Lattice Propel™ Builder. It targets MachXO3D and MachXO4 FPGA devices and can be implemented using the Place and Route tool in Lattice Diamond™ or Lattice Radiant™ software, integrated with the Synplify Pro® synthesis tool.

1.1. Features

The key features of the I2C Monitor IP include:

- Monitoring of traffic on an I2C bus for illegal activity based on programmable filter conditions
- Support for AMBA 3 APB Protocol v1.0 for CPU access

1.2. Conventions

1.2.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.2.2. Signal Names

Signal names that end with:

- *_n* are active low (asserted when value is logic 0)
- *_i* are input signals
- *_o* are output signals
- *_io* are bi-directional input/output signals

1.2.3. Host

The logic unit inside the FPGA interacts with the I2C Monitor IP through APB.

1.2.4. Attribute Names

Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

2. Functional Description

2.1. Overview

The I2C Monitor IP monitors the I2C bus traffic and compares the first eight bytes of traffic immediately after the target I2C address with the pre-defined filters in the database. The filters are set up by the system host through the APB Bus. Once a matching event is detected, it informs the host using status sampling through the APB Bus or dedicated interrupt. Meanwhile, according to user setup, it disables the current I2C communication to prevent catastrophic damage to the system.

The block diagram of the I2C Monitor IP is shown in Figure 2.1.

2.2. Block Diagram

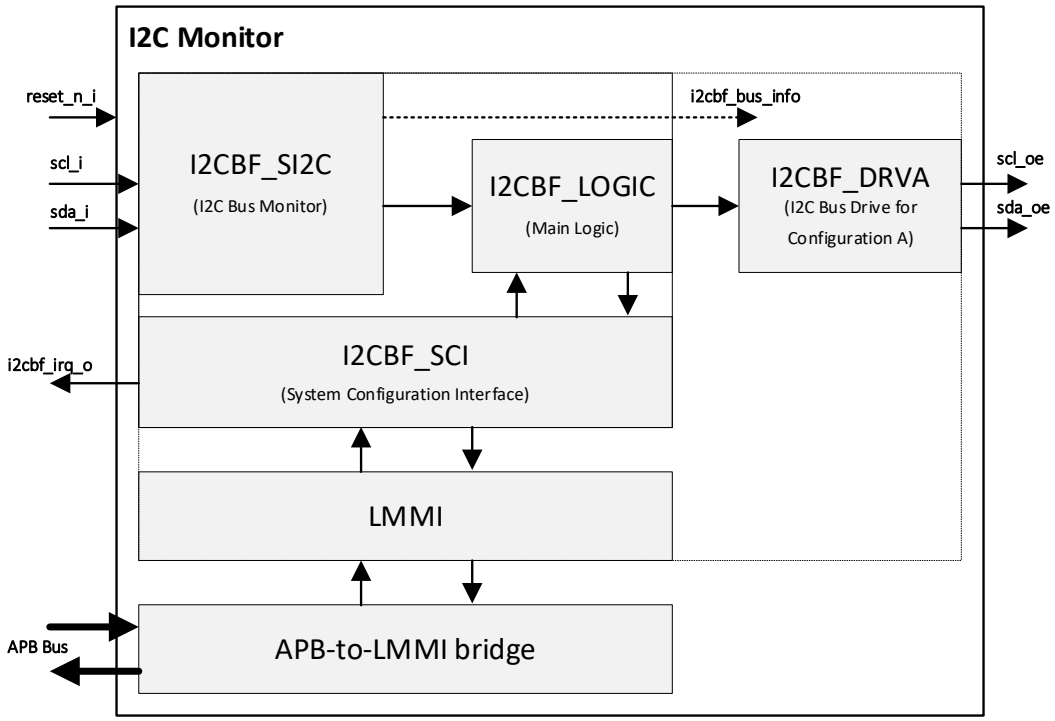

Figure 2.1. I2C Monitor IP Block Diagram

2.3. Signal Description

Table 2.1. I2C Monitor Signal Description

Port	Width	Direction	Description
System			
clk_i	1	In	Clock for APB and LMMI logic
reset_n_i	1	In	System Asynchronous Reset Active-low
i2cbf_irq_o	1	Out	I2C Monitor Event Detected Interrupt
i2cbf_sr_o	8	Out	I2C Monitor Status Register
i2cbf_cs_i	1	In	Chip select for I2C Monitor
APB			
apb_psel_i	1	In	Select signal Indicates that the completer device is selected and a data transfer is required.
apb_paddr_i	32	In	Address signal
apb_pwdata_i	32	In	Write data signal
apb_pwrite_i	1	In	Direction signal Write = 1, Read = 0
apb_penable_i	1	In	Enable signal Indicates the second and subsequent cycles of an APB transfer.
apb_pready_o	1	Out	Ready signal Indicates transfer completion. Completer uses this signal to extend an APB transfer.
apb_prdata_o	32	Out	Read data signal
apb_pslverr_o	1	Out	APB error signal The APB error signal is not supported in this IP. It is permanently tied to logic low (0), indicating that error signaling through the APB interface is not implemented.
I2C Bus Interface			
scl_i	1	In	SCL Clock Input for I2C Bus
sda_i	1	In	SDA Data Input for I2C Bus
scl_oe	1	Out	SCL Output Enable to Disable SCL
sda_oe	1	Out	SDA Output Enable to Disable SDA

2.4. Attribute Summary

The I2C Monitor has no RTL parameters for configuring the IP at instantiation time.

2.5. Register Description

The register address map specifies the available I2C Monitor IP core registers and which are accessible through APB.

Table 2.2. Summary of I2C Monitor IP Core Registers

Offset	Register Name	Access	Default value	Description
0x1FC	I2CBF_CR	R/W	32'H00000000	Control Register • Bit [31:8]: Unused • Bit [7]: i2cbf_en – This bit enables the I2CBF IP to perform the I2C bus traffic event detection. • Bit [6]: bus_stop – If asserted, this bit allows the host to unconditionally disable the I2C bus by driving both SCL and SDA low. The bus is released after this bit is written with 0. • Bit [5]: bus_dis_en – This bit enables the I2CBF IP to disable the I2C bus in case an event is detected. • Bit [4:0]: total_number_of_entry These five bits allow the host to inform the I2CBF IP of the number entries defined for the event detection. The current maximum number is 20.
0x1F8	I2CBF_INTENR	R/W	32'H00000000	Interrupt Enable Register • Bit [31:8]: Unused • Bit[7:6]: Reserved Bit[5]: int_en – This bit enables the interrupt from the I2CBF IP to the system host in case an I2C traffic event is detected. • Bit [4:0]: Reserved
0x1F4	I2CBF_INTSETR	R/W	32'H00000000	Interrupt Set Register • Bit [31:8]: Unused • Bit[7:6]: Reserved Bit[5]: int_set – This bit enables the interrupt from the I2CBF IP to the system host in case an I2C traffic event is detected. • Bit [4:0]: Reserved
0x1F0	I2CBF_SR	R	32'H00000000	Status Register • Bit [31:8]: Unused • Bit [7:6]: Reserved • Bit [5]: event_detected – This bit indicates that there is an event detected from the I2C bus traffic based on the entry table setup. • Bit [4:0]: entry_number_for_current_event These four bits indicate the entry number for the current event. It will be stable once an event is detected until the I2CBF IP is reset by the host.
0x140	Reserved	—	—	—

Offset	Register Name	Access	Default value	Description
0x13C	ENTRY20_D	R/W	32'H00000000	ENTRY 20 [127:96] • Bit [31]: entry_enable – This bit enables this particular entry for the event detection. • Bit [30]: 10_bits_address – This bit enables the 10 bits address for I2C target address checking. • Bit [29:27]: i2c_10_bits_address_msb – These bits are the MSB 3 bits of the 10 bits address if the bit [126] is set. • Bit [26:20]: 7_bits_address – These bits are the I2C Target Address for I2C bus traffic checking. • Bit [19]: rw – This bit is the RW checking bit for I2C bus traffic monitoring. The same as the I2C Bus Specification, 1 is for read and 0 for write. • Bit [18]: rw_nc – This bit is used to disable the RW bit checking. Once set, the RW bit is ignored for I2C bus traffic checking, hence, both I2C bus read and write are monitored. • Bit [17:16]: check_mode – These two bits are used to set up the checking mode for this entry. The provided modes are shown in Table 2.3. • Bit [15:8]: detection_enable_mask – These eight bits are the active High Mask to enable corresponding received byte(s) among the eight bytes immediately after the I2C target address for event detection. • Bit [7:0]: bit_wide_operation_selection_mask – These eight bits are the active High Mask to alter corresponding byte event detection from pattern matching to bit detection against the corresponding Check Data Byte. See the detailed format in Table 2.4.
0x138	ENTRY20_C	R/W	32'H00000000	ENTRY 20 [95:64] Bit [31:0]: check_data_mask_byte – These four bytes are the checking data for the event detection or Bit Mask bytes depending on the entry check mode setup. For Mode 00 and Mode 01, these four bytes serve as Bit Mask bytes for bitwise checking selection. The mask bytes order corresponds to the position of the SET bit (1) within the Bit-Wide Operation Selection Mask (Entry Bit [103:96]). The larger mask number index corresponds to the MSB side of the Bit-Wide Operation Selection Mask. A maximum of four Bit Mask bytes can be selectively enabled per entry. For Mode 10 and Mode 11, these four bytes are part of the check data bytes (total of 12 bytes). See the detailed format in Table 2.4.
0x134	ENTRY20_B	R/W	32'H00000000	ENTRY20 [63:32] Bit [31:0]: check_data_byte – These first four bytes of data are the checking data for the event detection. See the detailed format in Table 2.4.
0x130	ENTRY20_A	R/W	32'H00000000	ENTRY20 [31:0] Bit [31:0]: check_data_byte – These next four bytes of data are the checking data for the event detection. See the detailed format in Table 2.4.

Offset	Register Name	Access	Default value	Description
0x12C	ENTRY19_D	R/W	32'H00000000	Refer to Entry20 Register
0x128	ENTRY19_C	R/W	32'H00000000	Refer to Entry20 Register
0x124	ENTRY19_B	R/W	32'H00000000	Refer to Entry20 Register
0x120	ENTRY19_A	R/W	32'H00000000	Refer to Entry20 Register
—	—	—	—	ENTRY2_A – ENTRY18_D Refer to Entry20 Register
—	—	—	—	
—	—	—	—	
—	—	—	—	
0x0C	ENTRY1_D	R/W	32'H00000000	Refer to Entry20 Register
0x08	ENTRY1_C	R/W	32'H00000000	Refer to Entry20 Register
0x04	ENTRY1_B	R/W	32'H00000000	Refer to Entry20 Register
0x00	ENTRY1_A	R/W	32'H00000000	Refer to Entry20 Register

Table 2.3. Check Mode Table

Check Mode	Description	Detection Enable Mask	Bit-Wide Operation Selection Mask	Data Byte Utilized
2'b00 Check Mode 1	• Multiple byte checking against Data Byte 1–8 based on the Detection Enable Mask and Bit-Wide Operation Selection Mask setting • Event trigger by ALL enabled bytes matching to the corresponding receiving bytes	Utilized, Multiple Hot	Utilized, Max 4 Hot	Data Byte 1–8 Bit Mask 1–4
2'b01 Check Mode 2	• Multiple byte checking against Data Byte 1–8 based on the Detection Enable Mask and Bit-Wide Operation Selection Mask setting • Event trigger by ANY enabled bytes matching to the corresponding receiving bytes	Utilized, Multiple Hot	Utilized, Max 4 Hot	Data Byte 1–8 Bit Mask 1–4
2'b10 Check Mode 3	• Single byte checking against entry Data Byte 1–12, based on the Detection Enable Mask setting • Event is triggered if the specified receiving byte DOES NOT match any byte among the entry Data Byte 1–12.	Utilized, One Hot	—	Data Byte 1–12
2'b11 Check Mode 4	• Single byte checking against the entry Data Byte 1–12 based on the Detection Enable Mask Setting. • Event is triggered if the specified receiving byte DOES match one of the entry Data Byte 1–12.	Utilized, One Hot	—	Data Byte 1–12

Each Entry Data is 128 bits in length, which matches the data frame size of the MachXO2™, MachXO3™ and MachXO4 devices UFM (User Flash Memory). The field's assignments for each I2C Monitor Entry Data is shown Table 2.4. The APB host, through the 32 bits APB Bus, can read/write this True Dual Port memory.

Table 2.4. Data Entry Format

Bits	**127**	**126**	**125**	**124**	**123**	**122**	**121**	**120**	**119**	**118**	**117**	**116**	**115**	**114**	**113**	**112**
Name	Entry Enable	10 Bits Address	10 Bits Address MSB			I2C 7 Bits Address							RW	RW NC	Check Mode	
Bits	**111**	**110**	**109**	**108**	**107**	**106**	**105**	**104**	**103**	**102**	**101**	**100**	**99**	**98**	**97**	**96**
Name	Detection Enable Mask								Bit-Wide Operation Selection Mask							
Bits	**95**	**94**	**93**	**92**	**91**	**90**	**89**	**88**	**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**
Name	Check Data Byte 12 / Bit Mask 4								Check Data Byte 11 / Bit Mask 3							
Bits	**79**	**78**	**77**	**76**	**75**	**74**	**73**	**72**	**71**	**70**	**69**	**68**	**67**	**66**	**65**	**64**
Name	Check Data Byte 10 / Bit Mask 2								Check Data Byte 9 / Bit Mask 1							
Bits	**63**	**62**	**61**	**60**	**59**	**58**	**57**	**56**	**55**	**54**	**53**	**52**	**51**	**50**	**49**	**48**
Name	Check Data Byte 8								Check Data Byte 7							
Bits	**47**	**46**	**45**	**44**	**43**	**42**	**41**	**40**	**39**	**38**	**37**	**36**	**35**	**34**	**33**	**32**
Name	Check Data Byte 6								Check Data Byte 5							
Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Check Data Byte 4								Check Data Byte 3							
Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Check Data Byte 2								Check Data Byte 1							

The behavior of registers to write and read access is defined by its access type, which is detailed in Table 2.5.

Table 2.5. Access Type Definition

Access Type	**Behavior on Read Access**	**Behavior on Write Access**
RO	Returns register value	Ignores write access
WO	Returns 0	Updates register value
RW	Returns register value	Updates register value
RW1C	Returns register value	Writing 1'b1 on register bit clears the bit to 1'b0. Writing 1'b0 on register bit is ignored.
RSVD	Returns 0	Ignores write access

2.6. Module Description

2.6.1. I2CBF_SCI

I2CBF_SCI is the System Configuration Interface for the I2C Monitor IP, which contains the configurable memory for the IP. The system host can access this memory through the 32 bits LMMI bus. The memory/registers are:

- Control register, read and write access.
- Status register, read-only.
- True Dual Port memory (EBR) for the entry data for event detection, which can be read/written by the host through the 32-bit LMMI bus, and read by the I2CBF_LOGIC through the 128-bit internal data bus.

2.6.2. I2CBF_SI2C

The I2CBF_SI2C module monitors the I2C bus activities, detects the START/STOP conditions, examines the I2C target address, and fetches the first eight data bytes. It provides the received address, RW bits, received data bytes along with the data byte count number to the I2CBF_LOGIC module for event detection. Also, for some application scenarios, it can provide the receiving bit count and acknowledge information to I2CBF_DRVX block for I2C bus disable control.

2.6.3. I2CBF_LOGIC

The I2CBF_LOGIC module gets the current I2C bus activities from the I2CBF_SI2C module and the entry data from the I2CBF_SCI module. It then performs event detection based on the control register and entry data settings for every data byte received from the I2C bus traffic. Once an event is detected, it sets up corresponding status register bit and sends out interrupt to the host if control register setting allows.

2.6.4. I2CBF_DRVA

This I2CBF_DRVA module is controlled by the output of the I2CBF_LOGIC module to disable the I2C bus by driving both SCL and SDA low. This disrupts the I2C communication. Once the I2C bus is disabled, it could only be released by writing to the status register of the I2C Monitor IP from the host or by cycling the power supply. To only disrupt the I2C communication on the target side without disabling the whole I2C bus, a different module, such as I2CBF_DRVB with bus multiplexer, can be deployed to replace the I2CBF_DRVA module.

2.6.5. APB-to-LMMI

The APB-to-LMMI is an APB completer to LMMI controller interface bridge.

2.7. Programming Flow

During the system initialization phase, the system host should download the Entry Table for the I2C Monitor IP from the non-volatile UFM into the True Dual Port Memory (EBR) inside the I2CBF_SCI block through the APB bus. To start the I2C bus monitoring process, the host should write the I2CBF_CR through the APB bus with the I2CBF_EN bit set to 1. The host should receive interrupt if an event is detected, if the INT_EN bit is set inside I2CBF_CR, or the host has to pull the I2CBF_SR to identify the I2C bus status.

If the BUS_DIS_EN bit inside the I2CBF_CR is set, the I2C bus is disabled for further communication between controller and target. To resume the I2C bus communication, the host should perform a write operation to the I2CBF_SR through the Wishbone bus.

To stop I2C bus monitoring, the host should write the I2CBF_CR with the I2CBF_EN bit set to 0.

2.7.1. Example Data Alignment for Check Modes 1 and 2

For Check Mode 1 and Check Mode 2, the I2C Monitor checks every time a new byte (for the first eight bytes immediately after the I2C Target Address) is received for all available entries. For each entry, the Data and Mask alignment is demonstrated in Figure 2.2 below.

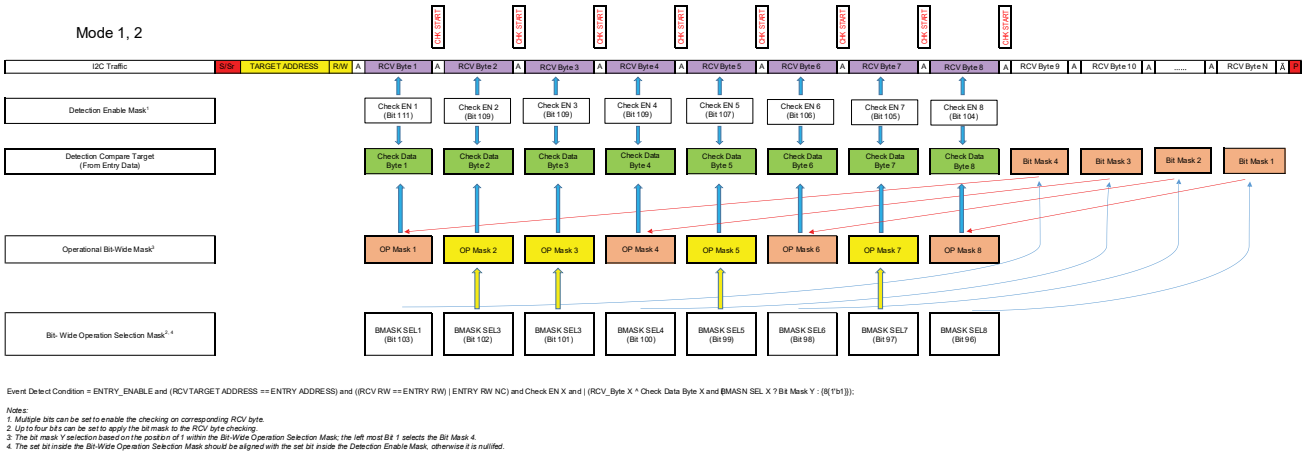

Figure 2.2. Check Mode 1, 2 Data Alignment

2.7.2. Example Data Alignment for Check Modes 3 and 4

For Check Mode 3 and Check Mode 4, the I2C Monitor checks every time a new byte (for the first eight bytes immediately after the I2C Target Address) is received for all available entries. However, the data arrangement is different. For each entry, the data alignment in Check Mode 3 and Check Mode 4 are demonstrated in Figure 2.3.

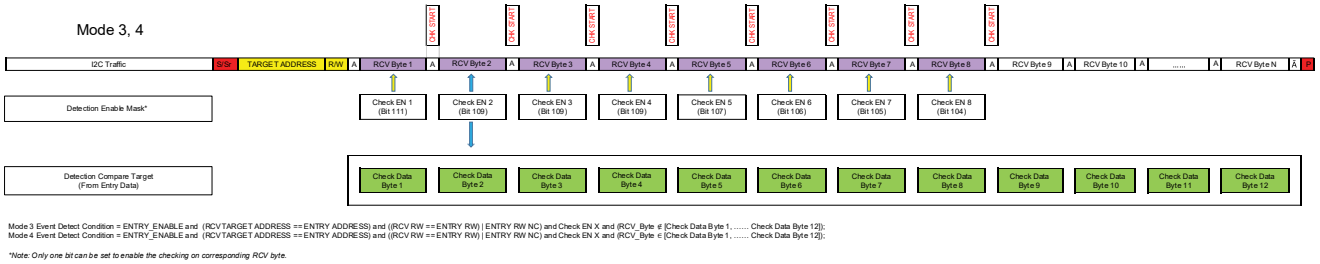

Figure 2.3. Check Mode 3, 4 Data Alignment

3. Licensing and Ordering Information

The Lattice Sentry I2C Monitor IP is provided at no additional cost with the Lattice Diamond and Radiant software.

Appendix A. Resource Utilization

Table A.1. Resource Utilization

FPGA Resource Utilization	Registers	LUTs	EBRs	Target Device	Synthesis Tools
Number of resource	399	541	1	MachXO3D	Synopsys Synplify Pro N-2018.03L-SP1-1
Number of resource	401	621	1	MachXO4	Synopsys Synplify Pro W-2025.03LR-SP1-Beta1

References

- Lattice Sentry I2C Monitor IP Release Notes (FPGA-RN-02082)
- MachXO3D web page
- MachXO4 web page
- Lattice Sentry I2C Monitor IP Core
- Lattice Diamond Software web page
- Lattice Propel Design Environment web page
- Lattice Radiant Software web page
- Lattice Sentry Solutions Stack web page
- Lattice Solutions IP Cores web page
- Lattice Solutions Reference Designs web page
- Lattice Insights web page for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Note: In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

Revision 1.1, IP v1.1.0, December 2025

Section	Change Summary
All	• Removed *Core for MachXO3D – Lattice Propel Builder* from the document title. • Added the IP version information on the cover page. • Added a note on the IP version in the *Revision History* section. • Minor adjustments to ensure that the document is consistent with Lattice Semiconductor's inclusive language policy. • Updated all instances of *I²C* to *I2C*. • Made editorial fixes.
Disclaimers	Updated boilerplate.
Inclusive Language	Added boilerplate.
Introduction	Updated the description to include the MachXO4 device family.
Functional Description	• Added the *apb_pslverr_o* signal to Table 2.1. I2C Monitor Signal Description. • Updated the description for Table 2.4. Data Entry Format to include the MachXO4 device family.
Licensing and Ordering Part Number	Updated this section.
Resource Utilization	Added the resource utilization for the MachXO4 device family.
References	Updated this section.
Technical Support Assistance	Updated this section.

Revision 1.0, May 2020

Section	Change Summary
All	Initial release.

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