Color Space Converter IP

IP Version: 2.4.1

User Guide

FPGA-IPUG-02085-1.7

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
CMY(K)	Cyan, Magenta, Yellow (Black)
CSC	Color Space Converter
DSP	Digital Signal Processor
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
HIS	Hue, Intensity, Saturation
HSV	Hue, Saturation, Value
IP	Intellectual Property
JPEG	Joint Photographic Experts Group
LUT	Look-Up Table
MPEG	Moving Picture Experts Group
NTSC	National Television Standards Committee
PAL	Phase Alternate Line
RBG	Red, Green, Blue
RTL	Register Transfer Level
SECAM	Sequential Color and Memory
YIQ	Luminance, Chrominance (Y, I, Q)
YUV	Luminance, Chrominance (Y, U, V)
YCbCr	Luminance, Chrominance (Y, Cb, Cr)

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1. Introduction

Color Space Converters (CSC) convert signals from one color space to another color space. Color space conversion is often required to ensure compatibility with display devices or to make the image data amenable for compression or transmission. CSCs are widely used in video and image display systems including televisions, computer monitors, color printers, video telephony and surveillance systems. They are also used in many video/image compression and processing applications, and in the implementation of National Television Standards Committee (NTSC)/Phase Alternate Line (PAL)/ Sequential Color and Memory (SECAM) television standards, Joint Photographic Experts Group (JPEG) system, and Moving Picture Experts Group (MPEG) system.

The Lattice Color Space Converter IP Core is widely parameterizable and can support any custom color space conversion requirement. Furthermore, several commonly used color space conversion methods are provided as ready-to-use configurations.

1.1. Quick Facts

Table 1.1 presents a summary of the Color Space Converter IP core.

Table 1.1. Quick Facts

IP Requirements	Supported Devices	CrossLink™-NX, Certus™-NX, CertusPro™-NX, MachXO5™-NX, Lattice Avant™, Certus-N2
	IP Changes[1]	For a list of changes to the IP, refer to the Color Space Converter IP Release Notes (FPGA-RN-02053).
Resource Utilization	Supported User Interface	Native interface, see the Signal Description section
	Resources	See the Resource Utilization section
Design Tool Support	Lattice Implementation	IP Core v2.4.1 – Lattice Radiant™ software 2025.2
	Synthesis	Lattice Synthesis Engine
		Synopsys® Synplify Pro® for Lattice
	Simulation	For a list of supported simulators, see the Lattice Radiant software user guide.

Note:

1. In some instances, the IP may be updated without changes to the user guide. This user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

1.2. Features

The key features of the Color Space Converter IP Core include:

- Input data width from 8 to 16 bits
- Output data width from 8 to 16 bits
- Signed or unsigned input and output data
- Supports standard configurations as well as custom configurations
- Parameterized coefficients precision from 9 to18 bits
- Full precision as well as limited precision output
- Programmable precision and rounding options for the output
- Optional sequential or parallel architecture for area or throughput optimization
- Registered input option available for input setup time improvement

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

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1.3.2. Signal Names

Signal names that end with:

- _n are active low
- _i are input signals
- _o are output signals

1.3.3. Attribute Names

Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

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2. Functional Descriptions

2.1. Overview

A color space is a three-dimensional representation of the color and intensity of an image's pixel. An example of a color space is RGB wherein each pixel's color is represented by the constituent red, green, and blue components. This color space is used in computer displays where the CRT uses red, green, and blue to display a multi-colored pixel. However, an RGB color space may not be ideal for image processing, efficient image transmission, or human interpretation of color information. A color space that represents a color pixel using the characteristics of hue, saturation, and brightness is more akin to the way humans interpret color information. HIS and HSV are examples of such color spaces.

It is known that human vision is more sensitive to brightness than color. In an image, the color green carries more of the brightness information than the red and blue components. Therefore, some of the information from the red and blue color components can be reduced in order to compress the signal for more efficient processing. It is useful to deploy a color space representing brightness (luminance) and color components (chrominance) for processing applications. Common examples of such color spaces are YUV, YIQ, and YCbCr, which are part of many video standards.

The following are some commonly used color spaces:

- **RGB** – Red, Green, Blue. This color space is used in computer displays.
- **YIQ, YUV, YCbCr** – Luminance, Chrominance. These color spaces are used in television systems. YIQ is used in NTSC systems, YUV is used in PAL systems and YCbCr is used in digital television systems.
- **CMY(K)** – Cyan, Magenta, Yellow, (Black). This color space is used in printing applications. The fourth component, black, is used to improve both the density range and color range. This removes the need to generate a good black color from CMY components.

Figure 2.1 shows the functional diagram for the Color Space Converter IP Core.

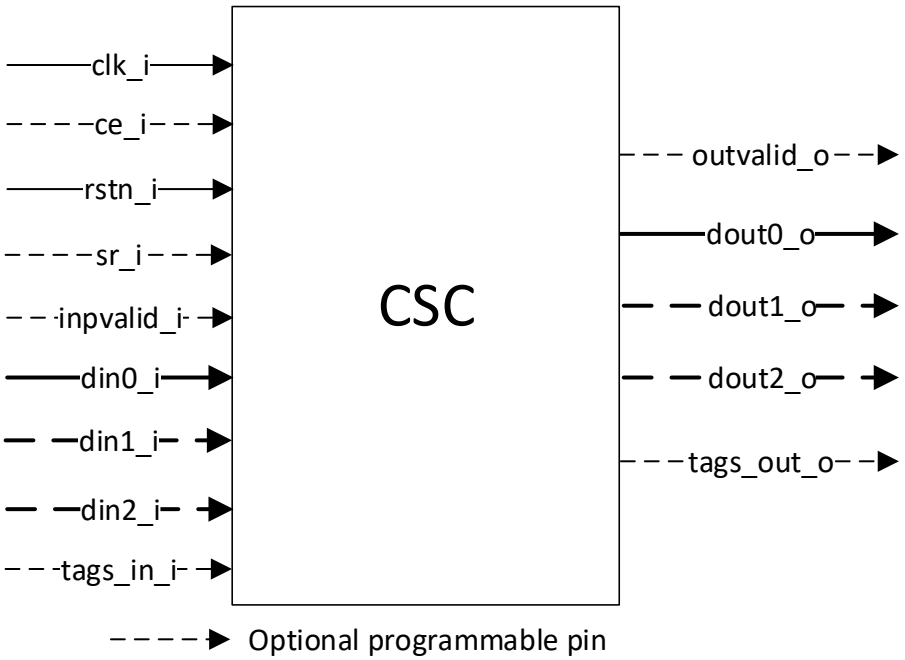

Figure 2.1. Functional Block Diagram

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2.2. Signal Description

Table 2.1. Color Space Converter IP Core Signal Description

Port Name	I/O	Width	Description
Clock and Reset			
clk_i	In	1	Reference clock for input and output data.
rstn_i	In	1	System-wide asynchronous active-low reset signal.
I/O Ports			
din0_i[1]	In	*Input data width*[3]	Input data. When the sequential architecture is selected, this port is used to give input data for all the three input color planes in sequence. When the parallel architecture is selected, this port is used to give input data for the first input color plane.
dout0_o[1]	Out	*Output data width*[3]	Output data. When the sequential architecture is selected, this port is used to give output data for all the three output color planes in sequence. When the parallel architecture is selected, this port is used to give output data for the first output color plane.
tags_in_i	In	*Tags Width*[3]	User-defined tag input, up counter.
tags_out_o	Out	*Tags Width*[3]	User-defined tag output, up counter which is delayed by *Latency* with respect to tags_in_i.
Parallel Architecture			
din1_i[1, 2]	In	*Input data width*[3]	Input data for second color plane.
din2_i[1, 2]	In	*Input data width*[3]	Input data for third color plane.
dout1_o[1, 2]	Out	*Output data width*[3]	Output data for second color plane.
dout2_o[1, 2]	Out	*Output data width*[3]	Output data for third color plane.
Valid Signals			
inpvalid_i	In	1	Input data valid. Indicates valid data is present on din0_i (also on din1_i and din2_i when present). When the parallel architecture is selected, this port is optional. In this case, this port is not used directly in the core but is used to generate the outvalid_o signal after initial core latency. When the sequential architecture is selected, this port is always enabled. In this case, this port is used inside the core and also used to generate the outvalid_o signal after initial core latency. Also, when the sequential architecture is selected, this signal should be asserted high for one clock cycle when valid data for the first input color plane is present on the din0_i port. For the second and third input color planes data, this signal should be low. Input data for all the three input color planes should be applied at successive clock cycles without any gap.
outvalid_o	Out	1	Output data valid. Indicates valid data is present on dout0_o (also on dout1_o and dout2_o when present). When the parallel architecture is selected, this port is optional. When the sequential architecture is selected, this port is always enabled and asserted high when the valid data is present for the first output color plane. During output data of second and third color planes outvalid_o is low.
Optional I/O			
ce_i	In	1	Clock Enable. While this is de-asserted, the core ignores all other synchronous inputs and maintain its current state.
sr_i	In	1	Synchronous Reset. Asserted for at least one clock period duration to re-initialize the core. After synchronous reset, all internal registers are cleared and outvalid_o goes low.

Notes:

2. For RGB to YCbCr: din0_i/din1_i/din2_i/dout0_o/dout1_o/dout2_o stands for R/G/B/Y/Cb/Cr accordingly.
   For YCbCr to RGB: din0_i/din1_i /din2_i /dout0_o /dout1_o /dout2_o stands for Y/Cb/Cr/R/G/B accordingly.
   For YUV to RGB: din0_i/din1_i /din2_i /dout0_o /dout1_o /dout2_o stands for Y/U/V/R/G/B accordingly.
   For RGB to YUV: din0_i/din1_i /din2_i /dout0_o /dout1_o /dout2_o stands for R/G/B/Y/U/V accordingly.

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For YIQ to RGB: din0_i/din1_i /din2_i /dout0_o /dout1_o /dout2_o stands for Y/I/Q/R/G/B accordingly.
For RGB to YIQ: din0_i/din1_i /din2_i /dout0_o /dout1_o /dout2_o stands for R/G/B/Y/I/Q accordingly.
For YIQ to YUV: din0_i/din1_i /din2_i /dout0_o /dout1_o /dout2_o stands for Yin/I/Q/Yout/U/V accordingly.

3. These ports are available only when the selected *Architecture* is Parallel.
4. The bit width of some signals is set by the attribute. Refer to Table 2.3 for the description of these attributes.

2.3. Attribute Summary

The configurable attributes of the Color Space Converter IP Core are shown in Table 2.2.The attributes can be configured through the IP Catalog's Module/IP wizard of the Lattice Radiant software.

Table 2.2. Attributes Table

Attribute	Selectable Values	Default	Dependency on Other Attributes
Input/Coefficient			
General			
Core Type	Custom, Computer RGB to YCbCr: SDTV, Computer RGB to YCbCr: HDTV, Studio RGB to YCbCr: SDTV, Studio RGB to YCbCr: HDTV, YCbCr: SDTV to Computer RGB, YCbCr: HDTV to Computer RGB, YCbCr: SDTV to Studio RGB, YCbCr: HDTV to Studio RGB, YUV to Computer RGB, Computer RGB to YUV, YIQ to Computer RGB, Computer RGB to YIQ, YIQ to YUV	Computer RGB to YCbCr:SDTV	—
Output Data Equation	—	See Table 2.3	—
Dout0			
coeff0	Calculated	0.257	*Core Type*
coeff1	Calculated	0.504	*Core Type*
coeff2	Calculated	0.098	*Core Type*
constant	Calculated	16.0	*Core Type*
Dout1			
coeff0	Calculated	-0.148	*Core Type*
coeff1	Calculated	-0.291	*Core Type*
coeff2	Calculated	0.439	*Core Type*
constant	Calculated	128.0	*Core Type*
Dout2			
coeff0	Calculated	0.439	*Core Type*
coeff1	Calculated	-0.368	*Core Type*
coeff2	Calculated	-0.071	*Core Type*
constant	Calculated	128.0	*Core Type*
Input Setting			
Architecture	Serial, Parallel	Parallel	—
Support VSS IP Suite	Checked, Unchecked	Checked	—
Input data type	Signed, Unsigned	Signed	—

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Attribute	Selectable Values	Default	Dependency on Other Attributes
Input data width	8–16	14	—
Coefficient Width	9–18	14	—
Tags width	9–18	9	Active if *Support VSS IP Suite* == True
Implementation			
Registered Input	Enable, Disable	Enable	—
Keep data at blank time	Checked, Unchecked	Unchecked	—
Optional Input/Output Ports			
Clock Enable	Checked, Unchecked	Checked	—
Synchronous Reset	Checked, Unchecked	Checked	—
Inpvalid/Outvalid	Checked, Unchecked	Checked	Active if *Architecture* == Parallel
Output			
Output latency			
Latency	Calculated	—	—
Output Setting			
Output data type	Signed, Unsigned	Signed	—
Output data width	8–16	12	—
Precision Control			
Overflow	Saturation, Wrap-around	Saturation	—
Rounding	None, Rounding up, Rounding away from zero, Rounding forwards zero, Convergent rounding	None	—

Table 2.3. Attributes Descriptions

Attribute	Description
Input/Coefficient	
Core Type	Selects between Custom and pre-defined standard configurations. When the *Core Type* is selected as Custom, you must manually enter the coefficient values in the Custom Coefficients tab.
Output Data Equation	Specifies the equation of Expected Output Data Dout = *coeff0*din0 + coeff1*din1 + coeff2*din2 + constant*
Architecture	Selects between parallel and sequential implementation architectures.
Support VSS IP Suite	If enabled, input port tags_in_i and output port tags_out_o are added to the core.
Input data type	Signed or Unsigned Input data type
Input data width	Specifies the bit width for the input color planes.
Coefficient Width	Specifies the coefficient precision width.
Tags width	Specifies the bit width for the tag ports: tags_in_i and tags_out_o.
Registered Input	If enabled, inputs are registered. The core inputs' setup time improves by registering the inputs. This attribute is useful when the input data is provided on the device pins
Keep data at blank time	This attribute keeps the auxiliary data of the video stream unchanged during blank time.
Clock Enable	If enabled, input port ce_i is added to the core.
Synchronous Reset	If enabled, input port sr_i is added to the core.
Inpvalid/Outvalid	Configurable depending on the value of *Architecture*. If enabled, inpvalid_i and outvalid_o ports are added to the core.
Output	
Latency	Provides the output latency for the selected core configuration.
Output data type	Specifies the bit width of the output color planes.
Output data width	Provides the latency for the selected core configuration.

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Attribute	Description
Overflow	This attribute is available whenever there is a need to drop some of the MSBs from the true output. Saturation – The output is made equal to the maximum positive or negative value based on the sign bits. Wrap-around – The MSBs are discarded without making any corrections.
Rounding	Allows you to specify the rounding method when there is a need to drop one or more LSBs from the true output. None – discards all bits to the right of the output lease significant bit and leaves the output uncorrected. Rounding up – Rounds up if the fractional part is exactly one-half. For example, 2.5 is rounded to 3 and -2.5 is rounded to -3. Rounding away from zero – Rounds away from zero if the fractional part is exactly one-half. For example, 2.5 is rounded to 3 and -2.5 is rounded to -3. Rounding towards zero – Rounds towards zero if the fractional part is exactly one-half. For example, 2.5 is rounded to 2 and -2.5 is rounded to -2. Convergent rounding – Rounds to the nearest even value if the fractional part is exactly one-half. For example, 2.5 is rounded to 2; -2.5 is rounded to -2; 3.5 is rounded to 4; -3.5 is rounded to -4.

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2.4. Operations Details

2.4.1. Timing Specifications

This section contains operational timing diagrams applicable to the Color Space Converter IP Core interfaces.

2.4.1.1. Parallel Architecture

Figure 2.2 shows the input and output signal timing diagram for the parallel architecture. The input data for all the three color planes are applied simultaneously on the input ports din0_i, din1_i, and din2_i.

The signal inpvalid_i is asserted to indicate a valid input data present on the input ports. After a latency of a few cycles, the output data for all three color planes appears on the output ports dout0_o, dout1_o and dout2_o. The signal outvalid_o is asserted to indicate valid output data present on the output ports.

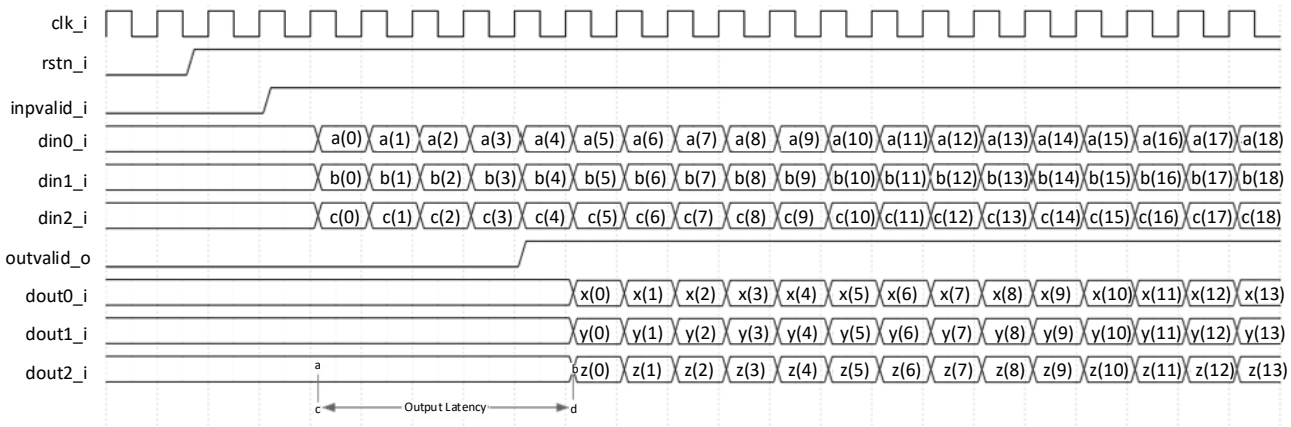

Figure 2.2. Parallel Architecture Timing Diagram

2.4.1.2. Sequential Architecture

Figure 2.3 shows the input and output signal timing for the sequential architecture. The input data for all three color planes are applied in sequence on the input port din0_i. The signal inpvalid_i is asserted to indicate the first color plane data on din0_i. In the following two cycles, the second and third color plane data are applied on din0_i. After a latency of a few cycles, the output data for the first color plane appears on the output port dout0_o. The signal outvalid_o is asserted to indicate the first color plane data on dout0_o. In the following two cycles, the second and third color plane data appear on dout0_o.

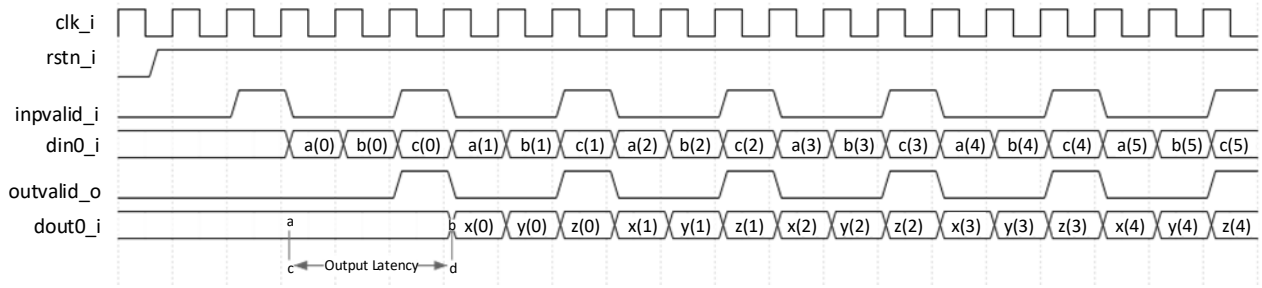

Figure 2.3. Sequential Architecture Timing Diagram

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2.5. Color Space Conversion

Color space conversion is required when transferring data between devices that use different color space models. For example, RGB to YCbCr color space conversion is required when displaying a computer image on a television. Similarly, YCbCr to RGB color space conversion is required when displaying television movies on a computer monitor. As a color can be represented completely using three dimensions, a color space is a three dimensional space. Color space conversion is a one-to-one mapping from one color space to another color space.

R'G'B' to Y'CbCr color space conversion is provided in the following equations. The prime notations are used to denote gamma-corrected values.

Y' = 0.257 * R' + 0.504 * G' + 0.098 * B' + 16

Cb = -0.148 * R' -0.291 * G' + 0.439 * B' + 128

Cr = 0.439 * R' - 0.368 * G' -0.071 * B' + 128

Y'CbCr to computer R'G'B' conversion is provided in the following equations.

R' = 1.164 * Y' +0.0 * Cb + 1.596 * Cr -222.912

G' = 1.164 * Y' -0.392 * Cb -0.813 * Cr + 135.616

B' = 1.164 * Y' + 2.017 * Cb + 0.0 * Cr -276.8

Examples of applications that use CSC for R'G'B' to Y'CbCr Conversion and Y'CbCr to R'G'B' conversion are shown in Figure 2.4 and Figure 2.5.

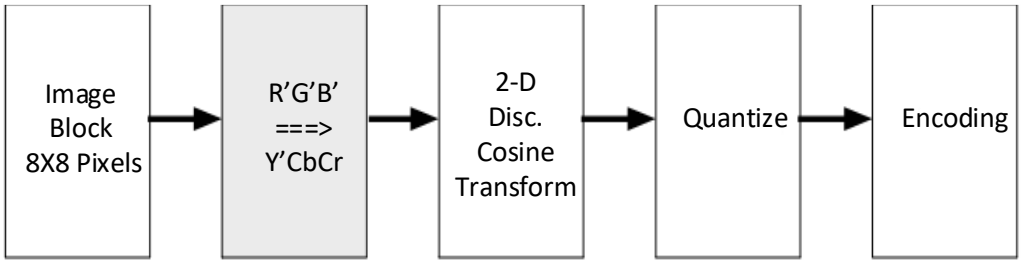

Figure 2.4. JPEG Encoding Application

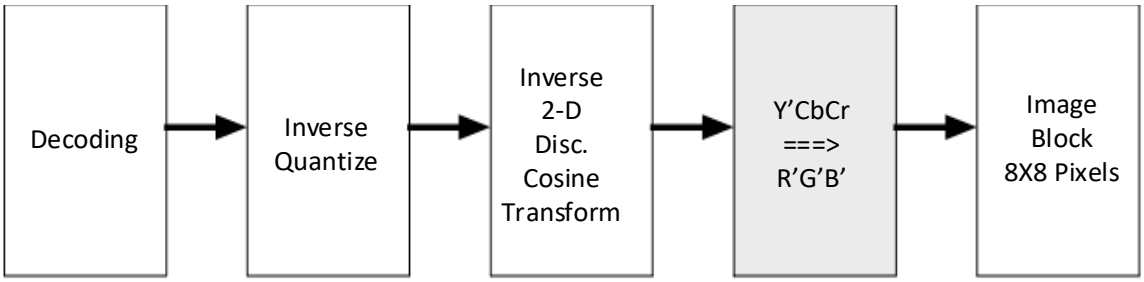

Figure 2.5. JPEG Decoding Application

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3. IP Generation and Evaluation

This section provides information on how to generate the IP Core using the Lattice Radiant Software and how to run simulation and synthesis. For more details on the Lattice Radiant Software, refer to the Lattice Radiant software user guide.

Note: The screenshots provided are for reference only. Details may vary depending on the version of the IP or software being used. If there have been no significant changes to the GUI, a screenshot may reflect an earlier version of the IP.

3.1. Licensing the IP

The Color Space Converter IP is provided at no additional cost with the Lattice Radiant software.

3.2. Generating the IP

The Lattice Radiant Software allows you to customize and generate modules and IPs and integrate them into the device's architecture. The procedure for generating the Color Space Converter IP Core in Lattice Radiant Software is described below.

To generate the Color Space Converter IP Core:

1. Create a new Lattice Radiant Software project or open an existing project.
2. In the **IP Catalog** tab, double-click on **Color Space Converter** under **IP, DSP** category. The **Module/IP Block Wizard** opens as shown in Figure 3.1. Enter values in the **Component name** and the **Create in** fields and click **Next**.

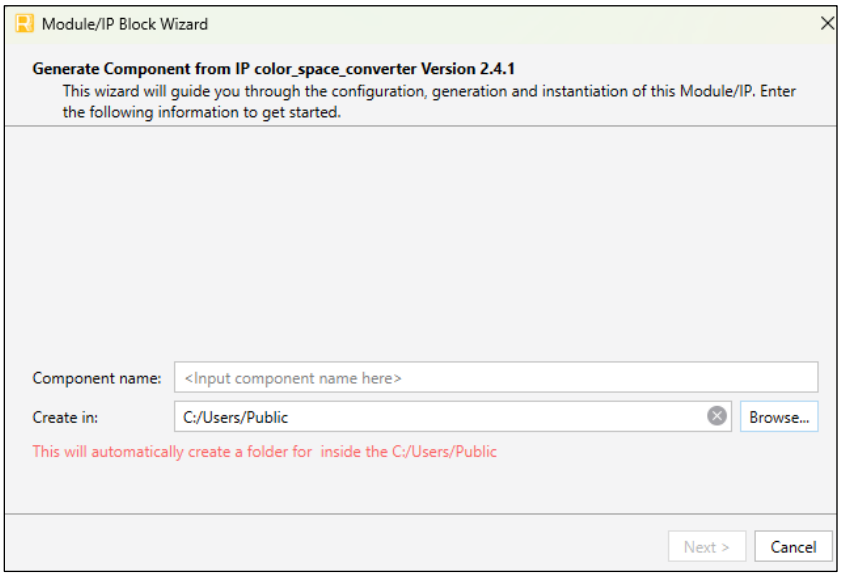

Figure 3.1. Module/IP Block Wizard

3. In the module's dialog box of the **Module/IP Block Wizard** window, customize the selected Color Space Converter IP Core using drop-down menus and check boxes. As a sample configuration, see Figure 3.2. For configuration options, see the Attribute Summary section.

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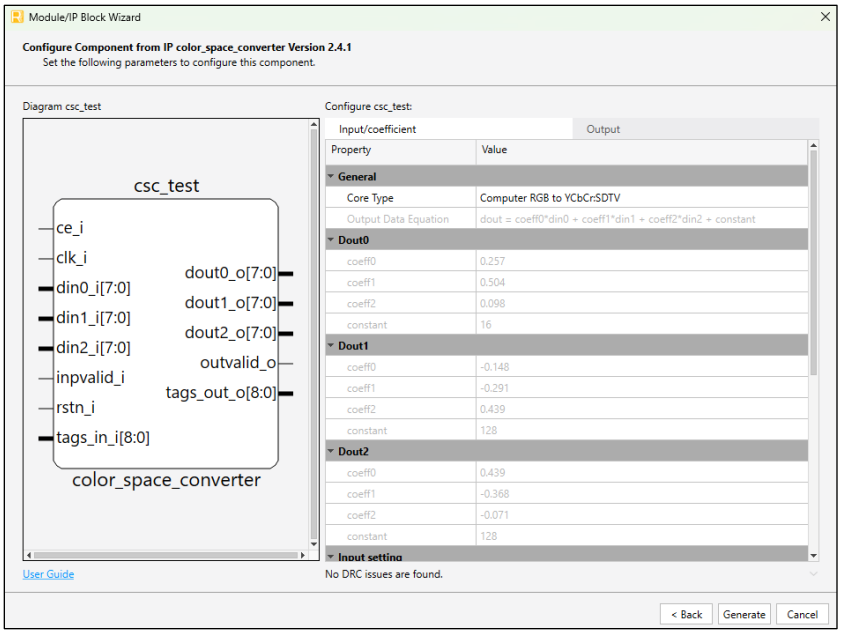

Figure 3.2. Configure User Interface of Color Space Converter IP Core

4. Click **Generate**. The **Check Generated Result** dialog box opens, showing design block messages and results (Figure 3.3).

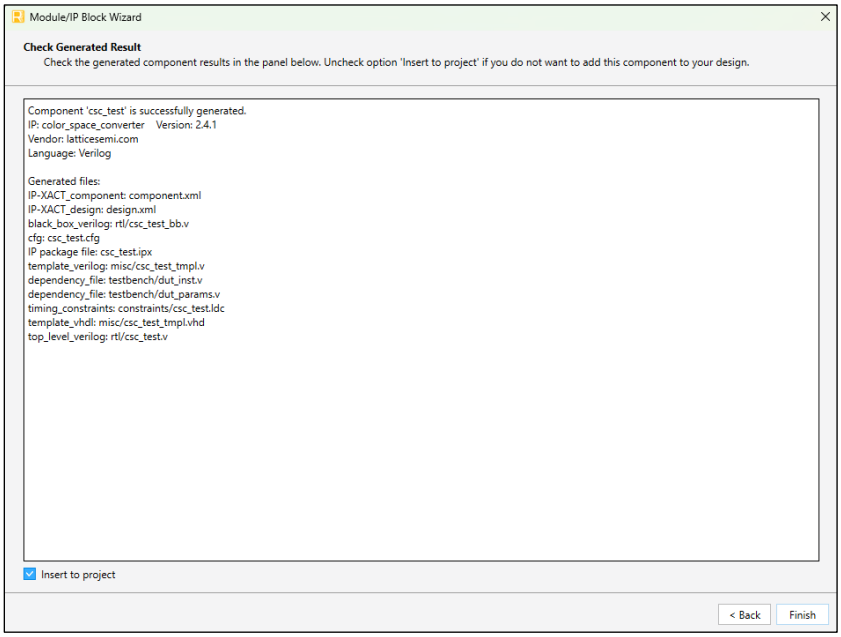

Figure 3.3. Check Generated Result

5. Click the **Finish** button. All the generated files are placed under the directory paths in the **Create in** and the **Component name** fields shown in Figure 3.1.

The generated Color Space Converter IP Core package includes the closed-box (<Component name>_bb.v) and instance templates (<Component name>_tmpl.v/vhd) that can be used to instantiate the core in a top-level design. An example RTL top-level reference source file (<Component name>.v) that can be used as an instantiation template for the IP core is also provided. You may also use this top-level reference as the starting template for the top-level for their complete design. The generated files are listed in Table 3.1.

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Table 3.1. Generated File List

Attribute	Description
<Component name>.ipx	This file contains the information on the files associated to the generated IP.
<Component name>.cfg	This file contains the attribute values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration attributes of the IP in IP-XACT 2014 format.
rtl/<Component name>.v	This file provides an example RTL top file that instantiates the IP core.
rtl/<Component name>_bb.v	This file provides the synthesis closed-box.
misc/<Component name>_tmpl.v misc /<Component name>_tmpl.vhd	These files provide instance templates for the IP core.

3.3. Running Functional Simulation

1. Click the  button located on the **Toolbar** to initiate the **Simulation Wizard** shown in Figure 3.4.

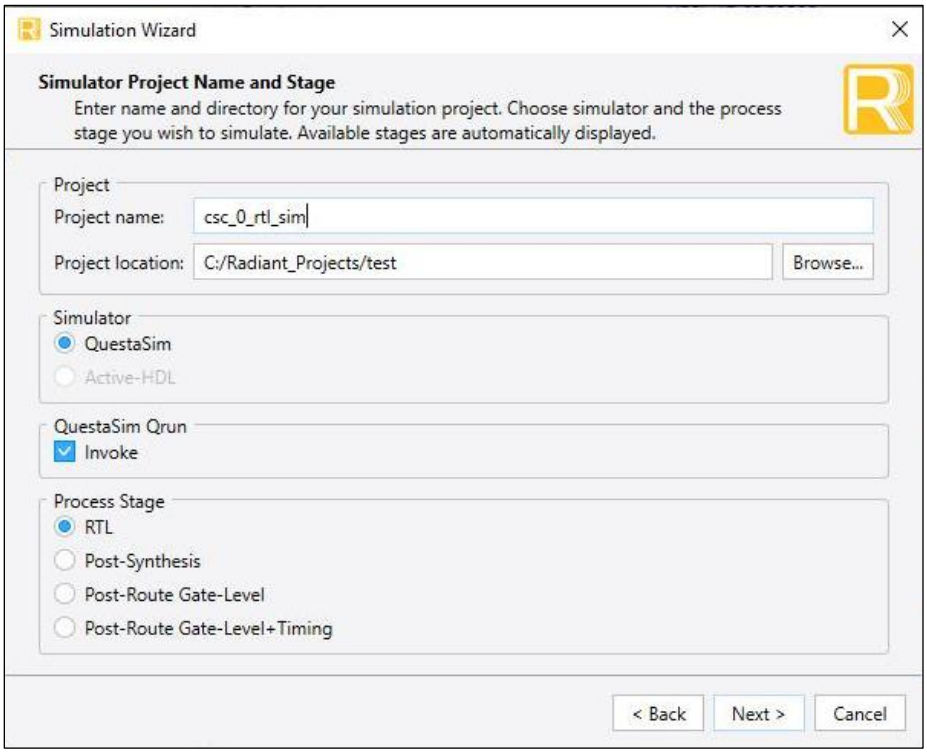

Figure 3.4. Simulation Wizard

2. Click **Next** to open the **Add and Reorder Source** window, as shown in Figure 3.5.

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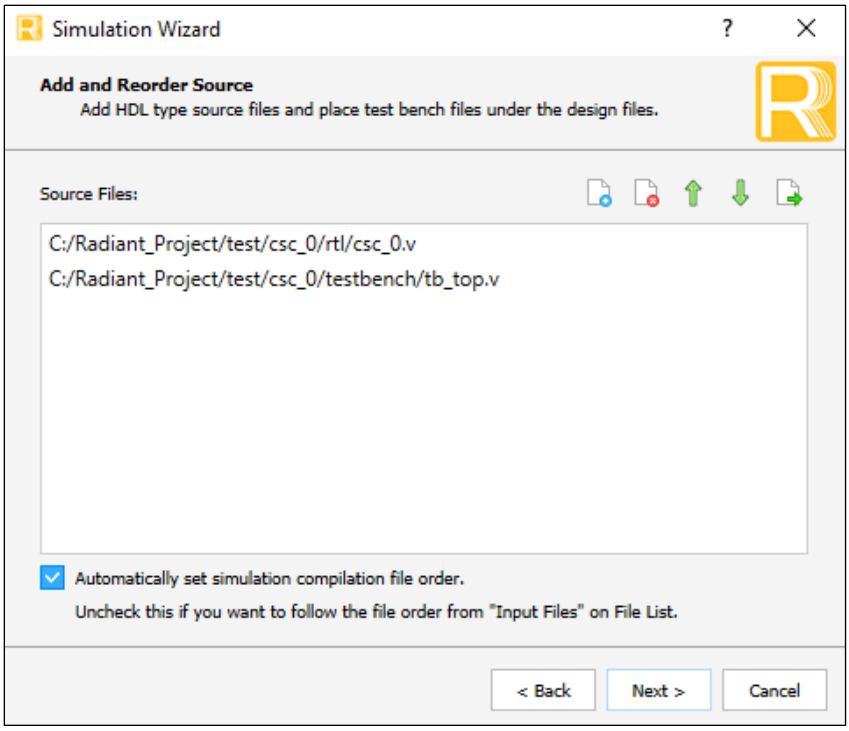

Figure 3.5. Adding and Reordering Source

3. Click **Next**. The **Summary** window is shown. Click **Finish** to run the simulation.

   Note: It is necessary to follow the procedure above until it is fully automated in the Lattice Radiant Software Suite. The results of the simulation in our example are provided in Figure 3.6.

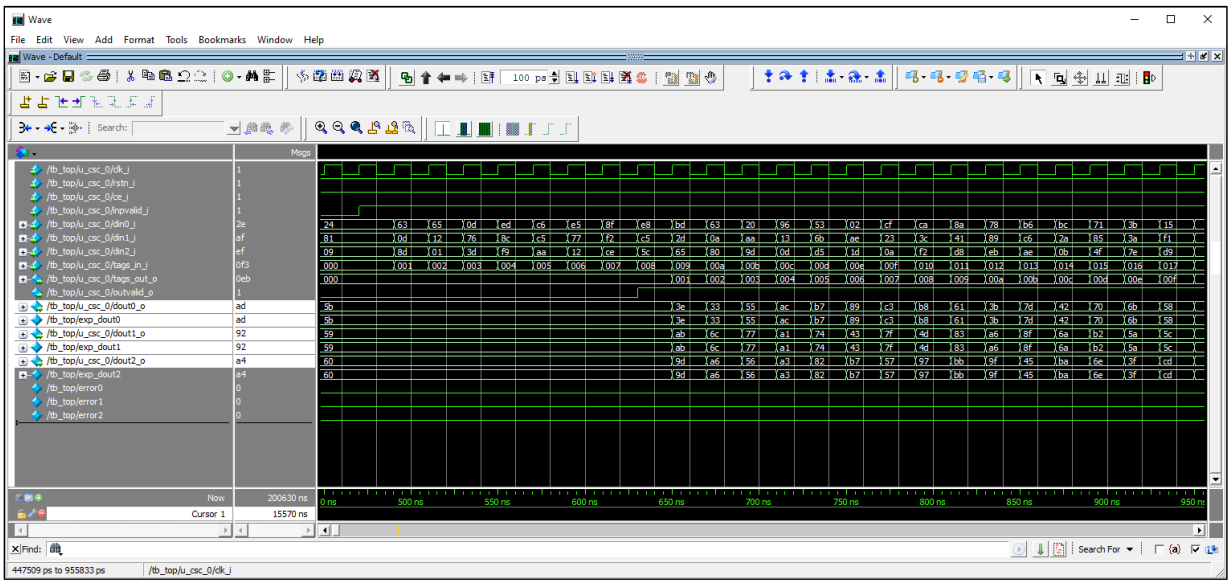

Figure 3.6. Simulation Waveform

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3.4. Constraining the IP

It is your responsibility to provide proper timing and physical design constraints to ensure that the design meets the desired performance goals on the FPGA. The content of the following IP constraint file can be added to the user design constraints:
<Instance_Path>/<Instance_Name>/constraints/<Instance_Name>.ldc
The above constraint file has been verified with the IP instantiated directly in the top-level module. The constraint in this file can be modified given a complete understanding of the effect of the constraint.
To use this constraint file, copy the content of the <Instance_Name>.ldc to the top-level design constraint for post-synthesis.
Refer to Lattice Radiant Timing Constraints Methodology (FPGA-AN-02059) for details on how to constraint the design.

3.5. Hardware Validation

No hardware validation has been done for this IP.

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4. Design Considerations

4.1. Limitations

For IP configurations with *Output data width* == 16 and *Coefficient width* == 18, simulation failure may occur because of data mismatch caused by design limitations. Consider reducing the *Output data width* or *Coefficient width* value.

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Appendix A. Resource Utilization

The following tables show the resource utilization of the Color Space Converter IP Core for devices using Synplify Pro of the Lattice Radiant software 2025.2. Default configuration is used and some attributes are changed from the default value to show the effect on the resource utilization.

Table A.1. Resource Utilization for the LN2-CT-20ES-1ASG410I Device

Configuration	Clk Fmax (MHz)[1]	Registers	LUTs	DSP
Default	226.50	344	190	9
Architecture = Sequential, Others = Default	250	251	73	3
Core Type = YUV to Computer RGB, Others = Default	179.73	309	124	4
Coefficient Width = 18, *Tags Width* = 10, Others = Default	207.64	406	244	9

Note:

1. Fmax is generated when the FPGA design only contains Color Space Converter IP Core and the target frequency is 200 MHz. These values may be reduced when user logic is added to the FPGA design.

Table A.2. Resource Utilization for the LAV-AT-E70-3LFG1156I Device

Configuration	Clk Fmax (MHz)[1]	Registers	LUTs	DSP
Default	217.39	344	190	9
Architecture = Sequential, Others = Default	250	251	73	3
Core Type = YUV to Computer RGB, Others = Default	250	241	124	4
Coefficient Width = 18, *Tags Width* = 10, Others = Default	218.77	406	244	9

Note:

1. Fmax is generated when the FPGA design only contains Color Space Converter IP Core and the target frequency is 200 MHz. These values may be reduced when user logic is added to the FPGA design.

Table A.3. Resource Utilization for the LIFCL-40-9BG400I Device

Configuration	Clk Fmax (MHz)[1]	Registers	LUTs	DSP
Default	200.00	344	206	9
Architecture = Sequential, Others = Default	200.00	251	82	3
Core Type = YUV to Computer RGB, Others = Default	200.00	309	139	4
Coefficient Width = 18, *Tags Width* = 10, Others = Default	200.00	406	260	9

Note:

1. Fmax is generated when the FPGA design only contains Color Space Converter IP Core and the target frequency is 200 MHz. These values may be reduced when user logic is added to the FPGA design.

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References

- Color Space Converter IP Release Notes (FPGA-RN-02053)
- Lattice Radiant Timing Constraints Methodology (FPGA-AN-02059)
- Certus-NX web page
- Certus-N2 web page
- CertusPro-NX web page
- CrossLink-NX web page
- MachXO5-NX web page
- Avant-E web page
- Avant-G web page
- Avant-X web page
- Color Space Converter (CSC) IP Core web page
- Lattice Radiant Software web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

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Revision History

Note: In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

Revision 1.7, IP v2.4.1, December 2025

Section	Change Summary
All	• Added a note on IP version in Quick Facts and *Revision History* sections. • Performed minor formatting and editorial edits.
Acronyms in This Document	Updated list of acronyms.
Introduction	Updated Table 1.1. Quick Facts as follows: • Added IP version. • Removed earlier IP versions.

IP Generation and Evaluation	• Added a note on IP version in GUI in the IP Generation and Evaluation section.
	• Added the Licensing the IP section.
	• Updated the following figures:
	  • Figure 3.1. Module/IP Block Wizard
	  • Figure 3.2. Configure User Interface of Color Space Converter IP Core
	  • Figure 3.3. Check Generated Result
	• Removed the *IP Evaluation* section.

Ordering Part Number	Removed this section.
Design Considerations	Added this section.
Resource Utilization	Updated resource utilization for the latest software version.
References	Updated references.

Revision 1.6, IP v2.4.0, July 2025

Section	Change Summary
Introduction	Added the Quick Facts section.
IP Generation and Evaluation	Updated the following figures: • Figure 3.1. Module/IP Block Wizard • Figure 3.2. Configure User Interface of Color Space Converter IP Core • Figure 3.3. Check Generating Result • Figure 3.4. Simulation Wizard
Ordering Part Number	Changed from *Multi-site Perpetual* to *Single Seat Perpetual*.
Resource Utilization	Updated resource utilization for the latest software version.

Revision 1.5, IP v2.3.0, December 2024

Section	Change Summary
All	• Renamed document from *Color Space Converter IP Core* to *Color Space Converter IP*. • Performed minor formatting and editorial edits.
Inclusive Language	Added the inclusive language boilerplate.
IP Generation and Evaluation	Changed *black box* to *closed-box* in the Generating the IP section.
Ordering Part Number	Updated Table 4.1. Ordering Part Number as follows: • Added OPN for Certus-N2, Avant-G, and Avant-X devices. • Changed from *Single Machine Annual* to *Single Seat Annual* license.
Resource Utilization	Added Table A.1. Resource Utilization for the LN2-CT-20-1CBG484I Device.
References	Updated references.

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Document Revision 1.4, February 2024

Section	Change Summary
All	Updated the document title to *Color Space Converter IP Core*.
Disclaimers	Updated this section.
IP Generation and Evaluation	Added the Constraining the IP section.
Resource Utilization	Updated device part number to *LAV-AT-E70-3LFG1156I* in the caption and description of Table A.2. Resource Utilization.
References	Added links to CrossLink-NX web page, Certus-NX web page, CertusPro-NX web page, MachXO5-NX web page, Avant-E web page, Lattice Radiant Software web page, and Lattice Insights for training series and learning plans.

Document Revision 1.3, December 2022

Section	Change Summary
All	Minor adjustments in formatting across the document.
Introduction	Removed Quick Facts section.
Attribute Summary	• Updated Table 2.1. Color Space Converter IP Core Signal Description to change input width to tags width and add reference to table note 3. • Updated entire Table 2.2. Attributes Table and Table 2.3. Attributes Descriptions content.
IP Generation and Evaluation	• Changed section name to Generating the IP. • Updated Figure 3.1. Module/IP Block Wizard, Figure 3.2. Configure User Interface of Color Space Converter IP Core, Figure 3.3. Check Generating Result, Figure 3.4. Simulation Wizard, Figure 3.5. Adding and Reordering Source, and Figure 3.6. Simulation Waveform. • Added Hardware Validation section.
Ordering Part Number	Updated section to add MachXO5-NX and Avant OPNs.
Appendix A. Resource Utilization	Updated Table A.2. Resource Utilization to include Avant support and corrected values in Table A.3. Resource Utilization.

Document Revision 1.2, June 2021

Section	Change Summary

Introduction	• Removed last paragraph.
	• Updated Table 1.1. Quick Facts.
	  • Added CertusPro-NX product family.
	  • Added LFD2NX-17 and LFCPNX-100 devices.
	  • Revised Lattice Implementation.
	  • Revised reference to Lattice Radiant Software User Guide.

Ordering Part Number	Added part numbers.
References	Revised reference to Lattice Radiant Software User Guide and removed link.
Appendix A. Resource Utilization	Updated device to LIFCL-40-9BG400I.

Document Revision 1.1, June 2020

Section	Change Summary
Introduction	Updated Table 1.1. • Added Certus-NX support. • Added LFD2NX-40 as targeted device. • Updated Synopsis Synplify Pro version. • Updated Lattice Implementation to Lattice Radiant 2.1.
Attribute Summary	Changed selectable values for *Registered Input.*
Ordering Part Number	Added this section.
Appendix A. Resource Utilization	Updated device to LIFCL-40-9BG400I.

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Document Revision 1.0, February 2020

Section	Change Summary
All	Initial release.

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