Lattice Radiant Software 2.0 Release Notes

Welcome to Lattice Radiant® software, the complete design environment for Lattice Semiconductor Field Programmable Gate Arrays (FPGAs).

What's New in Radiant Software 2.0

▶ **Device Support:**

- CrossLink-NX Device Family for the following packages:
    - 40K (-7/-8/-9) HP/LP 1.0V (COM/IND) - CABGA400
    - 40K (-7/-8/-9) HP/LP 1.0V (COM/IND) - CSBGA289
    - 40K (-7/-8/-9) HP/LP 1.0V (COM/IND) - QFN72

    The *Lattice Radiant 2.0 Software Guide for Lattice Diamond Users* has been enhanced to help users to migrate their designs to CrossLink-NX devices using the Radiant software. Users with designs on such Lattice devices as CrossLink and ECP5, designed using Lattice Diamond software, can use this guide to quickly grasp concepts of the new features of CrossLink-NX devices and designing with the Radiant software.

▶ **Tool and Other Enhancements:**

- **Device Constraint Editor** – Updates and enhancements have been added to Device Constraint Editor.
- **ECO Editor** – A new Radiant software tool has been added that supports interactive Engineering Change Order (ECO) editing.
- **Floorplan View** – Updates and enhancements have been added to Floorplan View. Updates include a new I/O placement feature that is used for I/O assignment such as DDR interface, DQS and clock assignments.
- **IP Catalog** – Updates and enhancements have been added to modules.
- **Power Calculator** – Updates and enhancements have been added to support CrossLink-NX devices.
- **Propagation of IP Constraints** – Radiant software now supports hierarchical constraints in IP applications and writes a new constraint file to propagate lower level constraints to top level under predefined constraint design rules.
- **Reveal Controller** – A new Radiant software tool has been added for the CrossLink-NX family to create virtual control switches/LEDs; reading/writing to bank of registers/memory; and read/write access to control and status registers of PLL, I2C/FIFO, DPHY, CDR and PCIe hard-IPs.

- o **Run Manager** – A new Radiant software tool has been added that is used to run multiple synthesis and place and route passes, compare the results of multiple implementations for further analysis to get best solutions.
- o **Source Template** –New CrossLink-NX templates have been added for both Verilog and VHDL in Source Template. In Source Template Editor, see:
  - Verilog > Primitive Templates > lifcl Primitive
  - VHDL > Primitive Templates > lifcl Primitive
- o **Simultaneous Switching Outputs (SSO) Calculator** – A new Radiant software tool has been added that estimates Simultaneous Switching Noise (SSN) affecting a victim pin according to the switching characteristics of aggressor pins.
- o **Timing Constraint Editor** – Updates and enhancements have been added to Timing Constraint Editor.

Help Resources

Available information resources for the Radiant software include the following:

- ▶ Online Help updated with CrossLink-NX content.
  - ▶ To view the Online Help, start the Lattice Radiant software and select the ⚡ "Getting Started" icon under Information Center.
- ▶ Installation:
  - ▶ *Lattice Radiant Software 2.0 Installation Guide for Windows*

    This document provides installation instructions for Windows OS.
  - ▶ *Lattice Radiant Software 2.0 Installation Guide for Linux/Ubuntu*

    This document provides installation instructions for Linux/Ubuntu OS.

System Requirements

The following shows the basic system requirements for Radiant software:

- ▶ Intel Pentium or Pentium-compatible PC
- ▶ 64-bit OS:
  - ▶ Windows 7, Windows 8 and 8.1, or Windows 10
  - ▶ Red Hat Enterprise Linux 6.6 or 7.0
  - ▶ Ubuntu version 16.04 LTS
- ▶ Approximately 3 GB free disk space
- ▶ Computer Memory Requirement: 2 GB Minimum, 3 GB Recommended
- ▶ 1024 X 768 graphics display

- ► Network adapter for license and network connectivity

- ► A Web browser with JavaScript capability

- ► Microsoft Internet Explorer 8 or higher (required for Aldec Active-HDL Lattice Edition simulator)

- ► Acrobat Reader 5.0 or later

Support for Third-Party Synthesis and Simulator Tools

In addition to the Synopsys Synplify Pro® for Lattice and Aldec Active-HDLTM Lattice Edition tools included with Radiant software suite, the following 3rd-Party Synthesis and Simulator tools are supported by Radiant software:

- ► **Synthesis Tools:**

    - ► Synopsys Synplify Pro FPGA synthesis software version P-2019.03LR-SP1

- ► **Simulator Tools:**

    - ► Aldec Active-HDL v10.5 or later
    - ► Mentor Questa® Sim v10.4g or later
        v10.6b or later (supports IP encryption)

Known Issues for Radiant Software 2.0

The following are known Issues for the Radiant software 2.0.

NVCM Boot time fluctuates when Osc frequency range strategy setting is set to 'Fast'.
Workaround: Use 'Medium' setting.
Devices affected: iCE40UP
Bug number: DNG-6499

PLL output is always 0 with advdataflow and dbg option for Active-HDL and Riviera.
Workaround: Don't use options advdataflow and dbg to run simulation with Active-HDL.
Devices affected: CrossLink-NX
Bug number: DNG-7752

For the Soft MIPI TX mode, the simulation results of the N port of clock and data are incorrect in high-speed mode.

For assistance with this issue, please contact Lattice Technical Support.
Devices affected: CrossLink-NX
Bug number: DNG-8199, DNG-8640

DPHY derating for CrossLink-NX does not work.

For assistance with this issue, please contact Lattice Technical Support.
Devices affected: CrossLink-NX
Bug number: DNG-8247

When using Aldec Active-HDL the RTL simulation of DLLDEL will output 'x' for VHDL DDR case when the clk < 100Mhz.

Workaround: Initialize clk signal as 1'b1 in the test bench and toggle the other signal after a delay of 20 ns.
Devices affected: CrossLink-NX
Bug number: DNG-8401

Post-syn fails when using Reveal with soft IP ROM.

Workaround: If you need to use Reveal with soft-IP ROM, then the data width of the ROM should be no more than 18 bits.
Devices affected: CrossLink-NX
Bug number: DNG- 8627

MAP does not report correct number of SEIO33 I/Os when sysCONFIG pins are used, and this can cause a resource violation.

Workaround: In Radiant 2.0 software, when enabling sysCONFIG pins in an LIFCL device, you need to set ldc_prohibit constraints on the sysCONFIG pins.
For example:
If you set JTAG_PORT = ENABLE, you need to prohibit usage of 4 JTAG pads: TDI, TCK, TMS, TDO.
Those 4 pads are E12, F12, E13, E11 in LIFCL-40 CSBGA289 package.
So, add the following constraints in the design:

```
{noformat}
ldc_prohibit -site E12
ldc_prohibit -site F12
ldc_prohibit -site E13
ldc_prohibit -site E11
{noformat}
```

Devices affected: CrossLink-NX
Bug number: DNG-8636

When generating PLL, calculations are not performed automatically. User must click "Calculate" button before generating PLL.

- When using the Radiant IP Catalog graphical user interface, if the Calculate button is not clicked before generating PLL, the PLL analog parameter values in the RTL will be incorrect. This affects all designs using PLL, such as GDDR 7:1 Receive Interface and GDDR with enabled PLL instantiation.

  Workaround: For configurations that use PLL, click the "Calculate" button before clicking the "Generate" button.

- If the ipgen command is used to generate PLL, the PLL analog parameter values in the RTL will be incorrect. This affects all designs using PLL, such as GDDR 7:1 Receive Interface and GDDR with enabled PLL instantiation.

  Workaround: For configurations that use PLL, the PLL must be manually generated using the Radiant IP Catalog graphical user interface. Click the "Calculate" button before clicking the "Generate" button.

Devices affected: CrossLink-NX
Bug number: DNG-8701

Tutorial project source files embedded in Radiant 2.0 software for CrossLink-NX Tutorial are incorrect and cause a synthesis error.

Workaround: Use updated tutorial project source files. A .zip file containing updated tutorial project source files can be downloaded from here:
https://www.latticesemi.com/view_document?document_id=52825
The updated tutorial can be downloaded from here:
https://www.latticesemi.com/view_document?document_id=52757
Devices affected: CrossLink-NX
Bug number: DNG-8739