Crosslink Product Family Qualification Summary

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1.0 INTRODUCTION

CrossLink™ from Lattice Semiconductor is a programmable video bridging device that supports a variety of protocols and interfaces for mobile image sensors and displays. The device is based on Lattice mobile FPGA 40nm technology. It combines the extreme flexibility of an FPGA with the low power, low cost and small footprint of an ASIC.

CrossLink supports video interfaces including MIPI® DPI, MIPI DBI, CMOS camera and display interfaces, OpenLDI, FPD-Link, FLATLINK, MIPI D-PHY, MIPI CSI-2, MIPI DSI, SLVS200, SubLVDS, HiSPi and more.
Lattice Semiconductor provides many pre-engineered IP (Intellectual Property) modules for CrossLink. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

The Lattice Diamond® design software allows large complex designs to be efficiently implemented using CrossLink. Synthesis library support for CrossLink devices is available for popular logic synthesis tools. The Diamond tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the CrossLink device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Interfaces on CrossLink provide a variety of bridging solutions for smart phone, tablets, wearables, VR, AR, Drone, Smart Home, HMI as well as adjacent ISM markets. The device is capable of supporting high-resolution, high-bandwidth content for mobile cameras and displays at 4k UHD and beyond.

This report details the Commercial/Industrial reliability qualification results of the Lattice CrossLink Commercial/Industrial Product Family.

Table 1.0.1 CrossLink Product Family Attributes

Part Attributes	LIF-MD6000				
	UWG36	UMG64	MG81	JMG80	KMG80
Die Fabrication Site	UMC, USJC				
Package Assembly Site	ASE Taiwan				
Final Test Site	ASE Taiwan				
Die Family (Product Line)	CrossLink				
Wafer Size	300mm				
Fabrication Process Technology	40LP-SA (40nm CMOS)				
Die Channel Length	Min 40nm				
Number of Mask Steps	45				
Die Size (W x L x T) (µm)	2507x2556x350	2507x2556x300			
Die Metallization	Cu				
# of Metallization Layers	9				
Thickness (Per Metallization Layer) (µm)	M1 - 0.125, M2-M5 – 0.14, M6-M7 – 0.21, M8 – 0.85, M9 – 3.4				
Die Interlevel Dielectric	IMD 1-5 – uLK, IMD 6-7 – LowK, IMD 8-9 - TEOS				
Die Passivation	PSG/SiN				
Passivation Thickness	PSG – 4000 Å, SiN - 5000 Å				
Die Preparation/Singulation	Laser Groove + Wafer Saw				
Package Type / Pin Count	WLCSP / 36	UCFBGA / 64	CSFBGA / 81	CTFBGA / 80	CKFBGA / 80
Package Size (mm)	2.535x2.583	3.5x3.5	4.5x4.5	6.5x6.5	7x7
Mold Compound Supplier/ID	NA	Sumitomo			
Mold Compound Type	NA	EME-G311SA Type C			
Flammability Rating	NA	V-0			
Fire Retardant Type/Composition	NA	Metal Hydroxide			
Glass Transition Temperature, Tg	NA	150 oC			
CTE (above and below Tg) (ppm/C)	NA	34			
Cu Pillar Composition	NA	98.2 Sn / 1.8 Ag			
Cu Pillar Diameter/Height	NA	45 µm/50 µm			
Redistribution Metal	Cu	NA			
UBM	Ti/Cu				
Repassivation Material	PBO (HD8820)	PI (HD4000E)			
Coating Film	LC2850	NA			
Bump Diagram	107699	107666	107652	107683	107663
Substrate Material	NA	PFR800 Aus410			
Substrate Thickness	NA	0.157 mm (+/-0.030)			0.282 mm (+/-0.040)
# of Substrate Metal Layers	NA	2 layers			4 layers
Plating Composition of Ball Solderable Surface	NA	OSP			
Substrate Panel Singulation Method	NA	Saw singulation			
Solder Ball Composition	98.25SN/1.2AG/0.5CU/0.05NI			96.45SN/3.0AG/0.5CU	
Solder Ball Diameter	0.250mm				0.350mm
Solder Ball Pitch (mm)	0.4		0.5	0.65	
Die Header Material	NA	EPP Substrate			solid core
Operating Supply Voltage Range	1.14-1.26 V				
Operating Temperature Range, Ta	-40oC to +100oC				
Operating Frequency Range	(see datasheet)				
LUTs	5936				
sysMEM Blocks (9kb)	20				

Part Attributes	LIF-MD6000				
	UWG36	UMG64	MG81	JMG80	KMG80
Embedded Memory (kb)	180				
Distributed RAM Bits (kb)	47				
General Purpose PLL	1				
Embedded I2C	2				
Oscillator (10KHz)	1				
Oscillator (48KHz)	1				
Hardened MIPI D-PHY	1	2*			
I/O	17	29	37	37	37
Core Voltage	1.2V				

* Additional D-PHY Rx interfaces are available using programmable I/O.

2.0 LATTICE PRODUCT QUALIFICATION PROGRAM

Lattice Semiconductor Corp. maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, the continued high reliability of Lattice products is assured through ongoing monitor programs as described in Lattice Semiconductor's Reliability Monitor Program Procedure (Doc. #101667). All product qualification plans are generated in conformance with Lattice Semiconductor's Qualification Procedure (Doc. #100164) with failure analysis performed in conformance with Lattice Semiconductor's Failure Analysis Procedure (Doc. #100166). Both documents are referenced in Lattice Semiconductor's Quality Assurance Manual, which can be obtained upon request from a Lattice Semiconductor sales office. Figure 2.0.1 shows the Product Qualification Process Flow.

If failures occur during qualification, an 8D process is used to find root cause and eliminate the failure mode from the design, materials, or process. The effectiveness of any fix or change is validated through additional testing as required. Final testing results are reported in the qualification reports.

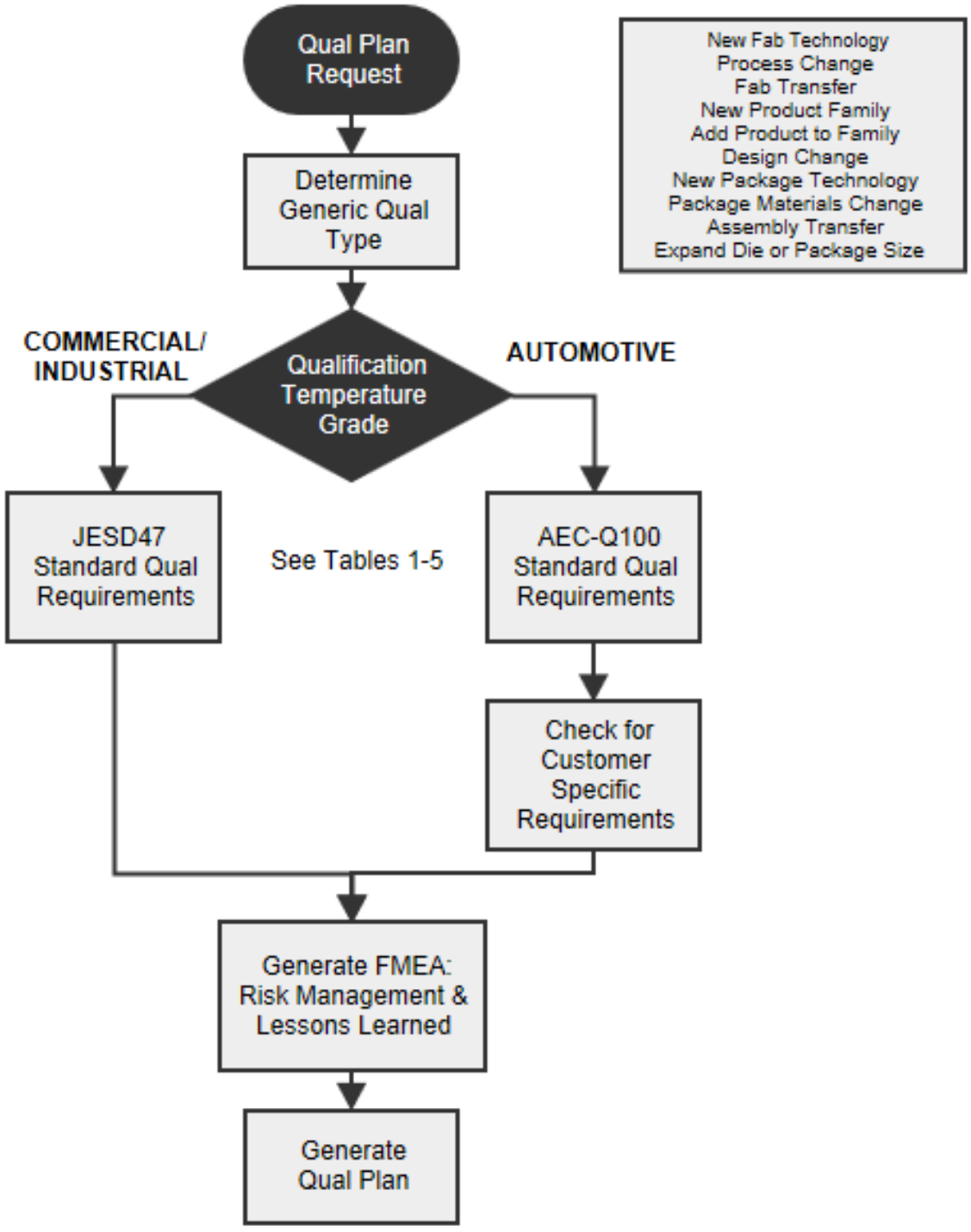
Product families are qualified based upon the requirements outlined in Table 2.0.1. In general, Lattice Semiconductor follows the current JEDEC Solid State Technology Association JESD47 Stress-Based Qualification testing methods. Package family qualification will include products with a wide range of circuit densities, package types, and package lead counts. Major changes to products, processes, or vendors require additional qualification before implementation in production.

CrossLink is fabricated at United Microelectronics Corporation (UMC) and United Semiconductor Japan Corporation (USJC) using a 40nm technology node (LP40-9M).

Lattice Semiconductor maintains a regular reliability monitor program. The current Lattice Reliability Monitor Report can be found at Product Reliability Monitor Report.

Figure 2.0.1 Lattice Standard Product Qualification Process Flow

This diagram represents the standard qualification flow used by Lattice to qualify new Product Families. The target end market for the Product Family determines which flow options are used. The CrossLink Product Family was qualified using the Commercial / Industrial Qualification Option.



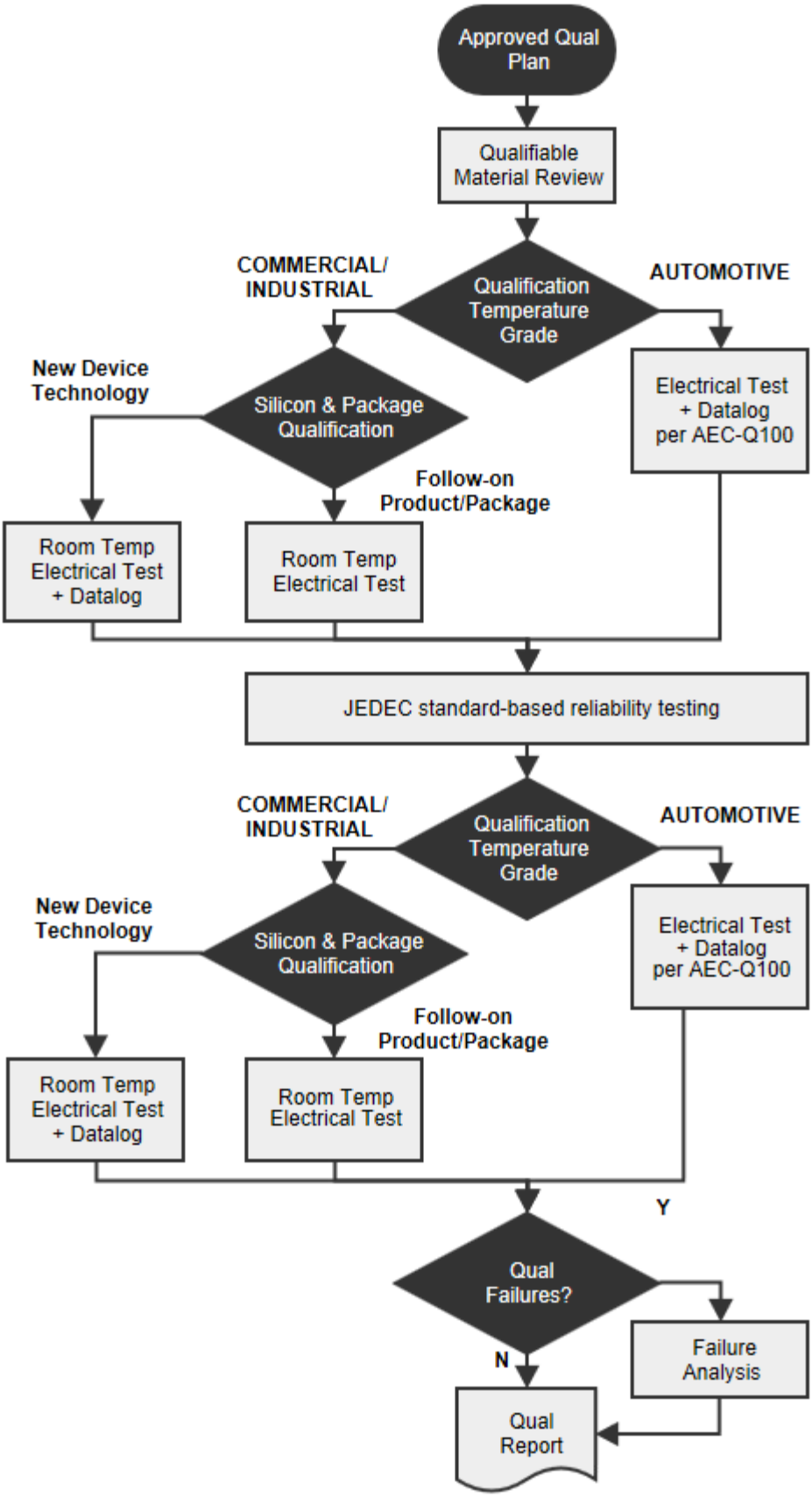

Approved Qual Plan
Qualifiable Material Review
COMMERCIAL/ INDUSTRIAL
Qualification Temperature Grade
AUTOMOTIVE
New Device Technology
Silicon & Package Qualification
Follow-on Product/Package
Electrical Test + Datalog per AEC-Q100
Room Temp Electrical Test + Datalog
Room Temp Electrical Test
JEDEC standard-based reliability testing
COMMERCIAL/ INDUSTRIAL
Qualification Temperature Grade
AUTOMOTIVE
New Device Technology
Silicon & Package Qualification
Follow-on Product/Package
Electrical Test + Datalog per AEC-Q100
Room Temp Electrical Test + Datalog
Room Temp Electrical Test
Y
Qual Failures?
N
Failure Analysis
Qual Report

Table 2.0.1 Typical Qualification Tests for Components in Non-Hermetic Packages

TEST	STANDARD	TEST CONDITIONS
High Temperature Operating Life (HTOL)	JESD22-A108	≥125°C Tj and max operating supplies
ESD: Human Body Model (HBM)	JS-001-2014	25°C (Technology/Device dependent Performance Targets)
ESD: Charged Device Model (CDM)	JS-002-2014	25°C (Technology/Device dependent Performance Targets)
Latch-Up (LU)	JESD78	Class II, +/-100mA trigger current and AMR operating supplies
Accelerated Soft Error Testing (ASER)	JESD89	25°C, Nominal operating supplies
Surface Mount Pre-conditioning (SMPC)	IPC/JEDEC J-STD-020	Per appropriate MSL level per J-STD-020
High Temp Storage Life (HTSL)	JESD22-A103	Condition B
Temperature Cycling (TC)	JESD22-A104	Condition B, soak mode 2 (typical)
Temperature Humidity Bias, THB (85/85) or Biased HAST (HAST)	JESD22-A101 JESD22-A110	85°C, 85 % RH, max operating supplies or 110°C, 85 % RH, max operating supplies or 130°C, 85 % RH, max operating supplies
Unbiased Temperature/Humidity (UHAST)	JESD22-A118	110°C, 85 % RH or 130°C, 85 % RH

3.0 QUALIFICATION DATA CROSSLINK PRODUCT FAMILY

Crosslink is fabricated at UMC and USJC using 40nm technology and assembled/tested at Advanced Semiconductor Engineering, Kaohsiung (ASET). The LIF-MD6000-MG81 is the lead product qualification vehicle for this family.

Product Family: LIF-MD6000

Packages offered: csfBGA

Process Technology Node: 40 nm

3.1 CrossLink Product Family Life (HTOL) Data

High Temperature Operating Life (HTOL) Test

The High Temperature Operating Life test is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. Consistent with EIA/JESD22-A108E "Temperature, Bias, and Operating Life", a pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at specified voltages as described in test conditions for each device type.

CrossLink Life Test (HTOL) Conditions:

Stress Duration: 1000 hours

Stress Conditions: CrossLink: HTOL Pattern, Vcc=1.32V (AMR), Vccio=3.63V, $T_{JUNCTION} = \geq 125°C$

Method: EIA/JESD22-A108E

Table 3.1.1 CrossLink Product Family Life Results

Product Name	Foundry	Lot #	Qty	48 Hrs Result	168 Hrs Result	500 Hrs Result	1000 Hrs Result	Cumulative Hours
LIF-MD6000	UMC	1	100	N/A	0	0	0	100,000
LIF-MD6000	UMC	2	100	N/A	0	0	0	100,000
LIF-MD6000	UMC	3	100	N/A	0	0	0	100,000
LIF-MD6000	UMC	4	85	N/A	0	0	0	85,000
LIF-MD6000	UMC	5	85	N/A	0	0	0	85,000
LIF-MD6000	UMC	6	84	N/A	0	0	0	84,000
LIF-MD6000	USJC	1	100	N/A	0	0	0	100,000

Crosslink HTOL Cumulative Result / Sample Size = 0 / 654
Crosslink Cumulative Life Testing Device Hours = 654,000
Crosslink Long Term Failure Rate < 20.0 FITs
Crosslink FIT Assumptions: CL=60%, Ea=0.7eV, Tjref=55C

3.2 CrossLink Product Family – ESD and Latch UP Data

Electrostatic Discharge-Human Body Model

CrossLink product family was tested per the JS-001-2014 Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) procedure.

All units were Class tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.2.1 CrossLink ESD-HBM Data

Product	36 WLCSP ($2.535x2.583mm^2$, 0.4mm pitch)	64 ucfBGA ($3.5.5x.3.5mm^2$, 0.5mm pitch)	81 csfBGA ($4.5x4.5mm^2$, 0.5mm pitch)	80 ctfBGA ($6.5x6.5mm^2$, 0.65mm pitch)	80 ckfBGA ($7x7mm^2$, 0.65mm pitch)
LIF-MD6000	HBM ≥ 2kV Class 2	HBM ≥ 2kV Class 2	HBM ≥ 2kV Class 2	HBM ≥ 2kV Class 2	HBM ≥ 2kV Class 2

HBM classification for Commercial/Industrial products per JS-001-2014.
All HBM levels indicated are dual-polarity (±).
HBM worst-case performance is the package with the smallest RLC parasitics. All other packages for a given product are qualified-by-similarity (QBS).

Electrostatic Discharge-Charged Device Model:

CrossLink product family was tested per the JESD22-C101F, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components procedure.

All units were Class tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.2.2 CrossLink ESD-CDM Data

Product	36 WLCSP ($2.535x2.583mm^2$, 0.4mm pitch)	64 ucfBGA ($3.5.5x.3.5mm^2$, 0.5mm pitch)	81 csfBGA ($4.5x4.5mm^2$, 0.5mm pitch)	80 ctfBGA ($6.5x6.5mm^2$, 0.5mm pitch)	80 ckfBGA ($7x7mm^2$, 0.65mm pitch)
LIF-MD6000	CDM ≥ 1kV Class IV(A)	CDM ≥ 1kV Class C3	CDM ≥ 1kV Class C3	CDM ≥ 500V Class C2 (B)	CDM ≥ 500V Class C2

CDM classification for Commercial/Industrial products, per (A) EIA/JESD22-C101E, (B) also passing 750V on corner pins, 500V on all other pins per AEC-Q100-011C1 C4B; All others, passing per EIA/JESD22-C101F.
All CDM levels indicated are dual-polarity (±).
CDM worst-case performance is the package with the largest bulk capacitance. All other packages for a given product are qualified-by-similarity (QBS).

Latch-Up:

CrossLink product family was tested per the JESD78D IC Latch-up Test procedure.

All units were Class tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.2.3 CrossLink I/O Latch Up >100mA @ HOT (105°C) Data

Product	36 WLCSP (2.535x2.583mm², 0.4mm pitch)	64 ucfBGA (3.5.5x.3.5mm², 0.5mm pitch)	81 csfBGA (4.5x4.5mm², 0.5mm pitch)	80 ctfBGA (6.5x6.5mm², 0.5mm pitch)	80 ckfBGA (7x7mm², 0.65mm pitch)
LIF-MD6000	> ±100mA ClassII	> ±100mA ClassII	> ±100mA ClassII	> ±100mA ClassII	> ±100mA ClassII

I-Test LU classification for Commercial/Industrial products, per JESD78D.
All IO-LU levels indicated are dual-polarity (±).
IO-LU worst-case performance is the package with access to the most IOs. All other packages for a given product are qualified-by-similarity (QBS).

Table 3.2.4 CrossLink Vcc Latch Up >1.5X @ HOT (105°C) Data

Product	36 WLCSP (2.535x2.583mm², 0.4mm pitch)	64 ucfBGA (3.5.5x.3.5mm², 0.5mm pitch)	81 csfBGA (4.5x4.5mm², 0.5mm pitch)	80 ctfBGA (6.5x6.5mm², 0.5mm pitch)	80 ckfBGA (7x7mm², 0.65mm pitch)
LIF-MD6000	> 1.5x Vcc ClassII	> 1.5x Vcc ClassII	> 1.5x Vcc ClassII	> 1.5x Vcc ClassII	> 1.5x Vcc ClassII

Vsupply Over-voltage Test LU classification for Commercial/Industrial products, per JESD78D.
Vcc-LU worst-case performance is the package with access to the most individual power rails. All other packages for a given product are qualified-by-similarity (QBS).

3.3 Accelerated Soft Error Rate (ASER)

Soft Error Rate (SER) testing is conducted to characterize the sensitivity of SRAM memory elements to Atmospheric Neutron and Alpha Particle radiation. Charge induced by the impact of these particles can collect at sensitive nodes in the device and result in changes to the internal states of the device. While these changes do not cause physical damage to the device, they can cause errors in device operation.

Neutron SER – The normalized upset rate of Configuration RAM and Embedded Block RAM (EBR) memories due to neutron events. During testing, devices were configured with a memory pattern, exposed to an accelerated neutron environment, and the memory was read back from the device. Upset bits were identified through pattern comparison. Neutron testing results are normalized to the standard neutron flux for New York City at sea level: 14 n/cm^2/hr. The SER is represented in Failures in Time per million bits (FIT/Mb) to allow for translation across different device families and densities.

Alpha Particle SER – The normalized upset rate of Configuration RAM and Embedded Block RAM (EBR) memories due to alpha particle events. During testing, devices were configured with a memory pattern, exposed to a calibrated alpha source (Am-241), and the memory was read back from the device. Upset bits were identified through pattern comparison. Alpha particle testing results are normalized to a standard flux for Ultra Low Alpha (ULA) packaging materials: 0.001 alpha/cm^2/hr. The SER is represented in Failures in Time per million bits (FIT/Mb) to allow for translation across different device families and densities.

Table 3.3.1 40LP-SA (40nm) SER

Particle Type	Memory	SER (FIT/Mb)
Neutron	Configuration RAM	176.2
	EBR	262.9
Alpha Particle	Configuration RAM	152.8
	EBR	346.8

Note: Detailed SER reports are available upon request.

4.0 PACKAGE QUALIFICATION DATA FOR CROSSLINK PRODUCT FAMILY

The CrossLink devices are assembled and tested at Advanced Semiconductor Engineering, Kaohsiung Taiwan (ASET). Package qualification tests include Surface Mount Pre-Conditioning (SMPC), Temperature Cycling (T/C), Biased HAST (BHAST), Unbiased HAST (UHAST) and High Temperature Storage (HTSL). Electrical test is performed pre- and post-stress. Mechanical evaluation tests include Scanning Acoustic Tomography (SAT) and Visual Package Inspection.

Table 4.0.1 Summary of Package Reliability Test Conditions and Results

Assembly Site	Test	Stress Conditions	Test Vehicle	Package Type	Lot Quantity	Cumulative Device Units/Hours/Cycles	# of Fails
ASET	SMPC	3x 260°C reflow	LIF-MD6000	81-csfBGA	8	2,577 units	0
				64-ucfBGA	4	1,695 units	0
				80-ctfBGA	3	1,401 units	0
				80ckfBGA	6	2,730 units	0
				36-WLCSP	3	1,497 units	0
ASET	TC	-55°C to 125°C	LIF-MD6000	81-csfBGA	7	446,600 cycles	0
				64-ucfBGA	4	215,600 cycles	0
				80-ctfBGA	3	462,000 cycles	0
				80ckfBGA	6	161,700 cycles	0
				36-WLCSP	3	231,000 cycles	0
ASET	BHAST/ THB	85%RH, 110°C, 264 hours	LIF-MD6000	81-csfBGA	8	162,624 hours	0
				64-ucfBGA	3	609,84 hours	0
		85%RH, 85°C, 1000 hours		64-ucfBGA	1	77,000 hours	0
		85%RH, 110°C, 264 hours		80-ctfBGA	3	60,984 hours	1
		85%RH, 85°C, 1000 hours		80ckfBGA	3	231,000 hours	2
		85%RH, 130°C, 96 hours		36-WLCSP	3	221,76 hours	1
ASET	UHAST	85%RH, 110°C, 264 hours	LIF-MD6000	81-csfBGA	8	162,624 hours	0
				64-ucfBGA	4	81,312 hours	0
				80-ctfBGA	3	60,984 hours	0
				80ckfBGA	3	60,984 hours	0
		85%RH, 130°C, 96 hours		36-WLCSP	3	22,176 hours	0
ASET	HTSL	150°C, 1000 hours	LIF-MD6000	81-csfBGA	4	308,000 hours	0
				64-ucfBGA	4	212,000 hours	0
				80-ctfBGA	3	135,000 hours	0
				80ckfBGA	3	135,000 hours	0
				36-WLCSP	3	135,000 hours	0

4.1 Surface Mount Preconditioning Testing

The Surface Mount Preconditioning (SMPC) Test is used to model the surface mount assembly conditions during component solder processing. All devices stressed through High Temperature Storage, Temperature Cycling, Un-biased HAST and Biased HAST were preconditioned. This preconditioning is consistent with J-STD-020D and JEDEC JESD22-A113F "Preconditioning Procedures of Plastic Surface Mount Devices Prior to Reliability Testing".

Surface Mount Preconditioning: (5cyc TC condition B, 24 hours bake @ 125°C; 30°C/60% RH soak for 192 hours (MSL3) or 85°C/85% RH soak for 168 hours (MSL1); 3X passes of reflow simulation) performed before all package stresses.

MSL3 Packages: csfBGA

MSL1 Packages: WLCSP

Method: J-STD-020D and JESD22-A113F

Table 4.1.1 Surface Mount Precondition Data

PRODUCT NAME	FOUNDRY	PACKAGE	ASSY SITE	LOT	MOISTURE SOAK LEVEL	3x REFLOW TEMP	QTY	FAIL
LIF-MD6000	UMC	UWG36	ASET	1	1	260°C	499	0
				2			499	0
				3			499	0
	UMC	UMG64		1	3		419	0
				2			419	0
				3			419	0
	USJC			4			438	0
	UMC	MG81		1			423	0
				2			423	0
				3			423	0
				4			239	0
				5			239	0
				6			239	0
				7			170	0
				8			421	0
	UMC	JMG80		1			467	0
				2			467	0
				3			467	0
	UMC	KMG80		1			430	0
				2			430	0
				3			430	0
				4			480	0
				5			480	0
				6			480	0

Cumulative SMPC Failure Rate = 0 / 9,900

4.2 Temperature Cycling (TC)

The Temperature Cycling test is used to accelerate those failures resulting from mechanical stresses induced by differential thermal expansion of adjacent films, layers and metallurgical interfaces in the die and package. Devices are tested at 25°C after exposure to repeated cycling between -55°C and +125°C in an air environment consistent with JEDEC JESD22-A104D “Temperature Cycling”, Condition B temperature cycling requirements. Prior to Temperature Cycling testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: csfBGA

MSL1 Packages: WLCSP

Stress Duration: 700 cycles, 1000cycles

Stress Conditions: Temperature cycling between -55°C to 125°C

Method: JESD22-A104D, Condition B

Table 4.2.1 Temperature Cycling Data

PRODUCT NAME	FOUNDRY	PACKAGE	ASSY SITE	LOT	STRESS TEMP	STRESS DURATION (cycles)	QTY	FAIL
LIF-MD6000	UMC	UWG36	ASET	1	-55°C to 125°C	1000	77	0
				2			77	0
				3			77	0
	UMC	UMG64		1		700	77	0
				2			77	0
				3			77	0
	USJC			1			77	0
	UMC	MG81		1		1000	77	0
				2			77	0
				3			77	0
				4		700	77	0
				5			77	0
				6			77	0
				7			77	0
	UMC	JMG80		1		1000	77	0
				2			77	0
				3			77	0
	UMC	KMG80		1			77	0
				2			77	0
				3			77	0
				4		700	77	0
				5			77	0
				6			77	0

Cumulative Temp Cycle Failure Rate = 0 / 1,771
Cumulative Device Temp Cycles = 1,516,900

4.3 Biased Highly Accelerated Temperature and Humidity Stress Test (BHAST) or Steady-State Temperature Humidity Bias Life Test (THB)

Highly Accelerated Stress Test (HAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The BHAST test is used to accelerate threshold shifts in the MOS device associated with moisture diffusion into the gate oxide region as well as electrochemical corrosion mechanisms within the device package. Consistent with JEDEC JESD22-A110 “Highly-Accelerated Temperature and Humidity Stress Test”, the biased HAST conditions are either 96 hours exposure at 130°C and 85% relative humidity, or 264 hours exposure at 110°C and 85% relative humidity.

Steady-State Temperature Humidity Bias Life Test (THB) uses temperature, humidity and bias, minus the pressure, to accelerate the penetration of moisture through the external protective material or along the interface between the external protective material and the metallic conductors that pass through. The stress usually activates the same failure mechanism as BHAST but with a lower acceleration factor, hence, units are subjected to a longer stress time of 1000 hours at 85°C and 85% relative humidity, consistent with JEDEC JESD22-A101 “Steady-State Temperature Humidity Bias Life Test”.

Prior to BHAST or THB, all Pb-free wirebonded devices are subjected to Surface Mount Preconditioning. This is a relatively new requirement consistent with JESD47 for Pb-free, wirebonded packages (WLCSP packages not included).

MSL3 Packages: csfBGA

MSL1 Packages: WLCSP

Stress Conditions: Vcc= Max operating condition and 130°C or 110°C and 85% RH (BHAST) or 85°C and 85% RH (THB)

Stress Duration: 96 Hrs, 264 Hrs or 1000 Hrs respectively

Method: JESD22-A110E

Table 4.3.1 Biased HAST and THB Data

PRODUCT NAME	FOUNDRY	PACKAGE	ASSY SITE	LOT	STRESS TEMP	STRESS DURATION (hours)	QTY	FAIL
LIF-MD6000	UMC	UWG36	ASET	1	130°C	96	77	0
				2			77	0
				3			77	1[1]
	UMC	UMG64		1	110°C	264	77	0
				2			77	0
				3			77	0
	USJC			4	85°C	1000	77	0
	UMC	MG81		1	110°C	264	77	0
				2			77	0
				3			77	0
				4			77	0
				5			77	0
				6			77	0
				7			77	0
				8			77	0
	UMC	JMG80		1			77	0
				2			77	1[2]
				3			77	0
	UMC	KMG80		1	85°C	1000	77	0
				2			77	1[3]
				3			77	1[4]

Cumulative BHAST Failure Rate = 4 / 1,540
Cumulative BHAST Device Hours = 537,768
Cumulative THB Failure Rate = 0 / 77
Cumulative THB Device House = 77,000

[1] FAR# LI1709028 - idcode_sspi. Failure is non-assembly related.
[2] FAR# LI1709044 – Laser groove-induced die delamination. Corrective/Preventive action in place.
[3] FAR# LI1807052 – Laser groove-induced die cracking. Corrective/Preventive action in place.
[4] FAR# LI1807003 – Potential random metal stringer-induced shorts at assembly. Failure is attributed to baseline/random assembly issues.

4.4 Unbiased HAST

Unbiased Highly Accelerated Stress Test (UHAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Unbiased HAST test is designed to detect ionic contaminants present within the package or on the die surface, which can cause chemical corrosion. Consistent with JESD22-A118B, “Accelerated Moisture Resistance - Unbiased HAST,” the UHAST conditions are 264 hours exposure at 110°C and 85% relative humidity. Prior to Unbiased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: csfBGA
MSL1 Packages: WLCSP
Stress Conditions: 110°C (csfBGA)/130°C (WLCSP), and 85% RH
Stress Duration: 264 Hrs (csfBGA)/ 96 Hrs (WLCSP)
Method: JESD22-A118B

Table 4.4.1 Unbiased HAST Data

PRODUCT NAME	FOUNDRY	PACKAGE	ASSY SITE	LOT	STRESS TEMP	STRESS DURATION (hours)	QTY	FAIL
LIF-MD6000	UMC	UWG36	ASET	1	130°C	96	77	0
				2			77	0
				3			77	0
	UMC	UMG64		1	110°C	264	77	0
				2			77	0
				3			77	0
	USJC			4			77	0
	UMC	MG81		1			77	0
				2			77	0
				3			77	0
				4			77	0
				5			77	0
				6			77	0
				7			77	0
				8			77	0
	UMC	JMG80		1			77	0
				2			77	0
				3			77	0
	UMC	KMG80		1			77	0
				2			77	0
				3			77	0

Cumulative UHAST Failure Rate = 0 / 1,617
Cumulative UHAST Device Hours = 388,080

4.5 High Temperature Storage Life

The High Temperature Storage Life test is used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms. Consistent with JEDEC JESD22-A103D, the devices are subjected to high temperature storage Condition B: +150 (-0/+10) °C for 1000 hours. Prior to High Temperature Storage, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: csfBGA
MSL1 Packages: WLCSP
Stress Duration: 1000 hours
Temperature: 150°C (ambient)
Method: JESD22-A-103D

Table 4.5.1 High Temperature Storage Life Data

PRODUCT NAME	FOUNDRY	PACKAGE	ASSY SITE	LOT	STRESS TEMP	STRESS DURATION (hours)	QTY	FAIL
LIF-MD6000	UMC	UWG36	ASET	1	150°C	1000	45	0
				2			45	0
				3			45	0
	UMC	UMG64		1			45	0
				2			45	0
				3			45	0
	USJC			1			77	0
	UMC	MG81		1			77	0
				2			77	0
				3			77	0
				4			77	0
	UMC	JMG80		1			45	0
				2			45	0
				3			45	0
	UMC	KMG80		1			45	0
				2			45	0
				3			45	0

Cumulative HTSL Failure Rate = 0 / 925
Cumulative HTSL Device Hours = 925,000

5.0 REVISION HISTORY

Table 5.0.1 CrossLink Product Family Qualification Summary Revisions

Date	Revision	Change Summary
June 2017	A	Initial document release covering LIF-MD6000-MG81
September 2019	B	Addition of UWG36, UMG64, JMG80 and KMG80 UMC and UMG64 FLM qualification data.
December 2019	C	Update to reflect United Microelectronics Corporation (UMC) purchased Fujitsu Microelectronics Limited (FLM). The new name is United Semiconductor Japan Corporation (USJC)
January 2021	D	Add ASER data

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