

## Introduction

While designing USB 3.1 Type-C solution hardware using LIF-UC devices (LIF-UC110, LIF-UC120, LIF-UC140), designers must pay special attention to the critical hardware requirements. This technical note describes the critical hardware requirements related to the USB 3.1 Type-C solutions. This document does not provide detailed step-by-step instructions, but offers a high-level summary and checklist to assist in the design process.

The LIF-UC ultra-low power and non-volatile devices are available in three versions.

- LIF-UC110 for CD/PD for charger applications
- LIF-UC120 for CD/PD PHY for hosts/devices applications
- LIF-UC140 for CD/PD for hosts/devices applications

*Note: You must be familiar with the features described in DS1052, [Lattice USB Type-C Solution Data Sheet](#) to understand this document.*

The critical hardware areas covered in this technical note includes:

- Power supply related to the LIF-UC devices supply rails and how to connect them to the PCB and the associated system
- Configuration of LIF-UC devices and how to perform the configuration mode selection
- Checklist of the USB 3.1 Type-C interface and critical signals

## Power Supply

VCC (Core Supply Voltage), SPI\_VCCIO1 and VPP\_2V5 determine the stability of the LIF-UC110 and LIF-UC120 devices. VCC, VCCIO\_2, SPI\_VCC and VPP\_2V5 determine the stability of the LIF-UC140 devices. The power supply needs to be at a valid and stable level before the device can become operational. Refer to the family data sheet for specific voltage requirements.

**Table 1. Power Supply Voltage Levels and Description**

Power Supply	Voltage (Nominal Value)	Description
VCC	1.2 V	Core supply voltage
VCCIO_X	3.3 V	Power supply I/O banks
VPP_2V5	2.5 V	NVCM (Non-volatile Configuration Memory) programming and operating supply voltage connected to 3.3V power supply through the diode
VPP_FAST	Unconnected	Optional fast NVCM programming supply
SPI_VCC	3.3 V	SPI interface supply voltage for LIF-UC140
SPI_VCCIO1	3.3 V	SPI interface supply voltage for LIF-UC110 and LIF-UC120
VCCPLL	1.2 V	Analog power supply voltage
GNDPLL	0 V	Analog Power supply GND

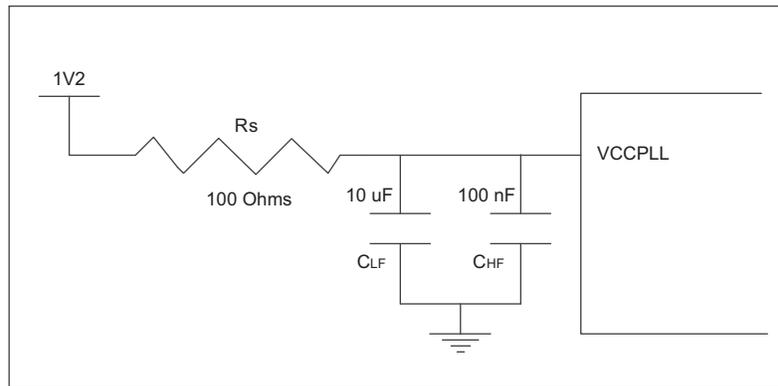
Notes:

- VCCPLL must be tied to VCC when PLL is not in use.
- External power supply filter is required for VCCPLL and GNDPLL.
- VPP\_FAST is not available in LIF-UC110 and LIF-UC120 devices

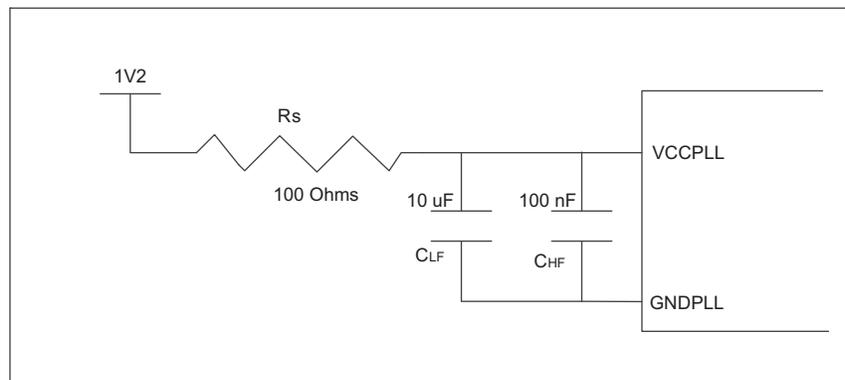
### Analogue Power Supply Filter for PLL

The LIF-UC sysCLOCK™ PLL contains analog blocks. Hence PLL requires a separate power and ground which is quiet and stable to reduce the output clock jitter of the PLL on device with external VCCPLL supply pins. Figure 1 and Figure 2 shows the recommended circuit for isolating PLL supplies.

**Figure 1. LIF-UC110, LIF-UC120 Isolating PLL Supplies**



**Figure 2. LIF-UC140 Isolating PLL Supplies**



### Configuration Considerations

The LIF-UC devices contain two types of memory.

- CRAM (Configuration RAM)
- NVCM (Non-volatile Configuration Memory)

CRAM contains an active configuration. NVCM provides on-chip storage of the configuration data. It is one-time programmable and recommended for a mass-production.

The configuration and programming of the LIF-UC devices from external memory by using the SPI port is in Master and Slave mode. In Master SPI mode, the device configures its CRAM from an external SPI Flash connected to it. In Slave mode, Lattice Diamond® Programmer or embedded processor configures the device.

For the LIF-UC device family, signal on the pin SPI\_SS\_B determines the configuration of LIF-UC.

- SPI\_SS\_B=0 => LIF-UC CRAM is configured from an external SPI
- SPI\_SS\_B=1 => LIF-UC is configured from the NVCM

SPI\_SS\_B pin is sampled after Power-on-Reset (POR) is released or CRESET\_B is held low or toggled (High-Low-High).

**Table 2. Configuration Pins**

Pin Name	Function	Direction	External Termination	Notes
CRESET_B	Configuration Reset, Active Low	Input	Refer to the Schematics section in DS1052, <a href="#">Lattice USB Type-C Solution Data Sheet</a>	A low on CRESET_B delay's configuration
CDONE	Configuration Done output from LIF-UC	Output	Refer to the Schematics section in DS1052, <a href="#">Lattice USB Type-C Solution Data Sheet</a>	
SPI_VCC	SPI interface supply voltage for LIF-UC140	Supply		
SPI_VCCIO1	SPI interface supply voltage for LIF-UC110 and LIF-UC120	Supply		
SPI_SI	SPI serial input to the LIF-UC, in both Master and Slave modes	Input		Released to user I/O after configuration
SPI_SO	SPI serial output from the LIF-UC, in both Master and Slave modes	Output		Released to user I/O after configuration
SPI_SCK	SPI clock	Input/ Output	10 kOhm pull-ups to VCC_SPI or SPI_VCCIO1 are recommended	Direction based on Master or Slave modes Released to user I/O after configuration
SPI_SS_B	Chip select	Input (Slave mode)/ Output (Master mode)	10 kOhm pull-ups to VCC_SPI or SPI_VCCIO1 in Master mode and 10 kOhm pull-down in Slave mode	

## IOs as Weak Pulled-Up During Configuration

During configuration, Lattice device IO pins are weak pulled-up for a time duration of 40 ms to 70 ms. Customers should design their circuit considering this IO behavior.

## Checklist

**Table 3. USB Type-C Hardware Checklist**

Sr. No	USB 3.1 Type-C Hardware Checklist	OK	N/A
1	<b>Power Supply</b>		
1.1	Core supply VCC at 1.2 V		
1.2	I/O Power Supply VCCIO 0-3 at 3.3 V		
1.3	SPI_VCC at 3.3 V		
1.4	SPI_VCCIO1 at 3.3 V		
1.5	VCCPLL pulled to VCC even if PLL is not used		
1.6	Power supply filter for VCCPLL and GNDPLL		
1.7	GNDPLL must NOT be connected to the board		
2	<b>Power-On-Reset (POR) Inputs</b>		
2.1	VCC		
2.2	SPI_VCC or SPI_VCC101		
2.3	VCCIO_0-3		
2.4	VPP_2V5		
2.5	VPP_FAST		
3	<b>Configuration</b>		
3.1	Configuration mode based on SPI_SS_B		
3.2	Pull-up on CRESET_B, CDONE pin		
4	<b>IO Pin Assignment</b>		
4.1	LVDS pin assignment considerations		
5	<b>Type-C Hardware Requirements</b>		
5.1	IO Pins are weak Pulled-up during configuration		
5.2	CC1_RP and CC2_RP resistor value — 36 kOhms + or - 20% pull up to 3.3 V for advertising Default USB current — 12 kOhms + or - 5% pull up to 3.3 V for advertising 1.5 A USB current — 4.7 kOhms + or - 5% pull up to 3.3 V for advertising 3.0 A USB current		
5.3	CC1_RD and CC2_RD resistor value 5.1 kOhms		
5.4	VCONN_5V Supply at 5 V		
5.5	Resistor value tolerance should be as per BOM		
5.6	Capacitor value tolerance can be + or – 10% and voltage rating should be two times of operating supply		
5.7	Source and Drain connections of CC line protection MOSFETs		
5.8	Pull-up Resistors for RGB0, RGB1 and RGB2		
5.9	VBUS resistor divider values should calculate according to VBUS voltage.		

## Technical Support Assistance

Submit a technical support case through [www.latticesemi.com/techsupport](http://www.latticesemi.com/techsupport).

## Revision History

Date	Version	Change Summary
July 2015	1.1	Updated <a href="#">Introduction</a> section. Revised list of critical hardware areas covered in this technical note.
		Updated <a href="#">Analogue Power Supply Filter for PLL</a> section. — Changed 100 W to 100 Ohms in Figure 1, LIF-UC110, LIF-UC120 Isolating PLL Supplies and Figure 2, LIF-UC140 Isolating PLL Supplies.
		Updated <a href="#">Checklist</a> section. — Formatted checklist headings in Table 3, USB Type-C Hardware Checklist. — Merged and revised CC1_RP and CC2_RP resistor value. — Revised 5.5 Resistor value tolerance.
June 2015	1.0	Initial release.