Lattice USB Type-C Solution

October 2016 Reference Design RD1209

Introduction

The USB Type-C receptacle, plug and cable provide a smaller, thinner and more robust alternative to existing USB interconnect. This new solution targets use in a variety of platforms, ranging from notebooks, PCs and monitors to smartphones and tablets, where existing Standard-A and Micro-AB receptacles are deemed too large, difficult to use, or inadequately robust. The USB Type-C plug enhances ease of use by being pluggable in either upside-up or upside-down directions and in either direction between host and devices. Determination of this host-to-device relationship is accomplished through a Configuration Channel (CC) that is connected through the cable.

These various solutions demonstrate the capabilities of the Lattice device as USB 3.1 Power Delivery and Type-C ASSP. The solution include a DRP (dual-role port) function, hence it can be used as both DFP/Host/Source and UFP/Device/Sink after role resolution.

One of the most important features of USB Type-C is the reversible nature of the connector and plug. This design also provides the provision to control a Super Speed switch required for data channel alignment/orientation management. Lattice PD controller can control both the SS (Super Speed Switch) and the HS (High Speed Switch) providing a seamless interface with Type C connector without any intervention from the main processor.

The USB PD specifications have another exciting functional extension using the Type-C connector known as Alternate Modes. Lattice PD controller provides support for Structured VDM (Vendor Defined Messages) to handle these alternate modes like VESA Display Port over Type-C.

This document is based on *Universal Serial Bus Power Delivery Specification revision 2.0 version 1.0* and *Universal Serial Bus Type-C Cable and Connector Specification revision 1.1*. Any references in this document to the PD specification and Type-C specification should be understood.

Features

- Two solutions cover majority of USB Type-C Power Delivery (PD) and Cable Detect (CD) applications:
  - — CD/PD for charger
  - — CD/PD for hosts/device
- Logical based PHY provides fast deterministic response and low power, typical solution power is 7 mW
- Standby power less than 100 uW
- Support for fast development
  - — Industry proven solutions reduce design risk
  - — Schematics and BOMs available to minimize system design effort
- Wide range of packages to match PCB technology
  - — 48 QFN
  - — 81 ucBGA
- Ultra-small form factor, as small as 2.078 mm X 2.078 mm
- USB Type-C Cable Detect (CD) support per USB Cable and Connector Specification
- USB Power Delivery (PD) support per Power Delivery Specification

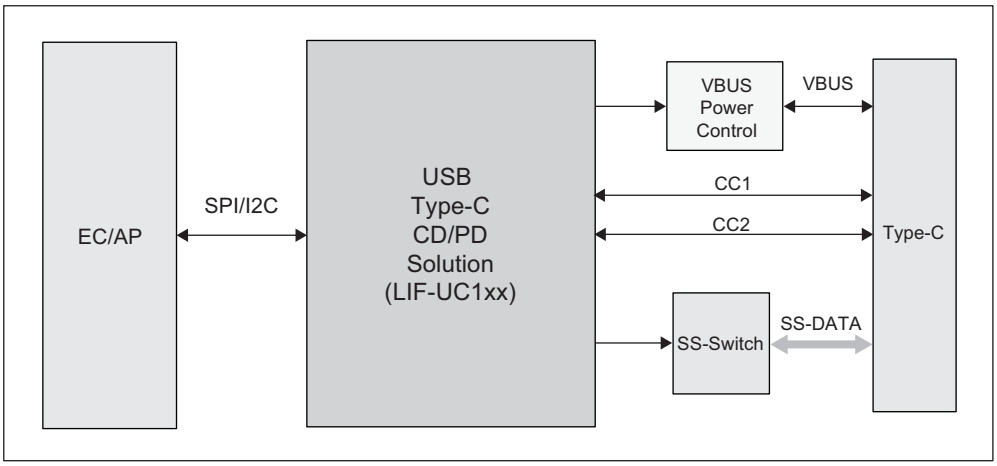
Table 1. USB Type-C Device Table

Solution	Package, Ball Pitch, Dimension	Typical End Application	OPN
CD/PD for Charger	48 QFN, 0.50 mm, 7.00 mm x 7.00 mm	Charger	LIF-UC110-SG48I
CD/PD for Hosts/Devices	81 ucBGA, 0.40 mm, 4.00 mm x 4.00 mm	Tablet	LIF-UC140-CM81I

System Block Diagram

Figure 1 shows the system block diagram of the USB Type-C Solution.

Figure 1. Block Diagram



Specifications

The design consists of the specifications described in this section.

Recommended Operating Conditions

See DS1052, Lattice USB Type-C Solution Data Sheet.

Power Supply Ramp Rates

See DS1052, Lattice USB Type-C Solution Data Sheet.

Power-on-Reset Voltage Levels

See DS1052, Lattice USB Type-C Solution Data Sheet.

ESD Performance

See DS1052, Lattice USB Type-C Solution Data Sheet.

DC Electrical Characteristics

See DS1052, Lattice USB Type-C Solution Data Sheet.

Power Supply Current

See DS1052, Lattice USB Type-C Solution Data Sheet.

Absolute Maximum Ratings

See DS1052, Lattice USB Type-C Solution Data Sheet.

Signal Descriptions

Table 2. Signal Descriptions

Signal Name	Type	Description
CLK_IN	I	5 MHz Reference Clock
EC_SCL	I/O	I^2C Serial Clock
EC_SDA	I/O	I^2C Data
EC_INT	O	Interrupt signal from FPGA to EC
EC_CS	I	Chip select signal from EC to FPGA
VSEL1,VSEL2,VSEL3,VSEL4	I/O	Voltage selection lines for selecting output voltages
SS_SEL1,SS_SEL2,SS_SEL3, SS_SEL4	O	SS/HS Switch Control Signal
VBUS_SOURCE_EN	O	Enable Signal for V_{BUS} Source
VBUS_SINK_EN	O	Enable Signal for V_{BUS} Sink
VBUS_DSICHARGE_EN	O	Enable Signal for V_{BUS} Discharge
VCC	I	1.2 V Core Supply
VCCIO	I	3.3 V/1.8 V IO Power Supply
VBUS	I	V_{BUS}
GND	I	Ground

See DS1052, Lattice USB Type-C Solution Data Sheet for detailed signal descriptions.

Electrical Requirements and Lattice Implementation Models

Lattice CD/PD controller implements the USB Power Delivery over USB Type-C. There are many requirements starting from successful detection to the final explicit contract. Based on the USB Type-C specification, there are two major electrical events between attach, negotiate and explicit contract states. The following sections will show the functional models of the approach used while implementing the Lattice CD/PD controller solution.

Cable Attach/Detach Determination

Cable attach and detach detection is the basic requirement of any Type-C port. The USB Type-C specification defines the process that has to be followed to detect these events along with the role information to be extracted based on the CC line voltage for a DFP and the presence of V_{BUS} in case of a UFP.

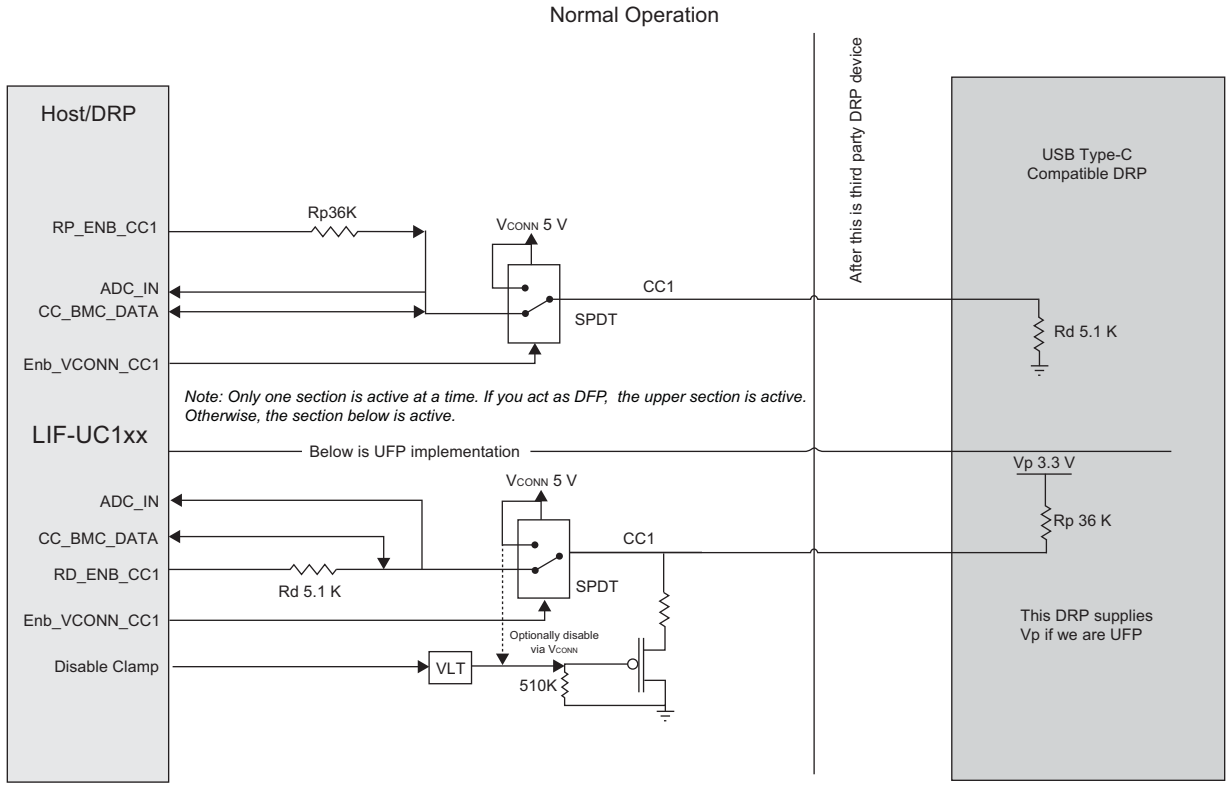
Lattice CD/PD controller is a Dual-Role Port (DRP) hence it needs the capability to detect the presence of both the R_P/R_D resistors (i.e. vRd) as well as V_{BUS}. Apart from detecting the port partner R_P/R_D, the logic should also be able to assert and de-assert its on RP and RD during the role-resolution phase.

Normal Mode Rp/Rd Functional Model

This model shows the implementation of Rp and Rd resistor based device detection method. This is just for illustration purpose and does not include the CC2 line. Under normal operation, the device is either a DFP or a UFP based on the resistors used in the device frontend.

- **DFP Detection** – A DFP device exposes a Rp resistor pulled up to Vp which in this case is 3.3 V always. This is done by driving ‘1’ on the “Rp_ENB_CC1” signal.
- **UFP Detection** – A UFP shall expose Rd resistor pulled down to Gnd in order to get detected by a DFP. This is done by driving ‘0’ on the “Rd_ENB_CC1” signal which acts as a pseudo ground when driven low.
- Once the DFP detects the UFP via the specification defined vRd on the CC line, it will turn ON its VBUS _SOURCE.
- The UFP will then detect the presence of this voltage on the V_{BUS} line and complete the connection.

Figure 2. R_P and R_D Functional Model for a DRP-DRP



Dead Battery Detection/Unpowered Port Detection

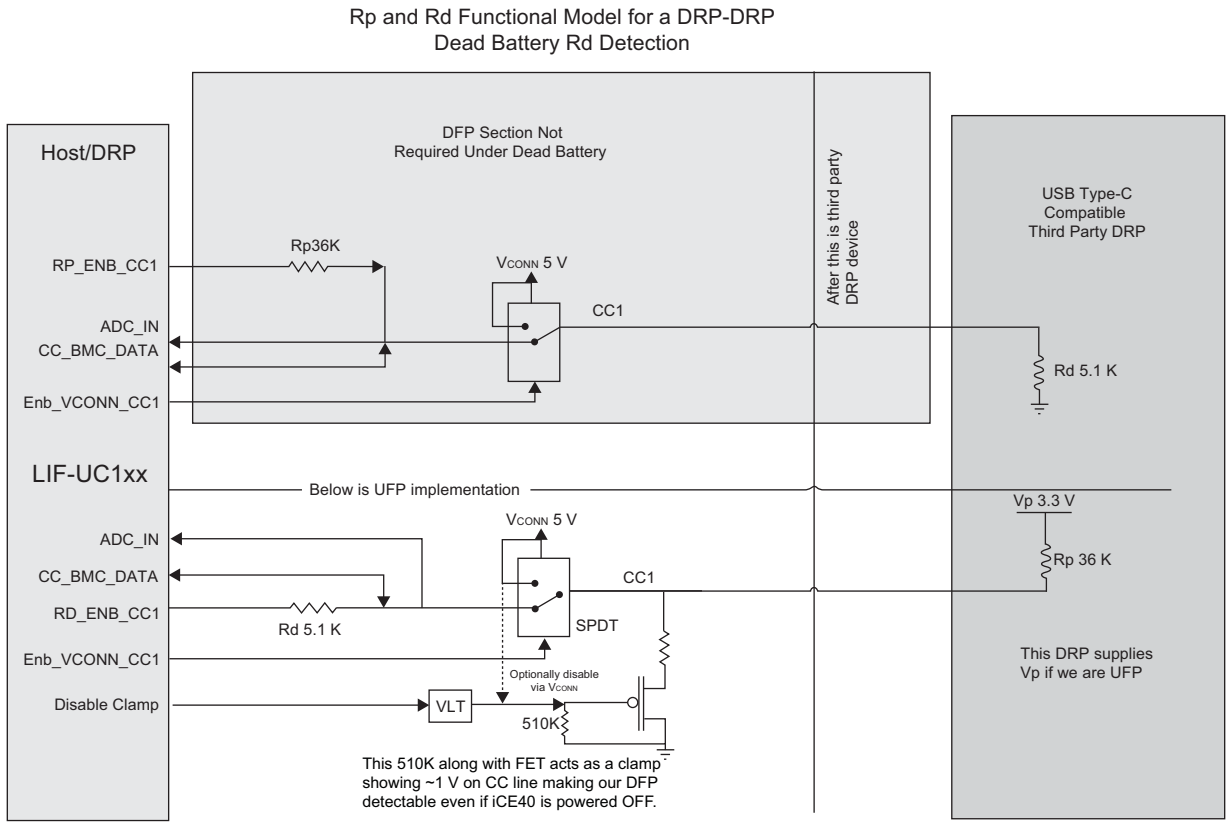
The Power Delivery specification provides a mechanism for a USB Device to provide power to a USB Host under the circumstances where the USB Host:

- Has a Dead Battery that requires charging
- Has lost its power source
- Does not have a power source
- Does not want to provide power

The USB Peripheral primarily acts as a USB Device that may also provide power to the USB Host if the correct detection is carried out. Lattice CD/PD controller has a provision to be able to expose pull down resistor on both CC lines so that it is detected as a Device with no power by the port partner and hence will be provide V_{BUS} to get the power for device operation.

Dead Battery/Lattice Device OFF Functional Model

Figure 3. Clamp Voltage Based Device Detection for a Dead Battery/Unpowered Device



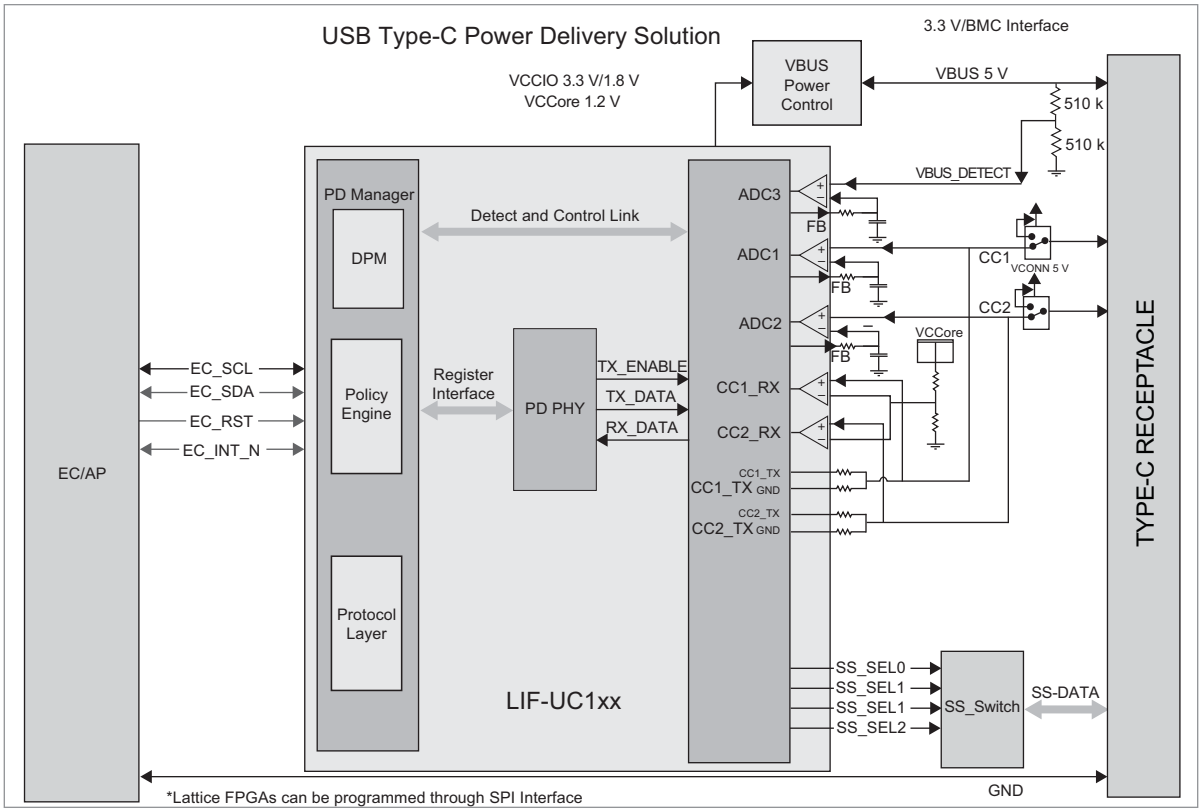
This model is an illustration of how the design handles the use case when the Lattice device is unable to turn ON and thus cannot drive the Gates of the FET operating in the switching mode. If the DRP has no power, it should expose the Rd resistors in order to be detected by the far end DRP as a Sink. To achieve this, the design has a PFET with the Gate pulled to GND line. This enables enough vClamp (~1 V) on the CC line, which leads to the detection of LIF-UC1xx as a Sink DRP and the port partner (source) starts providing the V_{BUS}. This situation will continue until the point when LIF-UC1xx PD frontend is turned ON. After the LIF-UC1xx frontend is configured and the detection FSM is controlling the Rp and Rd enable signals, the *Disable Clamp* signal will disable the clamp and FSM will expose either the Rp or Rd resistors depending on which DRP mode it is in. Alternately the clamp can be disconnected automatically using the VCONN supply but this will require proper sequencing of VCONN.

The time taken for the LIF-UC1xx to start operating is system dependent based on the Embedded Controller and other Power Management ICs.

Functional Descriptions

This section describes the function of each sub-block in the USB Type-C solution. See RD1210, Lattice USB Type-C Solution Design Document for more details.

Figure 4. Functional Block Diagram



CD or Cable Detect

This is the electrical/analog frontend. It controls the SS switch select signals as well as detects which CC line is connected by the cable with the port partner, and based on this information, it changes the SS switch select lines. This module also includes the Dual-Role Port FSM as described in the USB Type-C specification.

Sigma Delta ADC for Voltage Detection

The Type-C cable detection can be further divided into two parts:

- DFP/Source side CC vRd detection for ‘Attach’ and vOpen detection for ‘Detach’
- UFP/Sink side presence of V_{BUS} for ‘Attach’ and absence for ‘Detach’

Table 3. DFP and UFP Behaviors by State

State	DFP Behavior	UFP Behavior
Nothing attached	– Sense CC pins for attach – Do not apply V_{BUS} or V_{CONN}	– Sense V_{BUS} for attach
UFP attached	– Sense CC for orientation – Sense CC for detach – Apply V_{BUS} or V_{CONN}	– Sense CC pins for orientation – Sense loss of V_{BUS} for detach
Powered cable/No UFP attached	– Sense CC for attach – Do not apply V_{BUS} or V_{CONN}	– Sense V_{BUS} for attach
Powered cable/UFP attached	– Sense CC for orientation – Sense CC for detach – Apply V_{BUS} or V_{CONN}	– Sense CC for orientation – Sense loss of V_{BUS} for detach
Debug Accessory Mode attached	– Sense CC for detach – Reconfigure for debug	– N/A
Audio Adapter Accessory Mode attached	– Sense CC for detach – Reconfigure for analog audio	– N/A

Table 4. USB Type-C DFP Connection States

CC1	CC2	State	
Open	Open	vOpen	Nothing attached
Rd	Open	vRd	UFP attached
Open	Rd		
Open	Ra	vRa	Powered cable / No UFP attached
Ra	Open		
Rd	Ra	vRd + vRa	Powered cable / UFP attached
Ra	Rd		
Rd	Rd	vRd CC1 and CC2	Debug accessory mode attached (can be supported)
Ra	Ra	vRa CC1 and CC2	Audio Adapter Accessory Mode attached

CC Line vRd and vOpen Detection

This design uses RD1066, Simple Sigma-Delta to implement an ADC. This reference design provides two different topologies for ADC implementation, viz Direct topology and Network topology.

The ADC topologies used for vRd detection in the two solutions (CD/PD for Charger and CD/PD for host/devices) are different. See DS1052, Lattice USB Type-C Solution Data Sheet for details.

Table 5. CC Voltages on DFP Side - 3.0 A @ 5 V

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable / adapter (vRa)	0.00 V	0.75 V	0.80 V
UFP (vRd)	0.85 V	2.45 V	2.60 V
No connection (vOpen)	2.75 V		

Table 6. Voltage on UFP CC pins (Multiple DFP Current Advertisements)

Detection	Minimum Voltage	Maximum Voltage	Threshold
vRa	–0.25 V	0.15 V	0.2 V
vRd-Connect	0.25 V	2.04 V	
vRd-USB	0.25 V	0.61 V	0.66 V
vRd-1.5	0.70 V	1.16 V	1.23 V
vRd-3.0	1.31 V	2.04 V	

V_{BUS} Detection

On the UFP/Sink side, the first event after cable connection is the presence of VBUS on the Type-C receptacle. It is mandatory for a Device/Sink/UFP to detect this voltage and enter the 'Attached UFP' state as mentioned in the DRP FSM of the USB Type-C specification.

SS Switch Selection

One of the most exciting feature of the USB Type-C is the reversible nature of the plug. But this new feature calls for the need of detecting the orientation which is successfully done by Configuration Channel (CC1 and CC2) vRd detection. But once this orientation is detected, the device should be able to re-arrange its Data Channels to proper alignment in order to send the data across to the Port-Partner. This is done by means of external Super-Speed Switches (SS Switch) for the SSTX and the SSRX data lanes of USB3.1.

This design provides flexible number of IOs that can be used to perform the SS switch lane selection by controlling the select lines available on the switches. The design can provide up to four IOs for the select lines.

It is important to note that not all USB Type-C devices need the SS switches. This requirement is only for the USB communications capable devices. Devices such as USB Chargers and devices with Captive Cables may not need these cross bar switches since the orientation is either fixed due to captive nature or no requirement of USB data communication.

DRP FSM

This design is implemented in order to achieve the full functionality defined in the USB Type-C. Based on the specification, there are three type of ports, UFP (Device type), DFP (Host type) and the DRP (can be both UFP and a DFP).

PD PHY

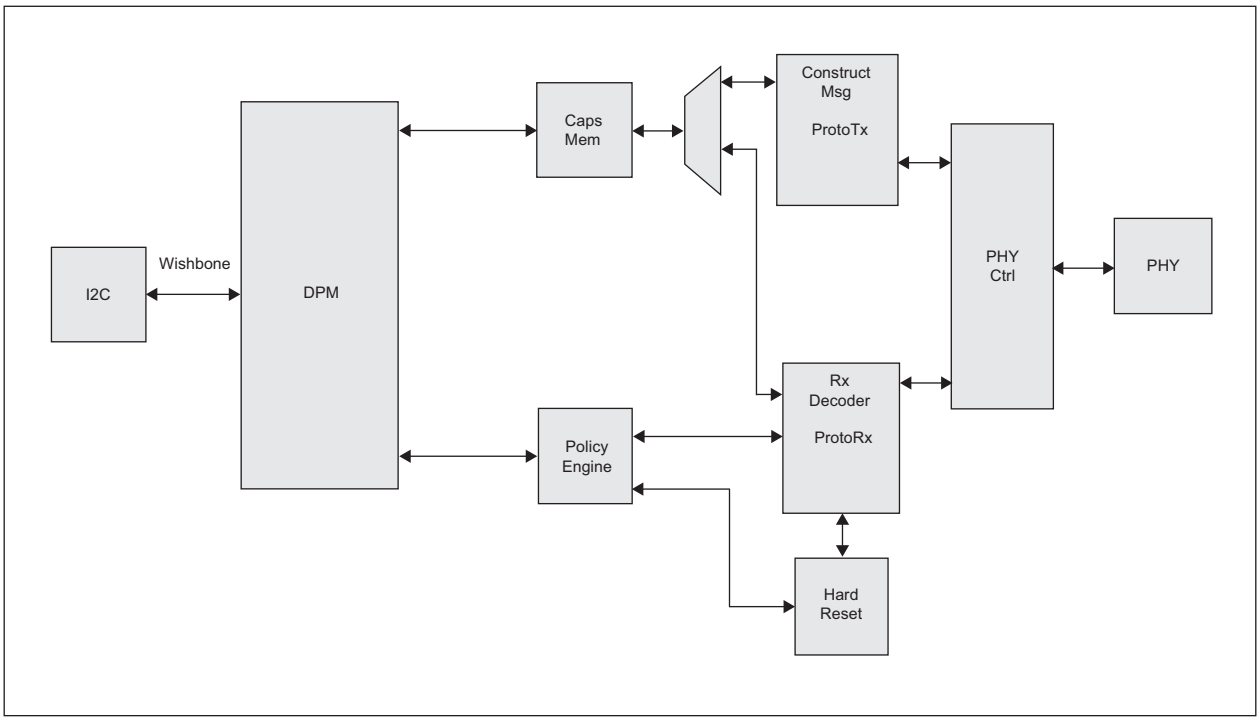
This module has three internal modules:

- Register Interface
- Tx with 4B5B and BMC encoding
- Rx with BMC decoding, start/stop detection and 4B5B decoder

PD PHY Manager

This module handles the USB PD implementation and responsible for transmission and reception of Power Delivery messages. The Figure 6 depicts the architecture of Power Delivery Manager.

Figure 5. Architecture of Power Delivery Manager



I²C Slave Controller

I²C Slave controller is used as the communication channel between Application Processor (AP) and Lattice PD. Power Delivery process is interrupt driven.

Device Policy Manager (DPM)

The Device Policy Manager is responsible for applying local policies based on the fixed I²C Register Set or inputs from the AP, to the Power Delivery negotiation process.

Capabilities Memory

This is a pre-initialized memory which has the default Port Source and Sink Power capabilities (PDO) defined. In addition, it has space to hold the received port partners Source and Sink Power capabilities (PDO) for the AP to access.

Policy Engine (PE)

The Policy Engine interprets the Device Policy Manager's input in order to implement Policy for a given Port and directs the Protocol Layer to send appropriate messages.

Protocol Layer

The Protocol Layer is divided into three modules:

- Proto Tx
- Proto Rx
- Hard reset

Proto Tx

Proto Tx module is responsible for transmission of a Power Delivery packet.

Proto Rx

Proto Rx module is responsible for reception of a Power Delivery Packet.

Hard Reset

Hard Reset module handles the hard reset condition if received by the port partner or if initiated by own port. On a hard reset condition, this module makes sure that all power levels and protocol layer is reset to default before any further PD communication.

PHY Control
The PHY control module is used as a communication interface between the Protocol Layer and the PHY

EC/AP Interface to Lattice Device

The registers provided in Lattice device may be accessed through most of the serial interfaces based on custom Requirements. By default Lattice solution offers ready access via I^2C serial interface.

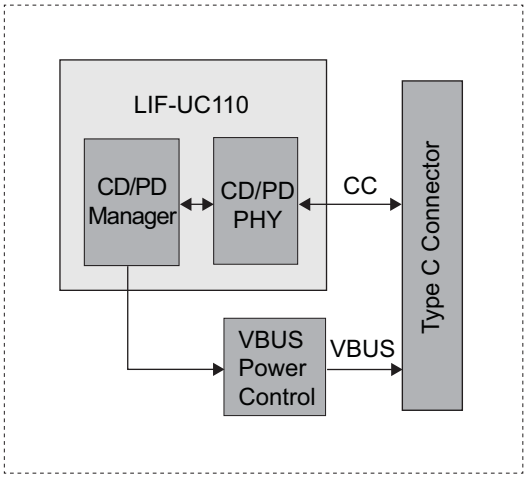
V_{BUS} Power Control

V_{BUS} Power control logic generates control signals to control V_{BUS} source, V_{BUS} Sink and V_{BUS} discharge FETs. For application like charger or multiple PD power profile, Lattice solution generates necessary control signals to select the multiple voltages.

Lattice Type-C Solutions

CD PD for Charger

Figure 6. USB CD/PD Charger (Captive or Non-captive Cable) Block Diagram



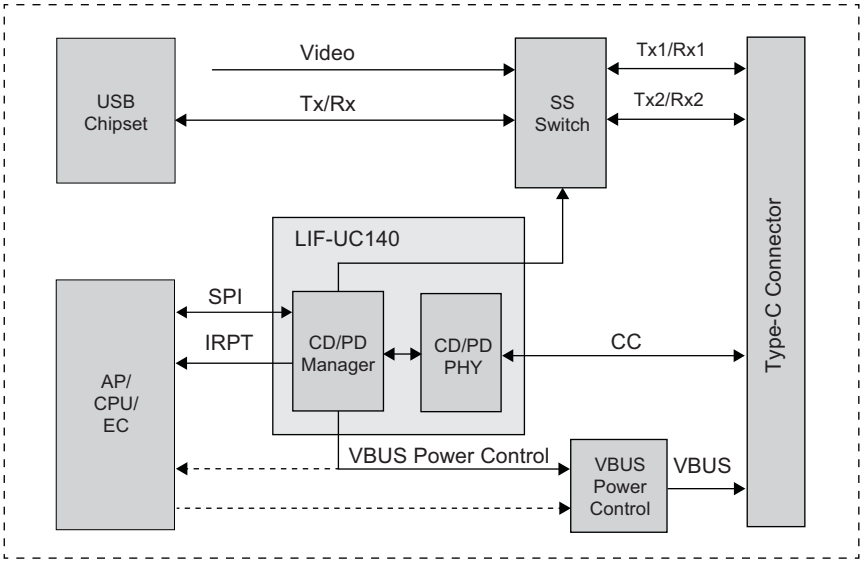
CD = Cable Detect
PD = Power Delivery

Lattice CD PD Charger is targeted for USB Type-C based chargers. This solution comes with the following:

- Cable Detect (CD) Logic
- PD PHY
- PD PHY Manager
- V_{BUS} Power control signals for V_{BUS} Source, discharge and selecting multiple PD Profiles

CD PD for Hosts/Devices

Figure 7. USB CD/PD for Hosts/Devices Block Diagram



CD = Cable Detect
PD = Power Delivery

This solution is targeted for mobile applications in notebooks, smartphones and tablets. This solution comes with the following:

- Cable Detect (CD) Logic
- PD PHY
- PD PHY Manager
- VDM Support
- Power Role and Data Role Swap
- Enter Billboard Mode signal for EC/AP
- SS Switch Control signals
- V_{BUS} Power control signals for V_{BUS} Source, Sink and discharge

Test Results

This section describes the results of a few tests performed using Rev A of *Lattice USB 3.1 Type-C Development Kit*. The full test report can be found in *Lattice USB 3.1-Type C Test Report* document. For access to this document, please contact your Lattice Sales Representative.

Dual Role Port (DRP)

A dual role port is capable of both sourcing and sinking and can become either a DFP or a UFP after role resolution with the partner port.

Pass Criteria

The tDRP parameter represents the overall period for a single cycle during which the port must be exposed as both a DFP and a UFP.

Figure 8. DRP Timing as Per Specification

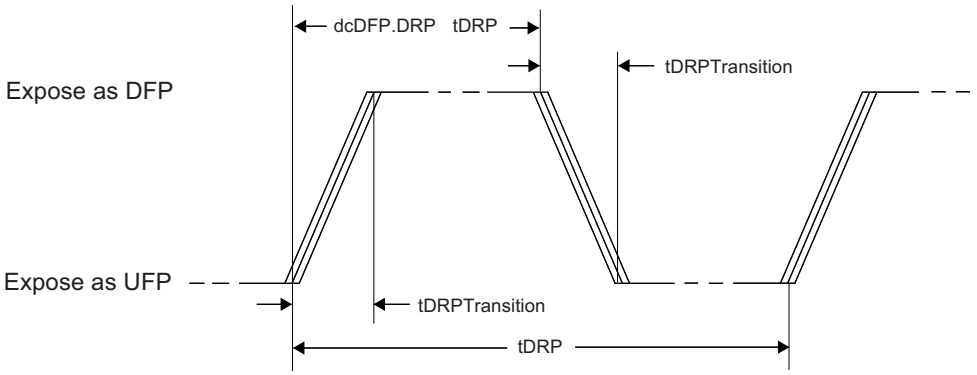


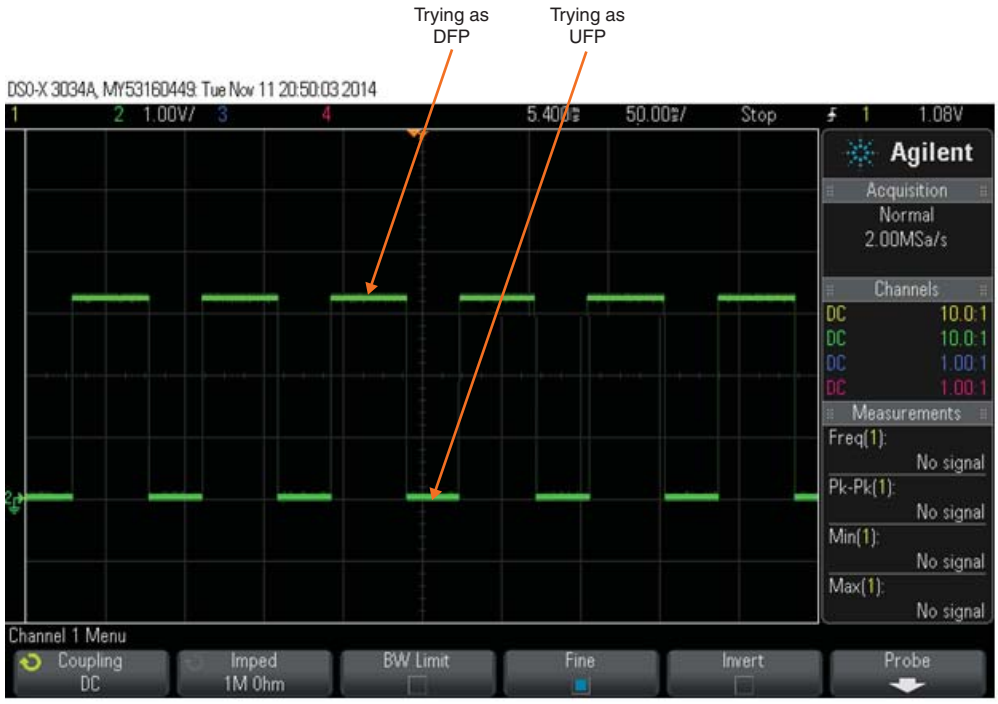
Table 7. DRP Timing Parameters

	Minimum	Maximum	Description
tDRP	50 ms	100 ms	The period a DRP shall complete a DFP to UFP and back advertisement
dcDFP.DRP	30%	70%	The percent of time that a DRP shall advertise DFP during tDRP
tDRPTransition	0 ms	1 ms	The time a DRP shall complete transitions between DFP and UFP roles during role resolution
tDRPHold	100 ms	150 ms	Wait time associated with the *Attach.DFP.DRPWait* state

Results

Figure 11 shows the CC line on the Lattice demo board when no port partner is connected. Note the difference in the duty cycle implying that RP is exposed for a longer period then RD, thus providing a provision of applying a preferred DFP implementation.

Figure 9. RP/RD Exposure on CC Line



Cable Attach

Pass Criteria:

As soon as a port partner (UFP) is connected, DRP should go to the attached state and the CC line voltage is seen for default USB current rating as per below specification table. Note that based on the RP resistor mounted on the demo board, the voltage level on the CC line falls between any of the three different ranges as mentioned in the USB TYPE-C specification.

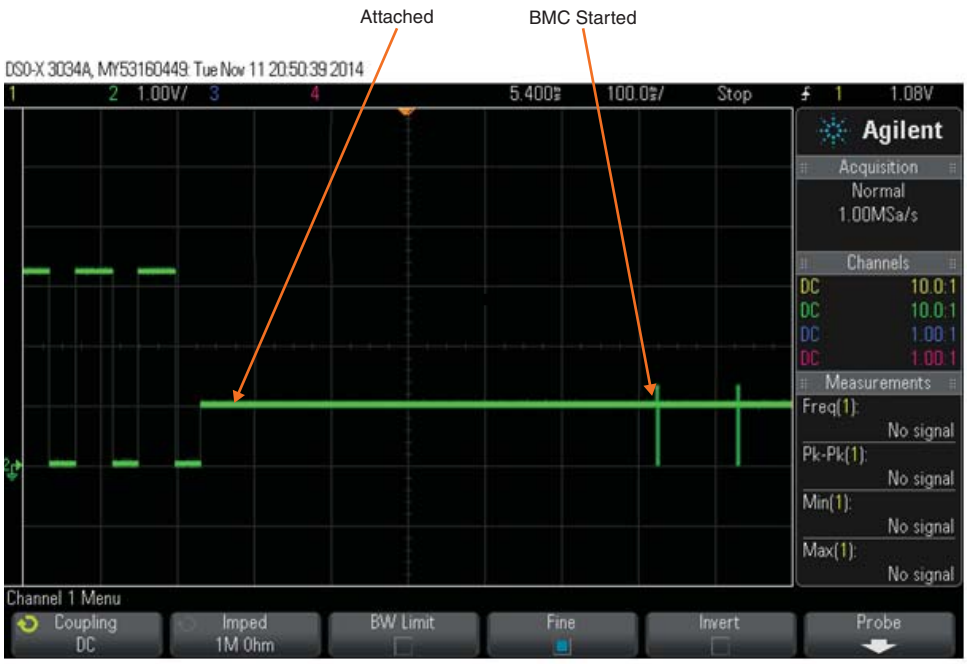
Table 8. CC Voltages on DFP Side – Default USB

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable / adapter (vRa)	0.00 V	0.15 V	0.20 V
UFP (vRd)	0.25 V	1.50 V	1.60 V
No connection (vOpen)	1.65 V		

Results

A voltage of ~1 V is observed on the connected CC line.

Figure 10. CC Voltage on DFP Side



Cable Detach

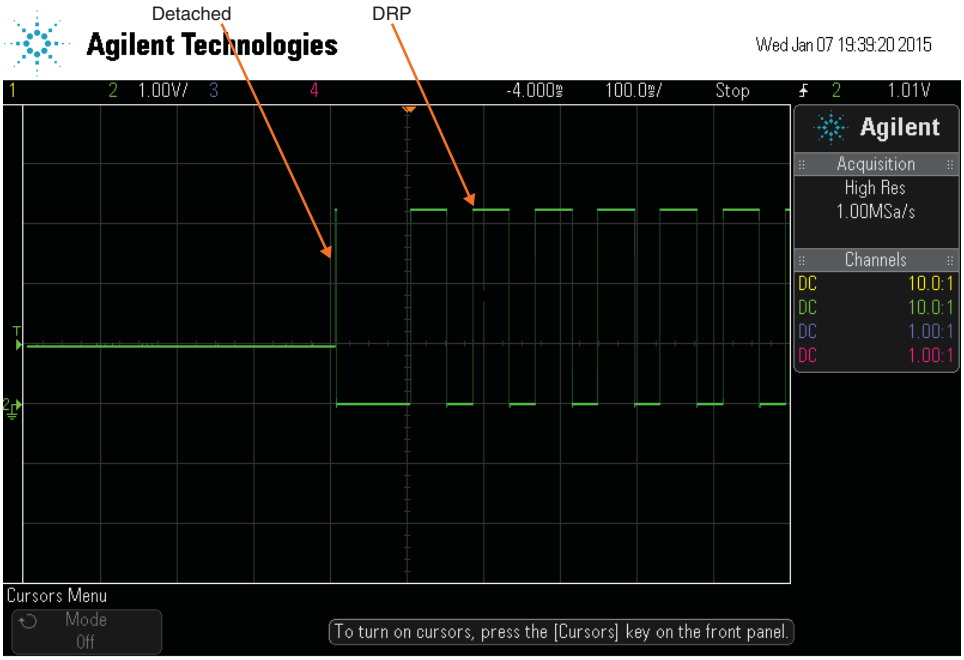
Pass Criteria

As soon as the port partner is disconnected, the Lattice DRP should go back to the role resolution state where it re-starts the RP/RD alternate exposure on the CC line.

Results

Figure 13 shows the DRP entering the role-resolution state after a detach condition.

Figure 11. Detach Event Leading to DFP to UFP and Back Advertisement (Role Resolution)



Cable Flip

Pass Criteria

The cable detect logic should successfully change the orientation by detecting the used CC line. If the Cable attach test is passed then the BMC transmission should follow on the connected Configuration Channel.

Result

Figure 15 shows the BMC data changing from CC1 to CC2 based on the orientation detection done by the cable detect logic.

Figure 12. BMC on CC1 Shows No Cable Flip

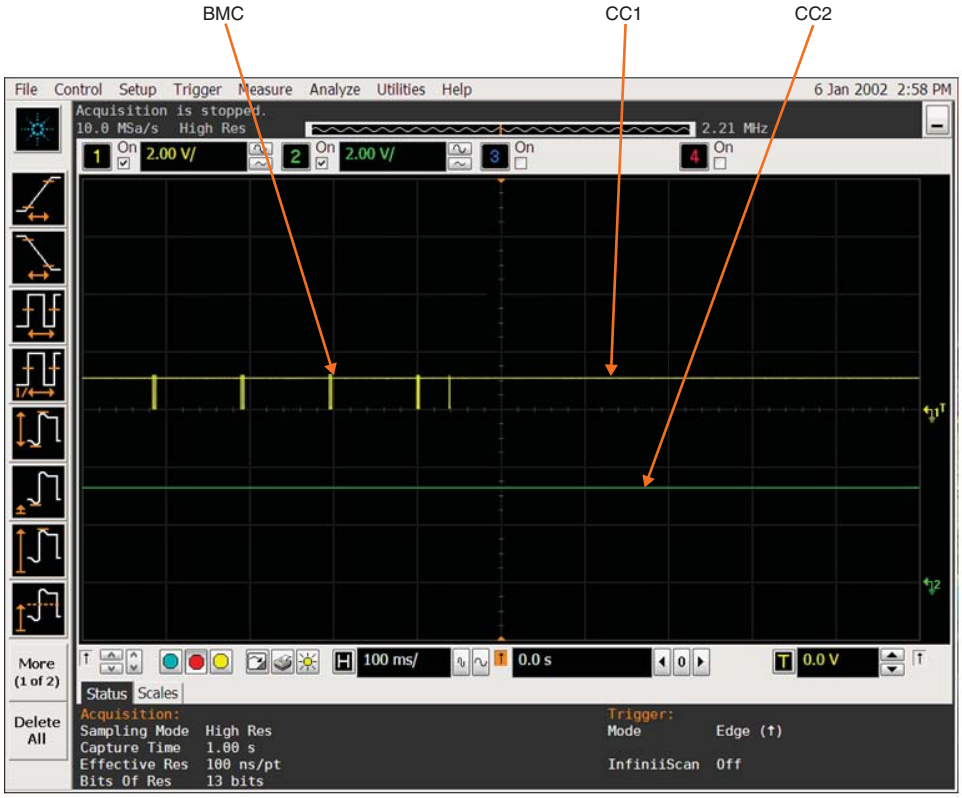
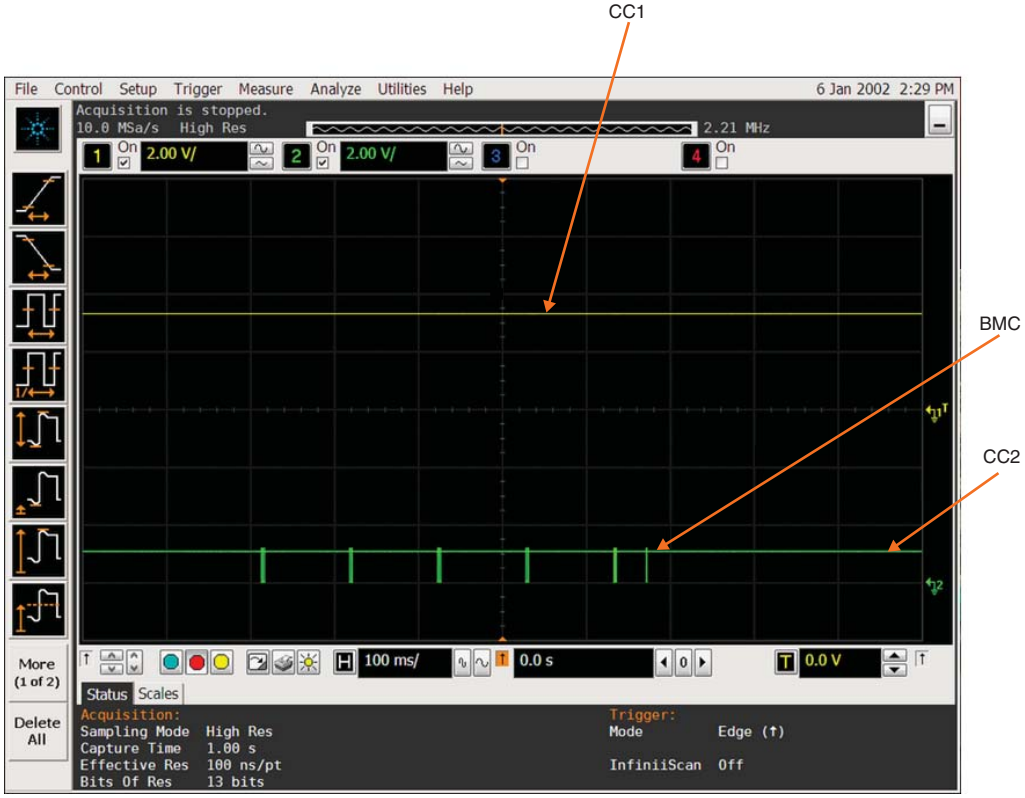


Figure 13. BMC on CC2 Shows Cable Flip



PD Contract

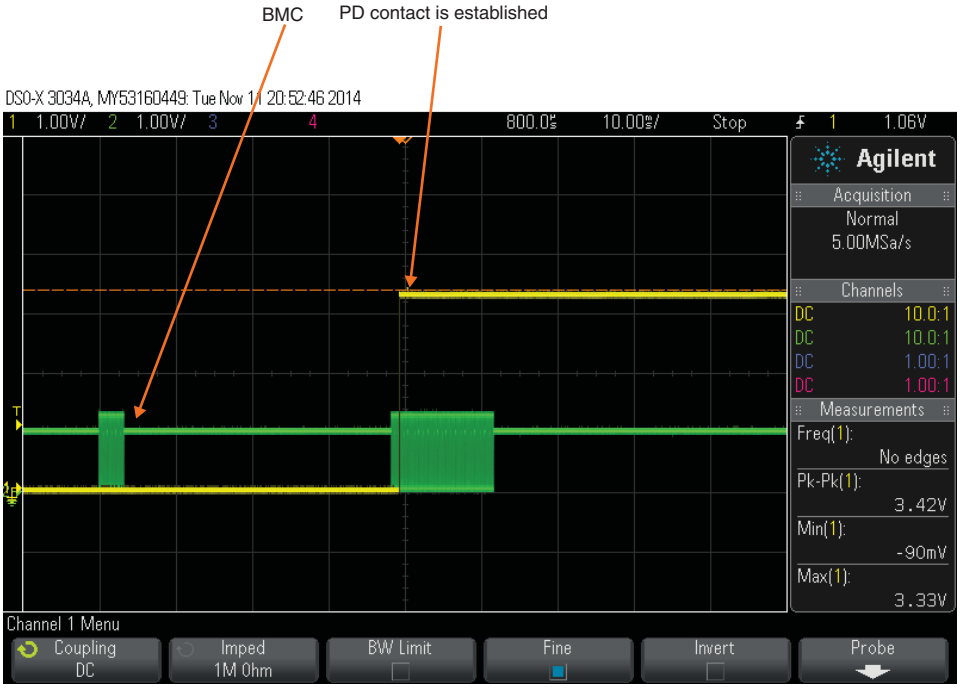
Pass Criteria

After cable detection, a power negotiation should lead to successful contract between port partners and hence enter into explicit power contract. Based on the design loaded on the demo board, different capabilities will be advertised by the DFP. In general, Lattice demo solutions hold the USB PD Fixed Supply Object i.e. Profile 0 at 5 V as the default capability.

Results

Figure 16 shows an “ACCEPT” message been sent followed by a “PS_RDY” after tSnkTransition (35ms).

Figure 14. CC Line Showing BMC Messages and a Test Point Showing Successful PD Contract



Eye Mask

Below test results are obtained using GRL software/masks on the Agilent DSA91304A. The eye masks are defined in the USB PD USB Type-C specification.

Pass Criteria

Transmitter (Near end) and Receiver (Far end) eye mask test should pass with GRL software. Since the USB Type-C has three different RP pull up resistor values that can change the CC line characteristics. Hence it is mandatory that the Eye Diagrams are captured and passed for all three RP values (36K, 12K and 4.7K.)

Results

Near End Eye Diagram (Tx) With Rp = 36 K

Eye diagrams tests are done with the resistor values of 45 Ω, 100 Ω and 2nF for the transmitter.

Figure 15. Near End Eye Diagram for '1' with Rp = 36 KΩ

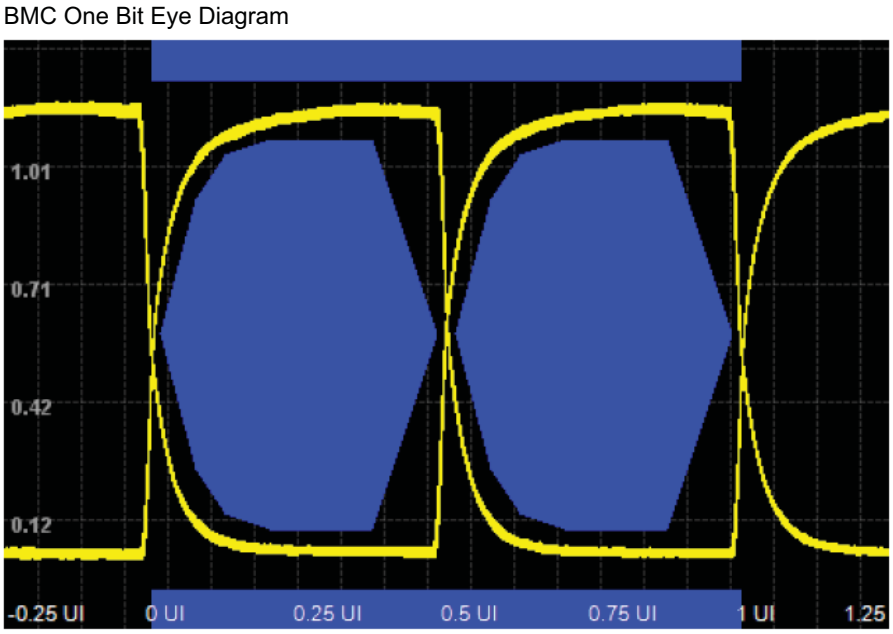
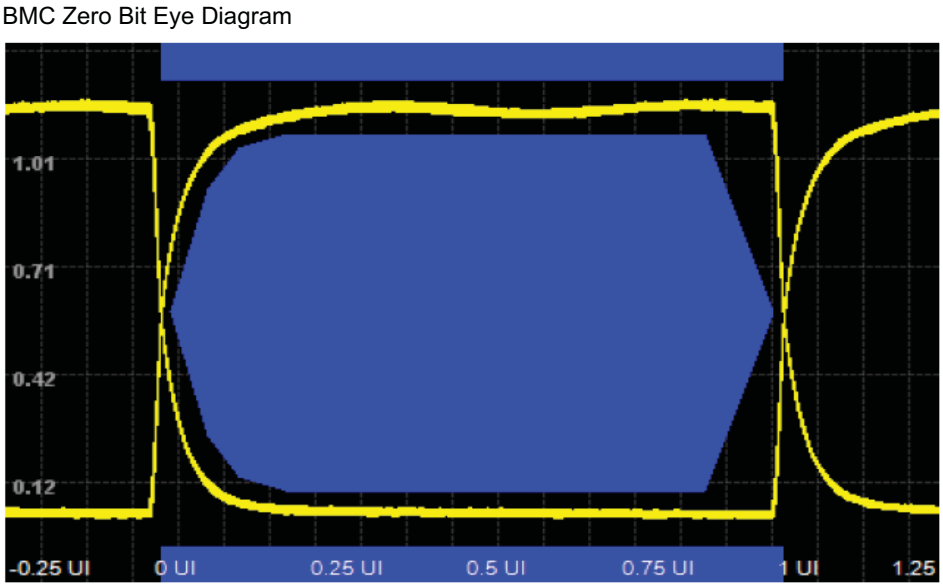


Figure 16. Near End Eye Diagram for '0' with Rp=36 KΩ



Far End Eye Diagram (Rx) With Rp = 36 K

Eye diagrams tests are done with the resistor values of 45 Ω, 100 Ω and 2nF for the transmitter.

Figure 17. Far End Eye Diagram for '1' with Rp=36 KΩ

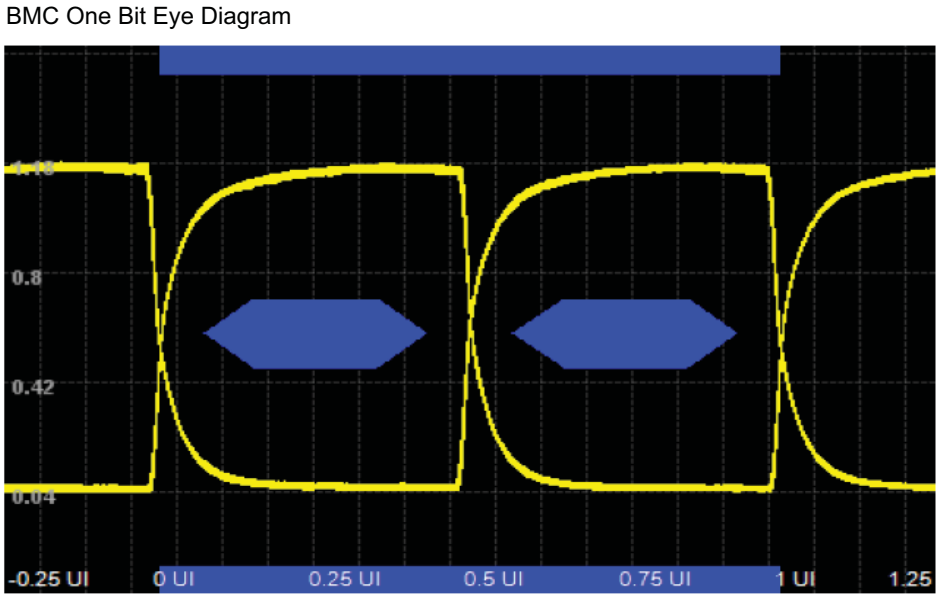
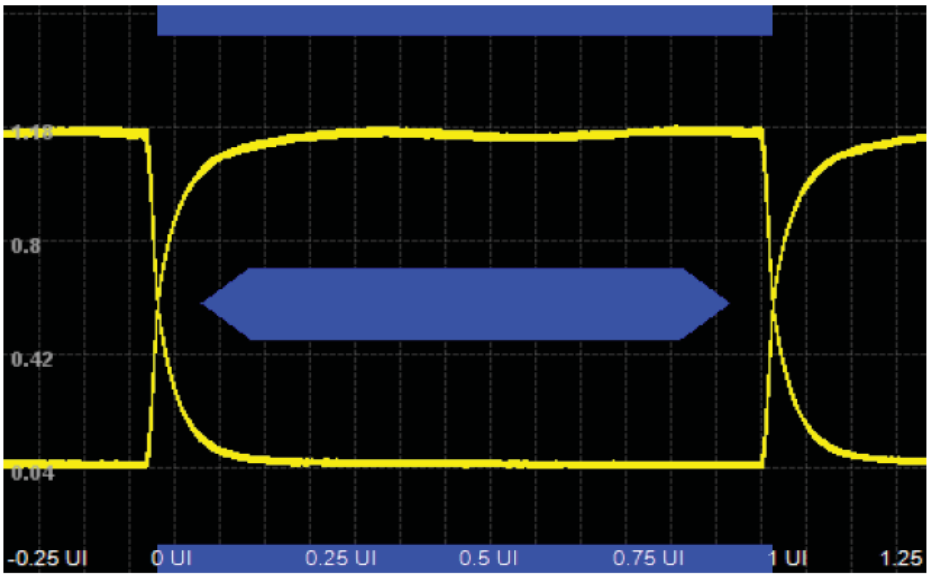


Figure 18. Far End Eye Diagram for '0' with Rp=36 KΩ



Test Results Summary

Table 9. Lattice CD/PD Test Cases and Results

S:No	Test	Pass	Comments
1	Dual Role Port	Yes	
2	Cable Attach	Yes	
3	Cable Detach	Yes	
4	Cable Flip	Yes	
5	Rise/Fall time	Yes	
6	Dead Battery	Yes	
7	Capability Exchange	Yes	
8	PD Contract (Fixed PDO 0)	Yes	
9	Multiple PD Contract	Yes	
10	Reject Message	Yes	
11	Capability Retrying	Yes	
12	Hard Reset	Yes	
13	Eye Mask for TX/RX	Yes	
14	Power Role Swap	Yes	
15	Data Role Swap	Yes	
16	Structured VDM Discovery Identity	Yes	
17	Structured VDM Entry/Exit	Yes	

Compliance Results

Charger

Ellisys Test - Ellisys USB Compliance Report

Date and time:	Wednesday, 11 May 2016 12:51:40 GMT+5
Vendor:	Lattice Semiconductor
Product:	LIF-UC110
Product version:	v1.0
Test ID:	10945
Generator used:	Ellisys USB Explorer 350 (EX350-62115)
Analyzer used:	Ellisys USB Explorer 350 (EX350-62114)
Software version:	Report generated with version 3.1.5962
Overall result:	Passed

Summary

		Test Status	Last Update
USB Type-C Tests	Passed		
» TD.PD.C.E1 DFP Attach/Detach Detection	Passed	Stable	2015-06-17
USB Type-C Functional Tests	Passed		
» TD.4.1.1 Initial Voltage	Passed	RC	2016-02-29
» TD.4.2.1 Source Connect Sink	Passed	Stable	2015-09-02
» TD.4.2.2 Source Connect Sink Accessory	Passed	Stable	2015-08-10
» TD.4.2.3 Source Connect DRP	Passed	Stable	2015-08-10
» TD.4.2.6 Source Connect Audio Accessory	Passed	Stable	2015-08-10

		Test Status	Last Update
» TD.4.2.8 Source Connect Powered Accessory	Not Applicable	Stable	2015-09-09
» TD.4.9.2 USB Type-C Current Advertisement	Passed	RC	2016-03-14
» TD.4.9.3 Source Power Role Swap	Not Applicable	Stable	2016-04-05
» TD.4.9.4 Source Vconn Swap	Not Applicable	Stable	2015-09-11
» TD.4.11.1 Data Role Swap	Not Applicable	RC	2016-03-30
USB PD Physical Tests	Passed		
» TD.PD.PHY.E1 BIST Test Data	Passed	Stable	2015-08-18
» TD.PD.PHY.E2 BIST Receiver Mode	Not Applicable	Stable	2016-02-10
» TD.PD.PHY.E3 BIST Transmitter Mode	Not Applicable	Stable	2015-08-18
» TD.PD.PHY.E4 Transmitter Bit Rate Drift	Passed	Stable	2016-04-13
» TD.PD.PHY.E5 Transmitter Collision Avoidance	Passed	RC	2016-01-20
» TD.PD.PHY.E6 Receiver Swing Tolerance	Passed	Stable	2015-08-18
» TD.PD.PHY.E7 Receiver Bit Rate Tolerance	Passed	Stable	2015-08-18
» TD.PD.PHY.E8 Receiver Bit Rate Deviation Tolerance	Passed	Stable	2015-08-18
» TD.PD.PHY.E9 Valid SOP Framing	Passed	Stable	2015-11-27
» TD.PD.PHY.E10 Invalid SOP Framing	Passed	Stable	2015-11-27
» TD.PD.PHY.E11 Valid SOP' Framing	Passed	Stable	2015-11-27
» TD.PD.PHY.E12 Invalid SOP' Framing	Passed	Stable	2015-11-27
» TD.PD.PHY.E13 Valid SOP" Framing	Passed	Stable	2015-11-27
» TD.PD.PHY.E14 Invalid SOP" Framing	Passed	Stable	2015-11-27
» TD.PD.PHY.E15 Valid SOP'/" Debug Framings	Passed	Stable	2015-11-27
» TD.PD.PHY.E16 Valid Hard Reset Framing	Passed	RC	2015-08-21
» TD.PD.PHY.E17 Invalid Hard Reset Framing	Passed	RC	2015-08-21
» TD.PD.PHY.E18 Valid Cable Reset Framing	Passed	RC	2015-08-21
» TD.PD.PHY.E19 Invalid Cable Reset Framing	Passed	RC	2015-08-21
» TD.PD.PHY.E20 EOP Framing	Passed	Stable	2015-08-18
» TD.PD.PHY.E21 Preamble	Passed	Stable	2015-08-18
USB PD Link Tests	Passed		
» TD.PD.LL.E2 Retransmission	Passed	Stable	2015-11-27
» TD.PD.LL.E3 Soft Reset Usage	Passed	Stable	2015-08-18
» TD.PD.LL.E4 Hard Reset Usage	Passed	Stable	2015-08-18
» TD.PD.LL.E5 Soft Reset	Passed	Stable	2015-08-18
USB PD Source Tests	Passed		
» TD.PD.SRC.E1 Source Capabilities sent timely	Passed	Stable	2016-01-19
» TD.PD.SRC.E2 Source Capabilities Fields Checks	Passed	Stable	2016-01-19
» TD.PD.SRC.E3 SourceCapabilityTimer Timeout	Passed	Stable	2015-08-27
» TD.PD.SRC.E4 SenderResponseTimer Deadline - Request	Passed	Stable	2015-08-27
» TD.PD.SRC.E5 SenderResponseTimer Timeout - Request	Passed	Stable	2015-08-27
» TD.PD.SRC.E6 PSHardResetTimer Timeout	Passed	Stable	2016-03-10
» TD.PD.SRC.E7 Accept sent timely	Passed	Stable	2015-08-27
» TD.PD.SRC.E8 Accept Fields Checks	Passed	Stable	2015-08-27
» TD.PD.SRC.E9 PS_RDY sent timely	Passed	Stable	2015-08-27
» TD.PD.SRC.E10 PS_RDY Fields Checks	Passed	Stable	2015-08-27
» TD.PD.SRC.E11 Accept Requests can be met	Passed	Stable	2015-08-27
» TD.PD.SRC.E12 Reject Requests can't be met	Passed	Stable	2015-08-27

		Test Status	Last Update
» TD.PD.SRC.E13 Reject Request - Invalid Object Position	Passed	Stable	2015-08-27
» TD.PD.SRC.E14 Atomic Message Sequence	Passed	RC	2015-09-23
» TD.PD.SRC.E15 Give_Source_Cap	Passed	RC	2015-09-23
» TD.PD.SRC.E16 PDO Transition	Passed	Beta	2015-11-06
USB PD Sink Tests	Passed		
USB PD Provider / Consumer Tests	Passed		
» TD.PD.PC.E1 tSrcTransition Check	Not Applicable	RC	2016-03-24
» TD.PD.PC.E2 PS_RDY Sent Timely	Not Applicable	RC	2016-03-24
» TD.PD.PC.E3 PSSourceOnTimer Deadline	Not Applicable	RC	2016-03-24
» TD.PD.PC.E4 PSSourceOnTimer Timeout	Not Applicable	RC	2016-03-24
» TD.PD.PC.E5 tSwapSinkReady Check	Not Applicable	RC	2016-03-24
» TD.PD.PC.E6 Externally Powered Bit Usage	Passed	RC	2016-03-24
» TD.PD.PC.E7 PDO Transition After PR_Swap	Not Applicable	RC	2016-03-24
USB PD Consumer / Provider Tests	Passed		
USB PD VDM Tests for UFPs and Cables	Passed		
DisplayPort Alt-Mode Tests for UFPs and Cables	Passed		
DisplayPort Alt-Mode Tests for DFPs	Not Applicable		
» TD.PD.DPD.E1 Cable Determination	Not Applicable	Stable	2015-09-16
» TD.PD.DPD.E2 DP SVID in Arbitrary Location	Not Applicable	Stable	2015-09-17
» TD.PD.DPD.E3 Status Update Presence	Not Applicable	Stable	2015-09-16
» TD.PD.DPD.E4 Enter Mode Rejected	Not Applicable	Stable	2015-09-16
» TD.PD.DPD.E5 Enter Mode Not Responded	Not Applicable	Stable	2015-09-16
» TD.PD.DPD.E6 DisplayPort Not Connected	Not Applicable	Stable	2015-09-16
» TD.PD.DPD.E7 Status Update Port Resolution	Not Applicable	Stable	2015-09-16
» TD.PD.DPD.E8 Not Compatible Connection	Not Applicable	Stable	2015-10-28
» TD.PD.DPD.E9 Field Checks - DisplayPort Configure	Not Applicable	Alpha	2016-03-10
USB PD Consistency Tests	Passed		
» TD.PD.VNDI.E4 SOP* Handling	Passed	Stable	2015-08-18
» TD.PD.VNDI.E5 Source Capabilities	Passed	RC	2016-02-29
» TD.PD.VNDI.E7 Accepts PR_Swap as Source	Not Applicable	Stable	2016-03-14
» TD.PD.VNDI.E9 Requests PR_Swap as Source	Not Applicable	Stable	2016-02-10

MQP Test - Phy Test

Packet-Master USB-PDT Report on Lattice_Semiconductor LIF-UC110

GraphicUSB V4.84 -- Scripts PDT Rev:0.9.1.4

Date and time:	Test run on Monday, May 16, 2016 16:09:01
Vendor:	Lattice Semiconductor
Product:	LIF-UC110
Product version:	v1.0
Test ID:	10945

The following tests have been selected:

- BMC-PHY-TX-EYE
- BMC-PHY-RX-INT-REJ
- BMC-PHY-RX-BUSIDL
- BMC-PHY-TERM
- BMC-PHY-MSG

Summary

BMC-PHY-TX-EYE	
BMC-PHY-TX-EYE Primary	Passed
BMC-PHY-TX-EYE Secondary	Passed
BMC-PHY-RX-INT-REJ	
BMC-PHY-RX-INT-REJ	Passed
BMC-PHY-RX-INT-REJ Secondary	Passed
BMC-PHY-RX-BUSIDL	
BMC-PHY-RX-BUSIDL	Passed
BMC-PHY-RX-BUSIDL Secondary	Passed
BMC-PHY-TERM	
BMC-PHY-TERM	Passed
BMC-PHY-TERM Secondary	Passed
BMC-PHY-MSG	
BMC-PHY-MSG	Passed
BMC-PHY-MSG Secondary	Failed

USB-IF Summary	
BMC PHY Tx	Passed
BMC PHY Rx	Passed
BMC PHY Misc:	Passed
Protocol Specific:	
Power Specific:	
Secondary	Failed

MQP Test - Power Test

Packet-Master USB-PDT Report on Lattice_Semiconductor LIF-UC110

GraphicUSB V4.84 -- Scripts PDT Rev:0.9.1.4

Date and time:	Test run on Monday, May 16, 2016 16:13:30
Vendor:	Lattice Semiconductor
Product:	LIF-UC110
Product version:	v1.0
Test ID:	10945

The following tests have been selected:

- BMC-POW-SRC-LOAD-P-PC
- BMC-POW-SRC-TRANS-P-PC

Summary

BMC-POW-SRC-LOAD-P-PC	
BMC-POW-SRC-LOAD-P-PC	Passed
BMC-POW-SRC-LOAD-P-PC Secondary	Failed
BMC-POW-SRC-TRANS-P-PC	
BMC-POW-SRC-TRANS-P-PC	Passed
BMC-POW-SRC-TRANS-P-PC Secondary	Failed

USB-IF Summary	
BMC PHY Tx	
BMC PHY Rx	
BMC PHY Misc:	
Protocol Specific:	
Power Specific:	Passed
Secondary	Failed

MQP Test - Protocol Test

Packet-Master USB-PDT Report on Lattice_Semiconductor LIF-UC110

GraphicUSB V4.84 -- Scripts PDT Rev:0.9.1.4

Date and time:	Test run on Monday, May 16, 2016 16:12:08
Vendor:	Lattice Semiconductor
Product:	LIF-UC110
Product version:	v1.0
Test ID:	10945

The following tests have been selected:

- BMC-PROT-SEQ-GETCAPS
- BMC-PROT-SEQ-CHKCAB-P-PC
- BMC-PROT-SEQ-NOMRK-P-PC
- BMC-PROT-SEQ-PRSWAP
- BMC-PROT-SEQ-DRSWAP
- BMC-PROT-SEQ-VCSWAP
- BMC-PROT-BIST-NOT-5V-SRC
- BMC-PROT-REV-NUM

Summary

BMC-PROT-SEQ-GETCAPS	
BMC-PROT-SEQ-GETCAPS	Passed
BMC-PROT-SEQ-GETCAPS Secondary	Passed
BMC-PROT-SEQ-CHKCAB-P-PC	
BMC-PROT-SEQ-CHKCAB-P-PC	Passed
BMC-PROT-SEQ-CHKCAB-P-PC Secondary	Passed
BMC-PROT-SEQ-NOMRK-P-PC	
BMC-PROT-SEQ-NOMRK-P-PC	Passed
BMC-PROT-SEQ-NOMRK-P-PC Secondary	Passed
BMC-PROT-SEQ-PRSWAP	
BMC-PROT-SEQ-DRSWAP	Passed
BMC-PROT-SEQ-DRSWAP Secondary	Passed
BMC-PROT-SEQ-DRSWAP	
BMC-PROT-SEQ-DRSWAP	Passed
BMC-PROT-SEQ-DRSWAP Secondary	Failed
BMC-PROT-SEQ-VCSWAP	
BMC-PROT-SEQ-VCSWAP	Passed
BMC-PROT-SEQ-VCSWAP Secondary	Passed
BMC-PROT-REV-NUM	
BMC-PROT-REV-NUM	Passed
BMC-PROT-REV-NUM Secondary	Passed

USB-IF Summary	
BMC PHY Tx	
BMC PHY Rx	
BMC PHY Misc:	
Protocol Specific:	Passed
Power Specific:	
Secondary	Passed

CD/PD for Host/Devices

Ellisys Test - Ellisys USB Compliance Report

Date and time:	Friday, 3 June 2016 18:02:08 GMT+5
Vendor:	Lattice Semiconductor
Product:	DRP
Product version:	v1.0
Test ID:	10945
Generator used:	Ellisys USB Explorer 350 (EX350-62115)
Analyzer used:	Ellisys USB Explorer 350 (EX350-62114)
Software version:	Report generated with version 3.1.5989
Overall result:	Failed

Summary

		Test Status	Last Update
USB Type-C Tests	Passed		
» TD.PD.C.E1 DFP Attach/Detach Detection	Passed	Stable	2015-06-17
» TD.PD.C.E2 UFP Rp	Passed	Stable	2015-06-17
» TD.PD.C.E5 DRP	Passed	Stable	2016-04-25
USB Type-C Functional Tests	Passed		
» TD.4.1.1 Initial Voltage	Passed	RC	2016-02-29
» TD.4.3.5 Sink Connect SNKAS	Not Applicable	Alpha	2016-01-15
» TD.4.5.1 DRP Connect Sink	Passed	Beta	2016-01-11
» TD.4.5.2 DRP Connect SNKAS	Passed	Beta	2015-10-22
» TD.4.5.3 DRP Connect Source	Passed	Beta	2016-05-09
» TD.4.5.4 DRP Connect DRP	Passed	Beta	2016-02-29
» TD.4.8.1 DRP Connect Audio Accessory	Passed	Stable	2015-10-28
» TD.4.8.3 DRP Connect Alternate Mode	Not Applicable	Stable	2016-01-26
» TD.4.9.2 USB Type-C Current Advertisement	Passed	RC	2016-03-14
» TD.4.9.3 Source Power Role Swap	Passed	Stable	2016-04-05
» TD.4.9.4 Source Vconn Swap	Not Applicable	Stable	2015-09-11
» TD.4.10.1 Sink Power Sub-States	Passed	Stable	2015-10-01
» TD.4.10.2 Sink Power Precedence	Passed	Alpha	2016-05-23
» TD.4.10.3 Sink Suspend	Not Applicable	Alpha	2016-04-25
» TD.4.10.4 Sink Power Role Swap	Passed	RC	2016-04-05
» TD.4.10.5 Sink Vconn Swap	Not Applicable	Stable	2015-09-11
» TD.4.11.1 Data Role Swap	Passed	RC	2016-03-30
» TD.4.11.2 Sink Dead Battery	Not Applicable	Beta	2016-01-18
USB PD Physical Tests	Passed		
» TD.PD.PHY.E1 BIST Test Data	Passed	Stable	2015-08-18
» TD.PD.PHY.E2 BIST Receiver Mode	Not Applicable	Stable	2016-02-10
» TD.PD.PHY.E3 BIST Transmitter Mode	Not Applicable	Stable	2015-08-18
» TD.PD.PHY.E4 Transmitter Bit Rate Drift	Passed	Stable	2016-04-13
» TD.PD.PHY.E5 Transmitter Collision Avoidance	Passed	RC	2016-01-20
» TD.PD.PHY.E6 Receiver Swing Tolerance	Passed	Stable	2015-08-18
» TD.PD.PHY.E7 Receiver Bit Rate Tolerance	Passed	Stable	2015-08-18
» TD.PD.PHY.E8 Receiver Bit Rate Deviation Tolerance	Passed	Stable	2015-08-18
» TD.PD.PHY.E9 Valid SOP Framing	Passed	Stable	2015-11-27
» TD.PD.PHY.E10 Invalid SOP Framing	Passed	Stable	2015-11-27
» TD.PD.PHY.E11 Valid SOP' Framing	Passed	Stable	2015-11-27
» TD.PD.PHY.E12 Invalid SOP' Framing	Passed	Stable	2015-11-27
» TD.PD.PHY.E13 Valid SOP" Framing	Passed	Stable	2015-11-27
» TD.PD.PHY.E14 Invalid SOP" Framing	Passed	Stable	2015-11-27
» TD.PD.PHY.E15 Valid SOP'/" Debug Framings	Passed	Stable	2015-11-27
» TD.PD.PHY.E16 Valid Hard Reset Framing	Passed	RC	2015-08-21
» TD.PD.PHY.E17 Invalid Hard Reset Framing	Passed	RC	2015-08-21
» TD.PD.PHY.E18 Valid Cable Reset Framing	Passed	RC	2015-08-21
» TD.PD.PHY.E19 Invalid Cable Reset Framing	Passed	RC	2015-08-21

		Test Status	Last Update
» TD.PD.PHY.E20 EOP Framing	Passed	Stable	2015-08-18
» TD.PD.PHY.E21 Preamble	Passed	Stable	2015-08-18
USB PD Link Tests	Passed		
» TD.PD.LL.E2 Retransmission	Passed	Stable	2015-11-27
» TD.PD.LL.E3 Soft Reset Usage	Passed	Stable	2015-08-18
» TD.PD.LL.E4 Hard Reset Usage	Passed	Stable	2015-08-18
» TD.PD.LL.E5 Soft Reset	Passed	Stable	2015-08-18
» TD.PD.LL.E6 Ping	Passed	Stable	2015-08-18
USB PD Source Tests	Passed		
» TD.PD.SRC.E1 Source Capabilities sent timely	Passed	Stable	2016-01-19
» TD.PD.SRC.E2 Source Capabilities Fields Checks	Passed	Stable	2016-01-19
» TD.PD.SRC.E3 SourceCapabilityTimer Timeout	Passed	Stable	2016-04-28
» TD.PD.SRC.E4 SenderResponseTimer Deadline - Request	Passed	Stable	2015-08-27
» TD.PD.SRC.E5 SenderResponseTimer Timeout - Request	Passed	Stable	2015-08-27
» TD.PD.SRC.E6 PSHardResetTimer Timeout	Passed	Stable	2016-03-10
» TD.PD.SRC.E7 Accept sent timely	Passed	Stable	2015-08-27
» TD.PD.SRC.E8 Accept Fields Checks	Passed	Stable	2015-08-27
» TD.PD.SRC.E9 PS_RDY sent timely	Passed	Stable	2015-08-27
» TD.PD.SRC.E10 PS_RDY Fields Checks	Passed	Stable	2015-08-27
» TD.PD.SRC.E11 Accept Requests can be met	Passed	Stable	2015-08-27
» TD.PD.SRC.E12 Reject Requests can't be met	Passed	Stable	2015-08-27
» TD.PD.SRC.E13 Reject Request - Invalid Object Position	Passed	Stable	2015-08-27
» TD.PD.SRC.E14 Atomic Message Sequence	Passed	RC	2015-09-23
» TD.PD.SRC.E15 Give_Source_Cap	Passed	RC	2015-09-23
» TD.PD.SRC.E16 PDO Transition	Passed	Beta	2015-11-06
USB PD Sink Tests	Passed with warnings		
» TD.PD.SNK.E1 SinkWaitCapTimer Deadline	Passed	Stable	2015-09-23
» TD.PD.SNK.E2 SinkWaitCapTimer Timeout	Passed	Stable	2015-09-23
» TD.PD.SNK.E3 Request Sent Timely	Passed	Stable	2015-08-27
» TD.PD.SNK.E4 Request Fields Checks	Passed	Stable	2015-08-27
» TD.PD.SNK.E5 SenderResponseTimer Deadline - Accept	Passed	Stable	2015-08-27
» TD.PD.SNK.E6 SenderResponseTimer Timeout - Accept	Passed	Stable	2015-08-27
» TD.PD.SNK.E7 PSTransitionTimer Deadline	Passed	Stable	2015-08-27
» TD.PD.SNK.E8 PSTransitionTimer Timeout	Passed	Stable	2015-08-27
» TD.PD.SNK.E9 GetSinkCap in Place of Accept	Passed	RC	2015-09-24
» TD.PD.SNK.E10 GetSinkCap in Place of PS_RDY	Passed with warnings	RC	2016-03-10
» TD.PD.SNK.E11 PDO Transition	Passed	Beta	2015-11-08
USB PD Provider / Consumer Tests	Passed		
» TD.PD.PC.E1 tSrcTransition Check	Passed	RC	2016-03-24
» TD.PD.PC.E2 PS_RDY Sent Timely	Passed	RC	2016-03-24
» TD.PD.PC.E3 PSSourceOnTimer Deadline	Passed	RC	2016-03-24
» TD.PD.PC.E4 PSSourceOnTimer Timeout	Passed	RC	2016-03-24
» TD.PD.PC.E5 tSwapSinkReady Check	Passed	RC	2016-03-24

		Test Status	Last Update
» TD.PD.PC.E6 Externally Powered Bit Usage	Not Applicable	RC	2016-04-28
» TD.PD.PC.E7 PDO Transition After PR_Swap	Passed	RC	2016-03-24
USB PD Consumer / Provider Tests	Passed		
» TD.PD.CP.E1 PSSourceOffTimer Deadline	Passed	RC	2016-03-24
» TD.PD.CP.E2 PSSourceOffTimer Timeout	Passed	RC	2016-03-24
» TD.PD.CP.E3 PS_RDY Sent Timely	Passed	RC	2016-03-24
» TD.PD.CP.E4 SwapSourceStartTimer Timeout	Passed	RC	2016-03-24
» TD.PD.CP.E5 PDO Transition After PR_Swap	Passed	RC	2016-03-24
USB PD VDM Tests for UFPs and Cables	Passed		
» TD.PD.VDMU.E1 Discover Identity Response	Passed	Stable	2015-08-18
» TD.PD.VDMU.E2 Discover SVIDs Response	Passed	Stable	2015-08-18
» TD.PD.VDMU.E3 Discover Modes Response	Passed	Stable	2015-08-18
» TD.PD.VDMU.E4 Enter Mode Response	Passed	Stable	2016-05-09
» TD.PD.VDMU.E5 Exit Mode Response	Passed	Stable	2016-05-09
» TD.PD.VDMU.E6 Discover Identity Response Time	Passed	Stable	2015-08-18
» TD.PD.VDMU.E7 Discover SVIDs Response Time	Passed	Stable	2015-08-18
» TD.PD.VDMU.E8 Discover Modes Response Time	Passed	Stable	2015-08-18
» TD.PD.VDMU.E9 Enter/Exit Mode Response Time	Passed	Stable	2015-08-18
» TD.PD.VDMU.E10 Discover Identity Wrong SVID	Passed	Stable	2015-08-18
» TD.PD.VDMU.E11 Discover SVIDs Wrong SVID	Passed	Stable	2015-08-18
» TD.PD.VDMU.E12 Discover Modes Wrong SVID	Passed	Stable	2015-08-18
» TD.PD.VDMU.E13 Enter Mode Wrong SVID	Passed	Stable	2015-08-18
» TD.PD.VDMU.E14 Exit Mode Wrong SVID	Passed	Stable	2015-08-18
» TD.PD.VDMU.E15 Applicability	Passed	Stable	2015-08-18
» TD.PD.VDMU.E16 Interruption by PD Command	Passed	Stable	2016-04-20
» TD.PD.VDMU.E17 Interruption by VDM Command	Passed	Stable	2016-05-09
» TD.PD.VDMU.E18 Data Role Swap Hard Reset	Passed	Stable	2015-08-18
DisplayPort Alt-Mode Tests for UFPs and Cables	Passed		
» TD.PD.DPU.E1 Enter Mode Response	Passed	Stable	2015-08-18
» TD.PD.DPU.E2 Status Update Response	Passed	Stable	2015-10-22
» TD.PD.DPU.E3 Time from Vbus/Vconn on to UFP Ready	Passed	Alpha	2016-03-14
DisplayPort Alt-Mode Tests for DFPs	Passed		
» TD.PD.DPD.E1 Cable Determination	Passed	Stable	2015-09-16
» TD.PD.DPD.E2 DP SVID in Arbitrary Location	Passed	Stable	2015-09-17
» TD.PD.DPD.E3 Status Update Presence	Passed	Stable	2015-09-16
» TD.PD.DPD.E4 Enter Mode Rejected	Passed	Stable	2015-09-16
» TD.PD.DPD.E5 Enter Mode Not Responded	Passed	Stable	2015-09-16
» TD.PD.DPD.E6 DisplayPort Not Connected	Passed	Stable	2015-09-16
» TD.PD.DPD.E7 Status Update Port Resolution	Not Applicable	Stable	2015-09-16
» TD.PD.DPD.E8 Not Compatible Connection	Passed	Stable	2015-10-28
» TD.PD.DPD.E9 Field Checks - DisplayPort Configure	Passed	Alpha	2016-03-10
USB PD Consistency Tests	Failed		
» TD.PD.VNDI.E1 VDM Identity	Failed	Stable	2015-09-24
» TD.PD.VNDI.E2 VDM SVIDs	Passed	Stable	2015-08-18
» TD.PD.VNDI.E3 VDM Modes	Passed	Stable	2015-08-18

		Test Status	Last Update
» TD.PD.VNDI.E4 SOP* Handling	Passed	Stable	2015-08-18
» TD.PD.VNDI.E5 Source Capabilities	Passed	Stable	2016-05-18
» TD.PD.VNDI.E6 Sink Capabilities	Passed	Stable	2016-05-18
» TD.PD.VNDI.E7 Accepts PR_Swap as Source	Passed	Stable	2016-03-14
» TD.PD.VNDI.E8 Accepts PR_Swap as Sink	Passed	Stable	2016-05-11
» TD.PD.VNDI.E9 Requests PR_Swap as Source	Passed	Stable	2016-02-10
» TD.PD.VNDI.E10 Requests PR_Swap as Sink	Passed	Stable	2015-08-18
» TD.PD.VNDI.E11 DisplayPort Alt-Modes	Passed	Stable	2015-10-22

MQP Test - Phy Test

Packet-Master USB-PDT Report on Lattice_Semiconductor DRP

GraphicUSB V4.84 -- Scripts PDT Rev:0.9.1.4

Date and time:	Test run on Monday, May 31, 2016 13:58:32
Vendor:	Lattice Semiconductor
Product:	DRP
Product version:	v1.0
Test ID:	10945

The following tests have been selected:

- BMC-PHY-TX-EYE
- BMC-PHY-RX-INT-REJ
- BMC-PHY-RX-BUSIDL
- BMC-PHY-TERM
- BMC-PHY-MSG

Summary

BMC-PHY-TX-EYE	
BMC-PHY-TX-EYE Primary	Passed
BMC-PHY-TX-EYE Secondary	Passed
BMC-PHY-RX-INT-REJ	
BMC-PHY-RX-INT-REJ	Passed
BMC-PHY-RX-INT-REJ Secondary	Passed
BMC-PHY-RX-BUSIDL	
BMC-PHY-RX-BUSIDL	Passed
BMC-PHY-RX-BUSIDL Secondary	Passed
BMC-PHY-TERM	
BMC-PHY-TERM	Passed
BMC-PHY-TERM Secondary	Passed
BMC-PHY-MSG	

BMC-PHY-MSG	Passed
BMC-PHY-MSG Secondary	Passed

USB-IF Summary	
BMC PHY Tx	Passed
BMC PHY Rx	Passed
BMC PHY Misc:	Passed
Protocol Specific:	
Power Specific:	
Secondary	Passed

MQP Test - Power Test

Packet-Master USB-PDT Report on Lattice_Semiconductor DRP

GraphicUSB V4.84 -- Scripts PDT Rev:0.9.1.4

Date and time:	Test run on Monday, May 31, 2016 14:05:23
Vendor:	Lattice Semiconductor
Product:	DRP
Product version:	v1.0
Test ID:	10945

The following tests have been selected:

- BMC-POW-SRC-LOAD-P-PC
- BMC-POW-SRC-LOAD-CP-ACC
- BMC-POW-SRC-TRANS-P-PC
- BMC-POW-SRC-TRANS-CP-ACC
- BMC-POW-SNK-TRANS-C-CP
- BMC-POW-SNK-TRANS-PC

Summary

BMC-POW-SRC-LOAD-P-PC	
BMC-POW-SRC-LOAD-P-PC	Passed
BMC-POW-SRC-LOAD-P-PC Secondary	Passed
BMC-POW-SRC-LOAD-CP-ACC	
BMC-POW-SRC-LOAD-CP-ACC	Passed
BMC-POW-SRC-LOAD-CP-ACC Secondary	Failed
BMC-POW-SRC-TRANS-P-PC	
BMC-POW-SRC-TRANS-P-PC	Passed
BMC-POW-SRC-TRANS-P-PC Secondary	Passed
BMC-POW-SRC-TRANS-CP-ACC	
BMC-POW-SRC-TRANS-CP-ACC	Passed
BMC-POW-SRC-TRANS-CP-ACC Secondary	Passed

BMC-POW-SNK-TRANS-C-CP	
BMC-POW-SNK-TRANS-C-CP	Passed
BMC-POW-SNK-TRANS-C-CP Secondary	Passed
BMC-POW-SNK-TRANS-PC	
BMC-POW-SNK-TRANS-PC	Passed
BMC-POW-SNK-TRANS-PC Secondary	Passed

USB-IF Summary	
BMC PHY Tx	
BMC PHY Rx	
BMC PHY Misc:	
Protocol Specific:	
Power Specific:	Passed
Secondary	Failed

MQP Test - Protocol Test

Packet-Master USB-PDT Report on Lattice_Semiconductor DRP

GraphicUSB V4.84 -- Scripts PDT Rev:0.9.1.4

Date and time:	Test run on Monday, May 31, 2016 14:03:29
Vendor:	Lattice Semiconductor
Product:	DRP
Product version:	v1.0
Test ID:	10945

The following tests have been selected:

- BMC-PROT-SEQ-GETCAPS
- BMC-PROT-SEQ-CHKCAB-P-PC
- BMC-PROT-SEQ-NOMRK-P-PC
- BMC-PROT-SEQ-CHKCAB-CP-ACC
- BMC-PROT-SEQ-NOMRK-CP-ACC
- BMC-PROT-SEQ-PRSWAP
- BMC-PROT-SEQ-DRSWAP
- BMC-PROT-SEQ-VCSWAP
- BMC-PROT-SEQ-DISCOV
- BMC-PROT-BIST-NOT-5V-SRC
- BMC-PROT-REV-NUM

Summary

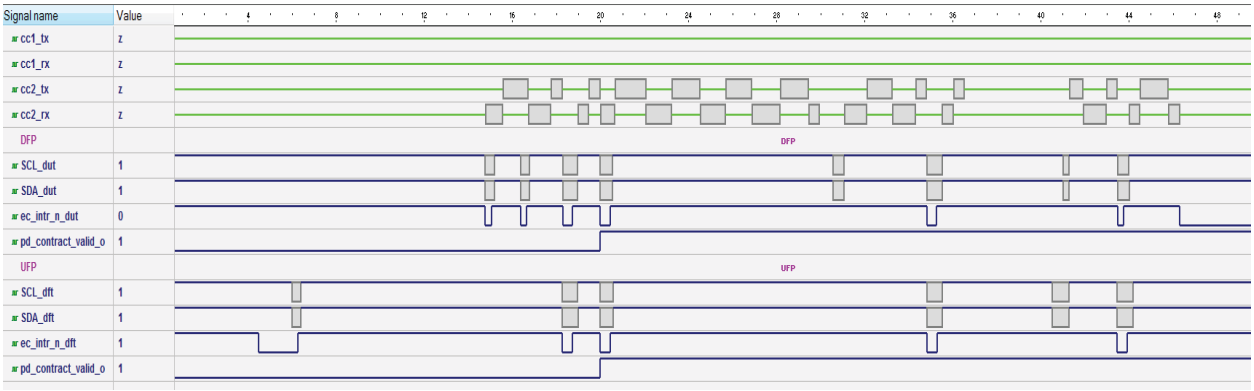
BMC-PROT-SEQ-GETCAPS	
BMC-PROT-SEQ-GETCAPS	Passed
BMC-PROT-SEQ-GETCAPS Secondary	Passed
BMC-PROT-SEQ-CHKCAB-P-PC	
BMC-PROT-SEQ-CHKCAB-P-PC	Passed
BMC-PROT-SEQ-CHKCAB-P-PC Secondary	Passed
BMC-PROT-SEQ-NOMRK-P-PC	
BMC-PROT-SEQ-NOMRK-P-PC	Passed
BMC-PROT-SEQ-NOMRK-P-PC Secondary	Passed
BMC-PROT-SEQ-CHKCAB-CP-ACC	
BMC-PROT-SEQ-CHKCAB-CP-ACC	Passed
BMC-PROT-SEQ-CHKCAB-CP-ACC Secondary	Passed
BMC-PROT-SEQ-NOMRK-CP-ACC	
BMC-PROT-SEQ-NOMRK-CP-ACC	Passed
BMC-PROT-SEQ-NOMRK-CP-ACC Secondary	Passed
BMC-PROT-SEQ-PRSWAP	
BMC-PROT-SEQ-DRSWAP	Passed
BMC-PROT-SEQ-DRSWAP Secondary	Passed
BMC-PROT-SEQ-DRSWAP	
BMC-PROT-SEQ-DRSWAP	Passed
BMC-PROT-SEQ-DRSWAP Secondary	Failed
BMC-PROT-SEQ-VCSWAP	
BMC-PROT-SEQ-VCSWAP	Passed
BMC-PROT-SEQ-VCSWAP Secondary	Passed
BMC-PROT-DISCOV	
BMC-PROT-DISCOV	Passed
BMC-PROT-DISCOV Secondary	Failed
BMC-PROT-REV-NUM	
BMC-PROT-REV-NUM	Passed
BMC-PROT-REV-NUM Secondary	Passed

USB-IF Summary	
BMC PHY Tx	
BMC PHY Rx	
BMC PHY Misc:	
Protocol Specific:	Passed
Power Specific:	
Secondary	Failed

Note: The failures shown in the reports are tester's bug and can be ignored.

Functional Simulation Results

Figure 19. Functional Simulation Waveform



ActiveHDL Console Results

```
# KERNEL: Asserting Reset
# KERNEL: De-asserting Reset
# KERNEL: Applying 2 kHz sawtooth input
# KERNEL:
# KERNEL: ---------------- Initial PD contract ----------------
# KERNEL:
# KERNEL: ###################### PD         ######################
# KERNEL:
# KERNEL: @            14788620ps                        >> SOURCE : SEND CAPABILITIES <<
# KERNEL: ********** Fixed supply match**************
# KERNEL: @            16085600ps                 3. SINK : SEND REQUEST
# KERNEL: @            17245220ps                 4. SOURCE : REQUEST RECEIVED
# KERNEL: ********** Source Capability Match **************
# KERNEL: ********** Source Comparison done **************
# KERNEL: @            17248420ps                        >> SOURCE : EVALUATE REQUEST <<
# KERNEL: @            17248420ps                 5. SOURCE : SEND ACCEPT
# KERNEL: @            18285600ps                 6. SINK : ACCEPT RECEIVED
# KERNEL:
# KERNEL: ###################### EC         ######################
# KERNEL:
# KERNEL:
# KERNEL:                          Power Transition Request Interrupt Received @UFP
# KERNEL:
# KERNEL:                                 Clear Interrupt Registers @UFP
# KERNEL:
# KERNEL:                          Power Transition Request Interrupt Received @DFP
# KERNEL:
# KERNEL:                                 Clear Interrupt Registers @DFP
# KERNEL:
# KERNEL:                          Set Power Transition Request Done in CTRL REG 1 @DFP
# KERNEL:
# KERNEL:                          Set Power Transition Request Done in CTRL REG 1 @UFP
# KERNEL:
# KERNEL: ###################### PD        ######################
# KERNEL:
# KERNEL: @            18983620ps                        >> SOURCE: POWER SUPPLY ADJUSTMENT <<
# KERNEL: @            18983620ps                 7. SOURCE : SEND PS_RDY
# KERNEL: @            20004000ps                 8. SINK : PS_RDY RECEIVED
# KERNEL:
# KERNEL: ###################### EC        ######################
# KERNEL:
# KERNEL:                                 PD contract established @UFP
# KERNEL:
# KERNEL:                                 Clear Interrupt Registers @UFP
# KERNEL:
# KERNEL:                                 PD contract established @DFP
# KERNEL:
# KERNEL:                                 Clear Interrupt Registers @DFP
# KERNEL:
# KERNEL: ---------------- New source PDO count update ----------------
# KERNEL:
# KERNEL: ###################### EC        ######################
# KERNEL:
# KERNEL:                                 Read PDO count @DFP
# KERNEL:
# KERNEL:
# KERNEL:                             PDO count @DFP = x46000001
# KERNEL:
# KERNEL:                                 Write Source PDO count update 'x86_00_00_09' @DFP
# KERNEL: @            31087620ps                        >> SOURCE : SEND CAPABILITIES <<
# KERNEL:
# KERNEL: ###################### PD         ######################
# KERNEL:
# KERNEL:
# KERNEL: ********** Fixed supply match**************
# KERNEL: @            32649600ps                 3. SINK : SEND REQUEST
# KERNEL: @            33810020ps                 4. SOURCE : REQUEST RECEIVED
# KERNEL: ********** Source Capability Match **************
# KERNEL: ********** Source Comparison done **************
# KERNEL: @            33813220ps                        >> SOURCE : EVALUATE REQUEST <<
```

```
# KERNEL: @            33813220ps                  5. SOURCE : SEND ACCEPT
# KERNEL: @            34847200ps                  6. SINK : ACCEPT RECEIVED
# KERNEL:
# KERNEL: ####################### EC        ######################
# KERNEL:
# KERNEL:
# KERNEL:                         Power Transition Request Interrupt Received @UFP
# KERNEL:
# KERNEL:                                   Clear Interrupt Registers @UFP
# KERNEL:
# KERNEL:                         Power Transition Request Interrupt Received @DFP
# KERNEL:
# KERNEL:                                   Clear Interrupt Registers @DFP
# KERNEL:
# KERNEL:                            Set Power Transition Request Done in CTRL REG 1 @DFP
# KERNEL:
# KERNEL:                            Set Power Transition Request Done in CTRL REG 1 @UFP
# KERNEL:
# KERNEL: ####################### PD         ######################
# KERNEL:
# KERNEL: @            35548220ps                       >> SOURCE: POWER SUPPLY ADJUSTMENT <<
# KERNEL: @            35548220ps                  7. SOURCE : SEND PS_RDY
# KERNEL: @            36568800ps                  8. SINK : PS_RDY RECEIVED
# KERNEL:
# KERNEL: ---------------- New Sink PDO number update ----------------
# KERNEL:
# KERNEL: ####################### EC        ######################
# KERNEL:
# KERNEL:                                   Read PDO count @UFP
# KERNEL:
# KERNEL:                      PDO count @UFP = x46000001
# KERNEL:
# KERNEL:                                   Write new Sink PDO number 'x46_00_00_0B' @UFP
# KERNEL:
# KERNEL: ####################### PD        ######################
# KERNEL: ********** Fixed supply match**************
# KERNEL:
# KERNEL: ********** Source Capability Match **************
# KERNEL: ********** Source Comparison done **************
# KERNEL: @            42470820ps                       >> SOURCE : EVALUATE REQUEST <<
# KERNEL: @            42470820ps                  5. SOURCE : SEND ACCEPT
# KERNEL: @            43504800ps                  6. SINK : ACCEPT RECEIVED
# KERNEL:
# KERNEL:  ####################### EC       ######################
# KERNEL:
# KERNEL:                         Power Transition Request Interrupt Received @DFP
# KERNEL:
# KERNEL:                                   Clear Interrupt Registers @DFP
# KERNEL:
# KERNEL:
# KERNEL:                         Power Transition Request Interrupt Received @UFP
# KERNEL:
# KERNEL:                                   Clear Interrupt Registers @UFP
# KERNEL:
# KERNEL:                            Set Power Transition Request Done in CTRL REG 1 @DFP
# KERNEL:
# KERNEL:                            Set Power Transition Request Done in CTRL REG 1 @UFP
# KERNEL:
# KERNEL: ####################### PD        ######################
# KERNEL:
# KERNEL: @            44037020ps                     >> SOURCE : POWER SUPPLY ADJUSTMENT <<
# KERNEL: @            44037020ps             7. SOURCE : SEND PS_RDY
# KERNEL: @            45056800ps             8. SINK : PS_RDY RECEIVED
```

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Date	Version	Change Summary
October 2016	1.4	Updated the Features section. — Revised features list.Table 1 — Updated Table 1, USB Type-C Device Table. Removed CD/PD PHY for Host/Devices solution.
		Updated Functional Descriptions section. — Removed mention of CD/PD PHY for host/devices. — Removed reference to Appendix A.
		Updated the Lattice Type-C Solutions section.
		Updated the Lattice Type-C Solutions section. Removed the CD/PD PHY for Host/Devices subsection.
		Updated the Test Results section. Added the Compliance Results sub-section.
		Removed Appendix A.
August 2015	1.3	Updated the Features section. — Removed 81 caBGA package. — Updated Table 1, USB Type-C Device Table. Revised heading to Package, Ball Pitch, Dimension and data. Removed the 81 BGA, 0.8 mm, 8 mm x 8 mm package.
		Updated the Lattice Type-C Solutions section. Revised the following diagrams: — Figure 6, USB CD/PD Charger (Captive or Non-captive Cable) Block Diagram. — Figure 7, USB CD/PD PHY for Host/Devices Block Diagram. — Figure 8, USB CD/PD for Hosts/Devices Block Diagram.
June 2015	1.2	Updated for Universal Serial Bus Type-C Cable and Connector Specification revision 1.1
		General update – removed version number references in specifications.
		Updated Introduction section. Added paragraph on specifications.
		Updated Features section. Removed specification revision numbers.
		Updated Functional Descriptions section. The following subsections are revised: — CC line vRd and vOpen Detection — V_{BUS} Detection — SS Switch Selection — DRP FSM — PD PHY — I^2C Slave Controller — Device Policy Manager (DPM) — Policy Engine (PE) — Proto Tx — Proto Rx — Hard Reset. Removed reference to USB PD specification.
		Updated Technical Support Assistance section.

Date	Version	Change Summary
March 2015	1.1	Updated CD or Cable Detect section. — Revised Table 4, USB Type-C DFP Connection States. — Revised Table 6, Voltage on UFP CC pins (Multiple DFP Current Advertisements).
		Updated Cable Attach/Detach Determination section. — Revised Figure 2, RP and RD Functional Model for a DRP-DRP. Changed 1M to 510K.
		Updated Dead Battery Detection/Unpowered Port Detection section. — Revised Figure 3, Clamp Voltage Based Device Detection for a Dead Battery/Unpowered Device.
		Updated CD PD for Charger section. — Revised heading to Figure 7, USB CD/PD Charger (Captive or Non-captive Cable) Block Diagram.
		Updated CD PD PHY for Hosts/Devices section. — Revised Figure 8, CD/PD PHY for Hosts/Devices Block Diagram. — Updated solution description.
February 2015	1.0	Initial release.