

## Introduction

This technical note provides general guidelines for a solder reflow and rework process for Lattice surface mount products. The data used in this document is based on IPC/JEDEC standards. Each board has its own profile which depends upon the reflow equipment used and the board design. The PCB must be individually characterized to find the reliable profile. This document covers SnPb, Pb-Free and Halogen-Free processes.

## Reflow

- Use caution when profiling to insure the maximum temperature difference between components is less than 10°C (7°C within an individual component).
- Forced convection reflow with nitrogen is preferred (with maximum oxygen content of 50-75 PPM).

## Inspection

- Pre-reflow: Use visual inspection to verify solder paste dispense location and quantity.
- Pick and place: Use machine vision as necessary to ensure proper component placement.
- Post reflow: Use electrical testing to verify solder joint formation (100% post-reflow visual inspection is not recommended).

## Cleaning Recommendations

- After solder reflow, printed circuit boards should be thoroughly cleaned and dried using standard cleaning equipment.
- Final rinse should be warm DI water (50° to 75°C) with resistivity of 0.2 Meg Ohms/cm or greater.
- After cleaning, boards should be baked for a minimum of 1 hour at 125°C to evaporate residual moisture.

## Rework Recommendations

Removal and replacement of SMT packages on printed circuit boards is fairly straightforward. However, reattachment or touch-up of SMT packages that have already been soldered to the board is not practical in most cases.

A few important criteria should be considered when choosing a rework system:

- Minimize the change in temperature across the solder joint array to promote good solder joint formation, minimize intermetallic growth, improve solderability and minimize component warpage.
- Minimize die temperature to prevent die delamination and wire bond failure.
- Minimize board temperature adjacent to the rework site to reduce intermetallic growth, prevent secondary reflow, and prevent possible component delamination.
- For boards with no internal ground plane, apply localized heat to the SMT package. When the solder is molten, remove package using appropriate vacuum tool.
- While the board is still hot, remove excess solder from the site using a vacuum desoldering system or a soldering iron and solder wicking material. Use care to avoid damaging the solder pads or the surrounding solder mask.
- For PCBs with internal ground plane(s), preheat the entire board to at least 80°C before removing the SMT packages.

- Use alcohol to remove residual flux, then wash the entire board using the standard board cleaning process before attempting to replace SMT components.

## BGA Reballing

BGA reballing is not recommended. Reballled BGA packages will void the original Lattice specifications.

## Pb-Free/Halogen-Free (RoHS-Compliant) Products

All Lattice Pb-Free products are also fully RoHS compliant. Similarly, all Lattice Halogen-free products are also Pb-Free and RoHS compliant. Lattice offers a broad range of Pb-Free and Halogen-Free (RoHS-compliant) products in a variety of package configurations. These packages include the Thin Quad Flat Pack (TQFP), Quad Flat Pack Saw-Singulated (QFNS), Fine Pitch BGA (fpBGA), Thin BGA (ftBGA), Chip-Scale BGA (csBGA), Ultra Chip-Scale BGA (ucBGA), Chip Array BGA (caBGA) and Flip Chip BGA (fcBGA).

## Peak Reflow Temperature (T<sub>P</sub>) by Package Size

Table 1 illustrates the peak reflow temperatures by package size. Refer to the [Package Diagrams](#) document and use maximum package dimensions to determine package thickness and volume.

**Table 1. Peak Reflow Temperature (T<sub>P</sub>)**

Classification	Package Thickness	Volume < 350 mm <sup>3</sup>	Volume = 350 - 2000 mm <sup>3</sup>	Volume > 2000 mm <sup>3</sup>
SnPb Package	< 2.5 mm	240 + 0/-5°C	225 + 0/-5°C	
	≤ 2.5 mm	225 + 0/-5°C		
Pb-Free and Halogen-Free Packages	< 1.6 mm	260 + 0/-5°C		
	1.6 mm to < 2.5 mm	260 + 0/-5°C	250 + 0/-5°C	245 + 0/-5°C
	≤ 2.5 mm	250 + 0/-5°C	245 + 0/-5°C	

Note: Package volume excludes external terminals (balls, bumps, lands, leads) and non-integral heat sinks.

Table 2 shows the peak reflow temperature for Lattice devices by package type and size.

**Table 2. Peak Reflow Temperature (T<sub>P</sub>) by Package Type and Size**

Package Type	Number of Leads/Balls	SnPb Package		Pb-Free / Halogen-Free Package (RoHS Compliant)	
		Moisture Sensitivity Level	Peak Reflow Temp. (+0/-5°C)	Moisture Sensitivity Level	Peak Reflow Temp. (+0/-5°C)
caBGA	49	3	240	Not Available	
	100				
	256			3	260
	332			Not Available	
csBGA	56	3	240	3	260
	64	Not Available			
	100	3	240		
	132				
	144				
ucBGA	64	Not Available		3	260
	132				
fcBGA	1020	4	225	4	245
	1152				
	1704				

Table 2. Peak Reflow Temperature (TP) by Package Type and Size (Continued)

Package Type	Number of Leads/Balls	SnPb Package		Pb-Free / Halogen-Free Package (RoHS Compliant)	
		Moisture Sensitivity Level	Peak Reflow Temp. (+0/-5°C)	Moisture Sensitivity Level	Peak Reflow Temp. (+0/-5°C)
fpBGA	100	3	240	3	260
	144			Not Available	
	208	3	225	3	250
	256				
	388			Not Available	
	416			Not Available	
	484			Not Available	
	516			Not Available	
	672			Not Available	
	676			Not Available	
	680			Not Available	
	900			Not Available	
	1152	Not Available			
1156	Not Available				
fpSBGA	680	3	225	Not Available	
ftBGA	208	Not Available		3	260
	256 (Option 1) <sup>1</sup>	3	225		
	256 (Option 2) <sup>2</sup>	Not Available		3	250
	324	3	225	3	260
TQFP (Thickness: 1.4mm)	48	3	240	3	260
	64				
	100				
	128		256		
	144				
	176				
TQFP (Thickness: 1.0mm)	44	3	240	3	260
	48				
BGA	256	3	225	Not Available	
	272				
	352				
	388				
PLCC	20	1	225	1	250
	28			1	245
	44	3	225	3	245
	68			Not Available	
	84			4	245
PQFP	100	3	225	3	245
	120			Not Available	
	128			Not Available	
	160			Not Available	
	208			3	245

**Table 2. Peak Reflow Temperature (TP) by Package Type and Size (Continued)**

Package Type	Number of Leads/Balls	SnPb Package		Pb-Free / Halogen-Free Package (RoHS Compliant)	
		Moisture Sensitivity Level	Peak Reflow Temp. (+0/-5°C)	Moisture Sensitivity Level	Peak Reflow Temp. (+0/-5°C)
QFNS	24	Not Available		1	260
	32	1	240		
	48	Not Available		3	260
	64				
SBGA	256	3	225	Not Available	
	320				
	352				
	432				
SSOP	28	1	225	Not Available	
WLCSP	25	Not Available		1	260

1. ispMACH 4000, MachXO2, MachXO, LatticeXP2.  
2. LatticeECP3.

## Reflow Profile for SMT Packages

The typical reflow process includes four phases.

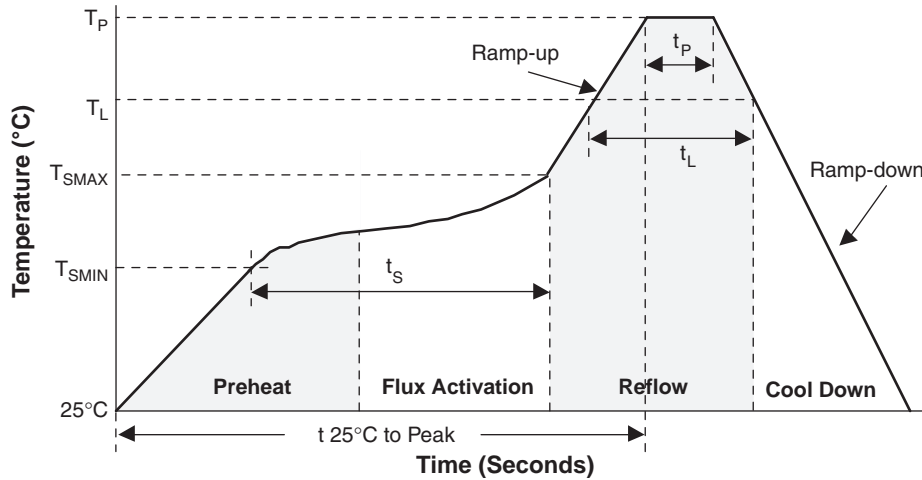
1. **Preheat** – Brings the assembly from 25°C to  $T_S$ . During this phase the solvent evaporates from the solder paste. Preheat temperature ramp rate should be less than 2°C/second to avoid solder ball spattering and bridging.
  - Solder Ball Spattering – The most common solder balling defect is spattering which is caused by explosive evaporation of solvents. It can be eliminated by a slower temperature rise in the preheat phase.
  - Bridging – Often seen on fine pitch components and usually caused by inaccurate or splashy screen printing. But it can also be a result of solder paste slumping caused by rapid temperature rise in the preheat phase.
2. **Flux Activation** – The temperature rises slowly and reaches a point at which the flux completely wets the surfaces to be soldered.
3. **Reflow** – In this phase, the temperature rises to a level sufficient to reflow the solder. The flux wicks surface oxides and contaminants away from the melted solder, resulting in a clean solder joint.
4. **Cool Down** – Ramp down rate should be as fast as possible in order to control grain size, but should not exceed 6°C/second.

Table 3 and Figure 1 describe the reflow profile.

**Table 3. Reflow Profiles**

Parameter	Description	SnPb Package	Pb-Free and Halogen-Free Packages
Ramp-Up	Average Ramp-Up Rate ( $T_{S_{MAX}}$ to $T_P$ )	3°C/second max.	3°C/second max.
$T_{S_{MIN}}$	Preheat Peak Min. Temperature	100°C	150°C
$T_{S_{MAX}}$	Preheat Peak Max. Temperature	150°C	200°C
$t_S$	Time between $T_{S_{MIN}}$ and $T_{S_{MAX}}$	60-120 seconds	60-120 seconds
$T_L$	Solder Melting Point	183°C	217°C
$t_L$	Time Maintained above $T_L$	60-150 seconds	60-150 seconds
$t_P$	Time within 5°C of Peak Temperature	10-30 seconds	20-40 seconds
Ramp-Down	Ramp-Down Rate	6°C/second max.	6°C/second max.
$t_{25^\circ\text{C to } T_P}$	Time from 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Figure 1. Thermal Reflow Profile



### Technical Support Assistance

Hotline: 1-800-LATTICE (North America)  
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 e-mail: techsupport@latticesemi.com  
 Internet: [www.latticesemi.com](http://www.latticesemi.com)

### Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
April 2008	02.2	Updated Peak Reflow Temperature ( $T_P$ ) by Package Type and Size table.
June 2009	02.3	Updated QFN information in Peak Reflow Temperature ( $T_P$ ) by Package Type and Size, SnPb Packages table.
		Updated QFN information in Peak Reflow Temperature ( $T_P$ ) by Package Type and Size, Pb-Free Packages table.
November 2010	02.4	Updated for Halogen-Free package support.
June 2011	02.5	Updated document to include 25 WLCSP package.