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Lattice Launches Low-Cost, Non-Volatile LatticeXP FPGA Family 'No Compromise' Flash + SRAM Based FPGAs are Instant- on, Infinitely Reconfigurable

On February 28th Lattice announced its new LatticeXP™ devices, which combine a low-cost FPGA architecture with non-volatile, infinitely reconfigurable ispXP™ (eXpanded Programmability) technology. The LatticeXP devices deliver the benefits of instant-on operation, excellent security and a single-chip implementation and provide cost-effective alternatives to SRAM-based FPGAs and their associated boot memories. Through advanced 130nm Flash silicon technology, an optimized architecture and proprietary circuit design, die sizes of the new LatticeXP devices have been reduced over 80% compared to the previous generation of Lattice non-volatile FPGAs. First samples of the 10K Look-Up Table (LUT) LatticeXP10 device are now available with the remaining four family members planned for second quarter availability.

LatticeXP devices are implemented on a cost effective, low-k, 130nm CMOS Flash process using copper metallization. The technology was co-developed by Fujitsu Limited and Lattice Semiconductor. Production wafers are fabricated by Fujitsu in their state-of-the-art wafer fab. LatticeXP devices support operation from 1.2V, 1.8V, 2.5V or 3.3V power supplies.

Best of Both Worlds: ispXP Technology

The ispXP technology used in the LatticeXP devices combines SRAM and non-volatile Flash memory to deliver an FPGA that is both non-volatile and infinitely reconfigurable. The SRAM-based memory cells control the operation of the device logic and are loaded from the on-chip Flash memory in less than 1mS at power-up, providing instant-on capability, or boot up on user command. The products can also be configured via a microprocessor interface, referred to as the sysCONFIG™ interface, or the JTAG interface.

Unlike traditional SRAM-based FPGAs, the



LatticeXP device does not require an external boot memory and so provides a single-chip solution with the associated benefits of reduced board area and simplified system manufacture. The absence of an external boot device also eliminates the need for an external bitstream at boot up and the possibility of bitstream snooping, a major security concern with SRAM FPGAs. Security features prohibit bitstream readback from the SRAM and Flash sections of the devices to further enhance security.

Optimized Architecture for Cost-Conscious, High Volume Designs

The LatticeXP architecture was developed concurrently, and from the "ground up," with that of the previously announced LatticeECP™ and LatticeEC™ FPGAs. As with the low-cost LatticeECP/EC devices, all LatticeXP architectural elements such as logic blocks, I/O capabilities including DDR support and embedded memory, among others, were evaluated in the context of their targeted high-

(Please See Page 2)

(LatticeXP FPGA Family, Continued)

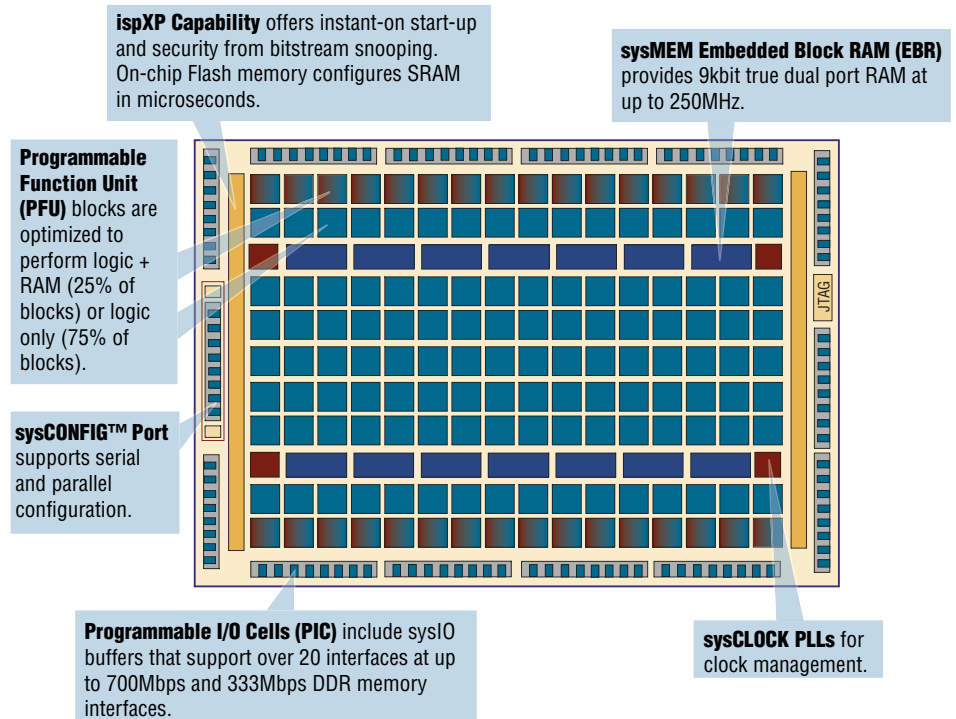
volume applications as the devices were defined. The feature sets were then precisely sculpted to be neither excessive (driving up cost) nor “bare bones” (limiting the application range) in order to maximize their broad adoption. The resulting combination of a superior streamlined architecture, compact circuit design and production-proven technology found in the LatticeXP devices allows them to provide the benefits of non-volatile, infinitely reconfigurable FPGAs and to be cost-effective alternatives to SRAM-based FPGAs and their associated boot memories.

A Closer Look: LatticeXP Optimized Architecture

- Based upon industry-standard, synthesis-friendly 4-input look-up table (LUT) logic blocks.
- Twenty-five percent of the logic blocks contain distributed memory, an optimization that reduces cost while supporting the vast majority of application requirements for small amounts of distributed memory.
- The availability of sysCLOCK™ Phase Locked Loops (PLLs) and Embedded Block RAMs (EBRs) allows designers to reduce costs further by integrating these functions within the FPGA, eliminating external discrete devices.
- Advanced sysIO™ buffer capability supports standards such as LVCMOS, LVDS, LVTTTL and PCI, as well as SSTL and HSTL, allowing users to easily and efficiently interface to the industry’s most popular bus standards. These standards were carefully selected to maximize application range while minimizing die area.
- The LatticeXP devices have dedicated circuitry to simplify DDR memory interfaces, while providing the highest performance, integration, signal integrity and ease of design for FPGAs in this class. DDR memory has become the low-cost memory of choice: estimates suggest DDR represented 75% of DRAM bits shipped in 2004, up from 39% in 2002.

LatticeXP Features

Feature	LFXP3	LFXP6	LFXP10	LFXP15	LFXP20
PFU/PFF Rows	16	24	32	40	44
PFU/PFF Columns	24	30	38	46	56
Number of PFUs/PFFs	384	720	1216	1932	2464
LUTs (K)	3.1	5.8	9.7	15.4	19.7
Distributed RAM (K Bits)	12	23	39	61	79
EBR Block SRAM (K Bits)	54	90	216	288	414
Number of EBR SRAM Rows	1	1	2	2	2
Number of EBR SRAM Blocks	6	10	24	32	46
VCC Voltage (V) Options	1.2/1.8 2.5/3.3V	1.2/1.8 2.5/3.3V	1.2/1.8 2.5/3.3V	1.2/1.8 2.5/3.3V	1.2/1.8 2.5/3.3V
Number of PLLs	2	2	4	4	4
Maximum Number of I/Os	136	188	244	300	340



LatticeXP Block Diagram

Design Tools and IP Support

In addition to a common FPGA architecture, the LatticeECP/EC and LatticeXP devices share a common design methodology and design tool flow supported by the Lattice ispLEVER design tool suite. Lattice ispLEVER software provides designers with access, in one software package, to all Lattice digital devices and includes synthesis support using

Mentor Graphics Precision RTL and Synplicity Synplify design tools. The ispLEVER 4.2 Service Pack 1 provides initial LatticeXP support.

An extensive range of IP (intellectual property) cores, particularly suited for high-volume applications, will be available from both Lattice and its IP partners. Complete details of IP support will be announced throughout 2005.

Lattice Announces Addition of Precision Power Manager to Programmable Mixed-Signal Product Portfolio

New Device Monitors Power Supply Voltages Down to 0.7V with 0.5% Precision

Lattice has extended its revolutionary ispPAC® Power Manager programmable mixed-signal product family with the production release of the Precision Power Manager Power1208P1 device. The Power1208P1 device, like its predecessor the Power1208, provides a complete solution for printed circuit board (PCB) power sequencing and management through an optimized set of programmable digital and analog functions. The Power1208P1 also extends the power and versatility of the Lattice Power Manager products: the analog inputs are capable of monitoring power supplies with voltages down to 0.67V, and are able to detect faults with greater than 0.5% precision. In addition, the Precision Power Manager can detect a power-off condition (i.e., power supply voltage less than 80mV). The Power1208P1 is pin compatible with the existing Power1208, and is available in a compact 44-pin Thin Quad Flat Pack (TQFP) package.

Increasing Emphasis on Precise Fault Detection

The complexity of power supply management has increased dramatically in recent years as the number of voltages found on the typical PCB has risen sharply. The use of core power supply voltages less than the standard 1.2V is becoming more common. Further, advanced integrated circuit tolerance of power supply voltage variation is also tightening. The ability of the Power1208P1 to simultaneously monitor all 12 power supply inputs provides rapid, accurate power supply fault detection, reducing fault propagation and consequently improving overall system reliability.

Managing today's power supply voltages with greater precision can only be achieved by using mixed-signal devices with higher accuracy. With the addition of the Power1208P1 device, designers can now employ our standardized power management



approach that includes PCBs that use power supplies of 1.2V or less.

About the Power1208P1

The Power1208P1 features 12 high precision analog power monitor inputs. Each analog input has programmable threshold (384 steps + power supply discharge detection) synchronous comparators with a fault detection precision of 0.5%. In addition, the 1208P1 device is equipped with on-chip programmable voltage references for supply monitoring, four noise-immune digital inputs and four open-drain digital outputs for system control interfacing, four programmable timers with an on-chip 1 MHz oscillator for delay control and a 16-macrocell Complex PLD (CPLD) to implement sequencing and control functions. The Power1208P1 is ruggedized to operate reliably in noisy power supply environments from 2.7V to 5.5V.

Lattice Power Manager devices provide a standard, off-the-shelf programmable mixed-signal solution for power management that enhances reliability and speeds time-to-market. Analog features such as input comparator thresholds and digital functions such as supply control sequences are programmed into non-volatile E²CMOS® elements on the devices using an IEEE1149.1 boundary scan protocol.

Applications for Power Manager devices include telecom and networking systems, storage systems, servers, test equipment and automotive electronics. Programmable features make Power Manager devices ideal for controlling multiple power supplies in conjunction with a wide range of regulator and switching technologies. Together with N-channel switching FETs, LDO (Low Drop Out) regulators, and/or DC-DC convertors (power bricks), the Power1208P1, Power1208 and Power604 devices provide compact, flexible power supply control solutions.

PAC-Designer® Version 3.4 Supports Enhanced Instruction Set LogiBuilder

The Precision Power Manager device is supported by the latest version of PAC-Designer software, an intuitive schematic design entry and simulation tool. Complex sequencing and monitoring functionality can be efficiently designed through easy-to-use pull-down menus in PAC-Designer's LogiBuilder module. The latest version of the tool features a new and improved instruction set that enables the user to implement complex functionality more efficiently. Designs can be completely verified using the tool's built-in waveform simulator. The PAC-Designer software is available for download from the Lattice web site at www.latticesemi.com.

The PACsysPOWR1208P1 evaluation kit enables designers to quickly build prototypes of their circuit implementations using the Power1208P1 in order to verify functionality. Designs implemented using the PAC-Designer software are downloaded into the device through a serial ispDOWNLOAD® cable that connects to a PC's parallel port. The kit contains an evaluation board for an ispPAC Power Manager device, an ispDOWNLOAD cable and the PAC-Designer version 3.3 software.

Final Member of ispClock5600 Family Released to Production

Lattice recently released the ispClock5610 device, the latest member of the ispClock5600 family, to production.

These new ispClock5600 devices, while pin compatible with the previously announced ispClock5500 devices, offer higher performance and additional functionality. For example, the ispClock5600 devices support external feedback for the PLL to support designs that require the generated output clock(s) to be phase aligned with the input clock. The first devices in the ispClock5600 family, the 10-output ispClock5610 and 20-output ispClock5620, combine a high-performance clock generator with a flexible, Universal Fan-out Buffer. The on-chip, zero-delay clock generator can provide up to five clock frequencies, ranging from 10MHz to 320MHz, using a high-performance PLL and clock multiply and divide facilities. The Universal Fan-out Buffer can drive up to 20 clock nets using either single-ended or differential signaling, with individual output control for improved signal and timing integrity.



Upgrade ispClock5500 Designs to ispClock5600 at No Extra Cost

Traditionally, Lattice Semiconductor has encouraged customers to take advantage of the improved performance of newer generation products at no extra cost. Because performance increase is achieved by replacing the PLL in the ispClock5500 device, the ispClock5600 devices can replace

the ispClock5500 devices without any circuit board layout changes. Older designs can easily be transferred into the ispClock5600 using PAC-Designer 3.4 with push-button convenience.

For additional information on the ispClock5600 family, visit the Lattice web site at www.latticesemi.com or contact your local Lattice sales representative.

ispClock Attributes Table

Feature	ispClock5500 Family		ispClock5600 Family	
	ispClock5510	ispClock5520	ispClock5610	ispClock5620
Input & Output Frequency Range	10-320MHz	10-320MHz	10-320MHz	10-320MHz
Programmable Input & Output Interface Types	LVTTTL, LVCMOS, SSTL, HSTL, LVDS, LVPECL	LVTTTL, LVCMOS, SSTL, HSTL, LVDS, LVPECL	LVTTTL, LVCMOS, SSTL, HSTL, LVDS, LVPECL	LVTTTL, LVCMOS, SSTL, HSTL, LVDS, LVPECL
Outputs	10	20	10	20
Feedback	Internal	Internal	Internal/External	Internal/External
Output-Output Skew (Max.)	50ps	50ps	50ps	50ps
Maximum Cycle-Cycle Jitter	70ps (peak-peak)	70ps (peak-peak)	60ps (peak-peak)	60ps (peak-peak)
Maximum RMS Period Jitter	14ps	14ps	10ps	10ps
Frequencies Generated	5	5	5	5
Programmable Skew	195ps to 12ns	195ps to 12ns	195ps to 12ns	195ps to 12ns
Programmable Termination	40 to 70Ω	40 to 70Ω	40 to 70Ω	40 to 70Ω
Package	48-pin TQFP	100-pin TQFP	48-pin TQFP	100-pin TQFP
Ordering Part Number	ispPAC-CLK5510V-01T48C	ispPAC-CLK5520V-01T100C	ispPAC-CLK5610V-01T48C	ispPAC-CLK5620V-01T100C

ispLEVER's New Model Year Provides Improved Performance and Features

ispLEVER 5.0 like many 2005 year automobiles, provides horsepower where it counts and features that would make a luxury sedan green with envy. The new version replaces version 4.2 and provides improvements in most every facet of the design environment.

Horsepower Where It Counts

The engines that optimize and implement your design have been tuned and some cases supercharged. A big benefit to users of ispLEVER 5.0 will be access to Mentor Graphics Precision RTL Synthesis. This next generation product includes the latest RTL optimization and FPGA targeting algorithms to provide you with the best quality of results possible. Another great feature of Precision RTL Synthesis is the analysis capabilities like RTL and technology schematic viewing that have traditionally only been available in more expensive versions of the product.

Fans of logic synthesis from Synplicity won't be disappointed in this release since Lattice has upgraded Synplify for Lattice to version 8.0 to include the latest device support and outstanding performance and speed users have come to expect.

Users of ispLEVER 5.0 will see significant gains in place-and-route

speed and quality-of-results over ispLEVER 4.2 and many benchmarks demonstrate upwards of 30% maximum operating frequency gains (f_{MAX}) with no additional placement effort or routing passes required.

Power Features for Design and Analysis

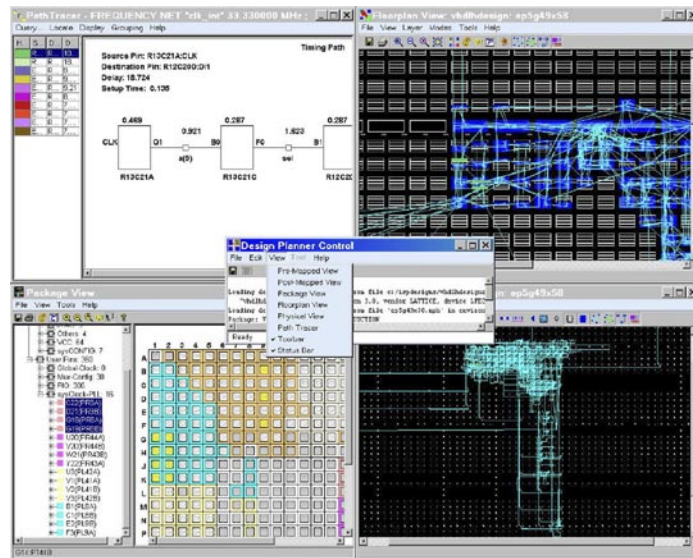
A significant redesign of the ispLEVER Floorplanner application provides a new window manager called the Design Planner that allows you to see many views in parallel,

a more intuitive display of floorplan elements like slices, EBRs, PLLs and sysDSP™ blocks, as well as dramatic load time improvement. Even diehard lovers of the EPIC Chip Editor will appreciate the visualization capabilities and speed.

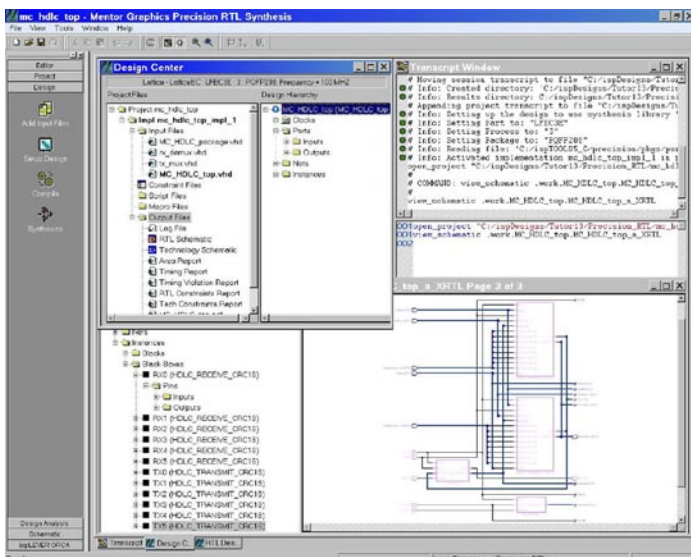
The Power Calculator application for power estimation provides even more real-world feedback in ispLEVER 5.0 with the new ability to import value change dump (VCD) information produced by ModelSim. This allows great correlation between your functional coverage and power analysis.

Design Guide Consolidates Expert Advice

In ispLEVER 5.0 the Lattice applications and technical publications teams are proud to introduce the FPGA Design Guide for Lattice Semiconductor. This book provides loads of advice from the Lattice applications field and factory staff in one easy to use reference. The guide covers subjects critical to both new and experienced Lattice FPGA designers including: migration of Altera and Xilinx FPGA designs, DSP design guidelines, HDL coding guidelines, place and route for timing closure, and on-chip debugging and analysis. Rationale, strategy and



ispLEVER 5.0 Floorplanner



Mentor Graphics Precision RTL for Lattice

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(ispLEVER 5.0, Continued)

high-level concepts are covered and it makes a great companion to the online help for each ispLEVER design tool. Early reviews indicate that these “big picture” topics go a long way toward helping designers adopt Lattice FPGAs and are considered essential to your desktop collection.

ispLEVER-Starter

ispLEVER-Starter is Lattice’s introductory ispLEVER configuration, intended for evaluation and student users. Still, ispLEVER-Starter is a complete design tool package, and includes everything required to take a design from concept to a programmed solution. With ispLEVER 5.0, the ispLEVER-Starter configuration will be expanded to support higher density FPGAs, and more device families. Visit the Lattice Semiconductor web site for more details about ispLEVER-Starter at: www.latticesemi.com/starter.

ispVM® System 15.0

ispVM System is the comprehensive programming management tool that helps you download your ispLEVER design to a programmable device. The newest release, ispVM 15.0, is included with ispLEVER 5.0 or is available as a download from the Lattice web site. ispVM System 15.0 includes:

- Support for the new LatticeXP FPGA technology
- Updates to the Universal File Writer (translates different programming file formats)
- Expanded SPI Flash programming support
- SPI Flash IP daisy chain enhancements

Precision RTL Synthesis Tools Power Your FPGA Design

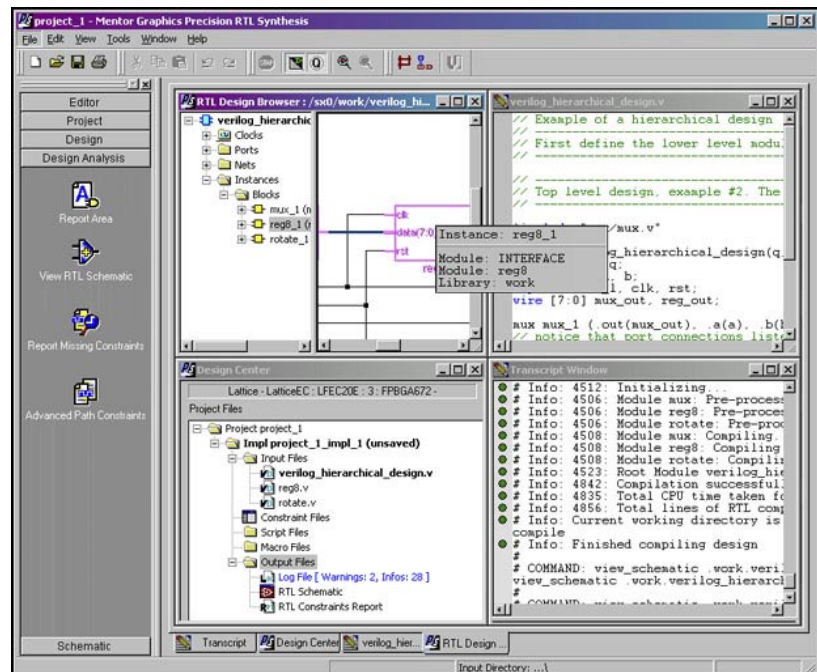
To help you get the most from your FPGA design, Lattice is committed to providing the best third-party tools as standard features of the ispLEVER design flow. This commitment continues with the addition of Precision RTL Synthesis from Mentor Graphics.

Precision RTL is Mentor Graphics premier FPGA synthesis environment. It includes a new set of features and tools wrapped in an intuitive user interface to help you achieve optimal design performance and maximize your productivity.

Precision RTL can be run via the ispLEVER Project Navigator or in stand-alone mode. In stand-alone

mode, the design flow is controlled through a simple, yet powerful Design Bar that guides you through all steps in the design process. With the schematic RTL view, you can visualize and optimize the intricate structure of your RTL connections. Precision RTL also helps automate complex constraint assignment and analysis and can even help identify missing constraints. The PreciseTime feature helps you quickly evaluate and analyze the timing results of numerous “what if” scenarios.

Starting with the ispLEVER 5.0 release, Precision RTL synthesis is included with the ispLEVER installation.



Mentor Graphics Precision RTL for Lattice

Two Evaluation Boards Support New LatticeXP Family

Lattice is pleased to offer a pair of new development boards specially designed for the LatticeXP FPGA technology. These boards provide ready-made platforms to help you evaluate the features and performance of the LatticeXP technology or to aid in the development of your application.

LatticeXP Standard Evaluation Board

The LatticeXP Standard evaluation Board was designed for basic evaluation of the LatticeXP FPGA in an operating environment that's ready to go. Each board features a LatticeXP10C device in the 256 fpBGA package. Power can be provided from a standard 5V AC adapter, or from other external sources. On-board regulators are included to supply 3.3V and/or other adjustable voltages to the device. The LatticeXP device can be configured directly with a Lattice ispDOWNLOAD Cable and ispVM System software (downloadable from the Lattice web site). The system clock can be provided from an on-board 33MHz oscillator or an external source. The board also includes mounts for SMA/SMB connectors of the user's preference. These can be used for high-frequency signals to and from the clock, PLL or I/O on the LatticeXP device. Additionally, the board features an extensive prototyping area with access to all the device's general purpose I/O. Finally, a number of general-purpose headers, LEDs and DIP switches are provided to support additional custom configuration and feedback.

LatticeXP Advanced Evaluation Board

The LatticeXP Advanced evaluation board is designed for detailed evaluation of the LatticeXP10 device, specifically IP-related functions and interfaces. At the heart of this board is a LatticeXP10 FPGA in a 388 fpBGA package. The LatticeXP Advanced evaluation board includes 3.3V, 2.5V and 1.2V power planes. Most of the basic features of the LatticeXP Stan-

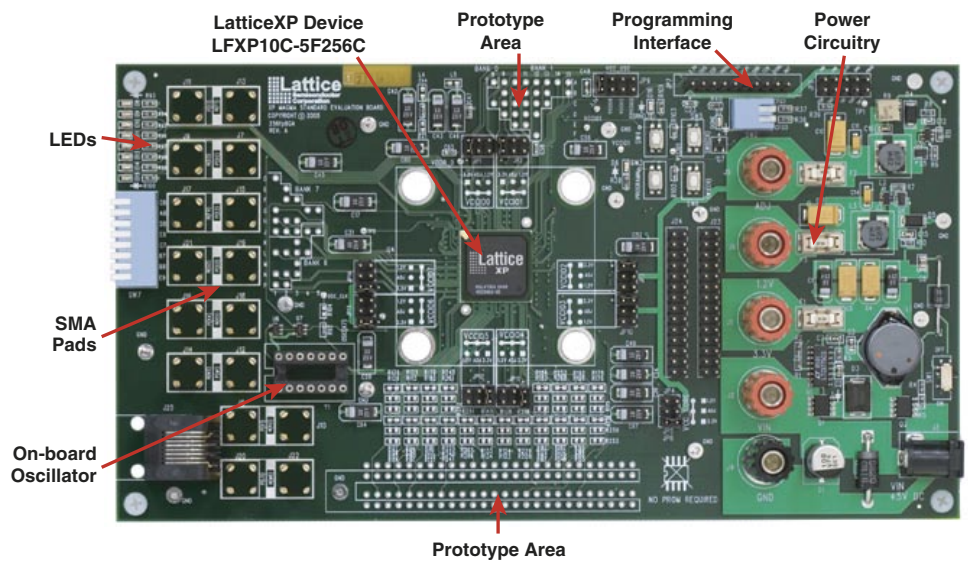
dard evaluation board (described above) are also included on this board, though the LatticeXP Advanced evaluation board has more limited prototyping access.

The LatticeXP Advanced evaluation board also includes an SODIMM socket supporting 16-bit, 166MHz, 200-pin DDR SDRAM (SDRAM module not included). A 256Mb (8Mb x 4 x 8-bit) FCRAM device is also included

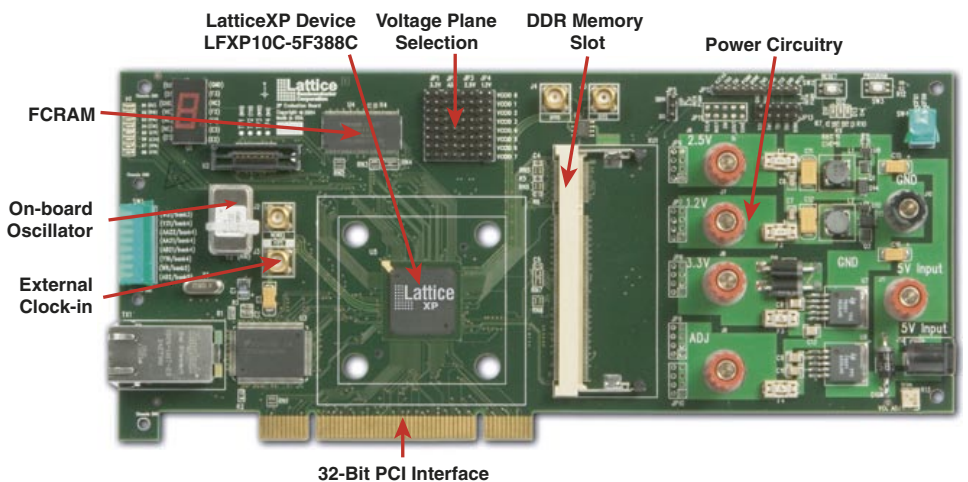
on the board. The board features a 32-bit PCI interface, conforming to the PCI form-factor standard.

For More Information

Additional information about all Lattice evaluation boards is available on the Lattice Semiconductor web site at www.latticesemi.com/boards.



LatticeXP Standard Evaluation Board



LatticeXP Advanced Evaluation Board

Worldwide Exhibitions Showcase Latest Lattice Products

2005 has proven to be a busy year for Lattice employees worldwide. Participation in several international conferences and exhibitions has provided an excellent opportunity for Lattice to show off its latest devices and design tools to an eager market.

Lattice's presence at these events is significant for our customers as well as for Lattice, solidifying our commitment to provide design engineers with high performance, low cost programmable products.

Electronics Design & Solutions Fair Yokohama, Japan January 2005

Lattice participated in the Electronic Design and Solutions Fair January 27-28 in Yokohama, Japan. In its fifth year, EDSFair 2005 is Asia's leading trade show for suppliers of EDA, FPGA, System-On-Chip and IP solutions. Since its inception, EDSFair has won strong global acclaim as the largest exhibition of its kind in Asia.

Over the course of two days, the Lattice booth was visited by nearly 100 engineering professionals from companies such as Fujitsu, NEC, Canon, Yazaki and Korg. Lattice was represented at the booth by all of our Lattice-Japan sales managers, FAEs and dedicated distributor sales teams. The turnout on the second day was even stronger than the first.

Major portions of the show floor were occupied by companies such as Synopsis, Mentor Graphics, Cadence, HP, Sun Microsystems, LSI Logic, Fujitsu and NEC.

The Fujitsu booth included information on foundry services which prominently featured the Lattice-Fujitsu partnership and three LatticeECP/EC devices were displayed.

In addition to the Lattice booth, Lattice employees also presented four seminars: "Simplified DDR Controller Design Using the LatticeECP/EC FPGA Family", "Implementing DSP Functions in the Low-Cost LatticeECP FPGA", "Using SPI Serial FLASH for Low-Cost FPGA Configuration" and



In February, Lattice Participated in the Embedded World Conference in Nuremberg, Germany



Design Engineers Learned about Lattice's New FPGA Families at the Electronics Design & Solutions Fair in Yokohama, Japan

"Designing Clock Nets Without Buffers, Trace Compensation or Delay Lines."

Embedded World Conference Nuremberg, Germany February 2005

Spanning three days from February 22-24, 2005, the Embedded World Conference is an annual event held in Nuremberg, Germany. Over the

years, the show has grown to become a major European conference that has begun to attract an audience outside its European roots. This year's conference set a record with 487 exhibitors from 24 countries, confirming its position as the top international event for the embedded industry.

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(Worldwide Exhibitions, Continued)

Along with three days of conference proceedings, displays from various exhibitors spanned four large exhibition halls, each with a different theme (silicon, software development tools, IP, etc.). This was a large event by any standards; each hall was abuzz with engineers eager for technical solutions to design engineering problems.

Internationally renowned speakers presented papers on the latest embedded systems topics in numerous sessions, tutorials and workshops. Johannes Fottner, Lattice Field Applications Engineer, presented a paper on Digital Signal Processing.

The show coincided with the launch of the new LatticeXP non-volatile FPGA device family. A press conference led by Lattice Vice President of Marketing, Stan Kopec, included a press presentation and questions fielded from a large contingency of editors from the European technical press.

Embedded Systems Conference San Francisco, California, USA March 2005

Lattice participated in the Embedded Systems Conference 2005 March 8-10 in San Francisco. Now in its 17th year, the Embedded Systems Conference has a strong reputation for offering high-caliber, solutions-oriented technical sessions. The 2005 technical program was the most robust program offered to-date. With 132 technical classes, 16 full-day tutorials, seven design seminars and numerous vendor workshops, it is the largest systems design technical program offered in North America. The conference experienced record attendance on the final day of the show, including approximately 10,000 attendees comprised of engineers and engineering managers, technology analysts, media representatives and many others.

Design engineers worldwide attend this conference not only to learn about cutting edge products from leading companies (systems manufacturers, board manufacturers, silicon vendors and design houses) but also to attend



The Lattice Booth was a Popular Stop for Attendees at the Embedded Systems Conference in San Francisco

the design seminars on analog power, DSP, silicon design, 3G cellular design, network design, and much more.

Because LatticeECP/EC products were finalists in this year's EE Times Annual Creativity in Electronics (ACE) Awards, Lattice Semiconductor also participated in the prestigious gala awards dinner. The ACE Awards honor the people, companies and products that demonstrate industry leadership.

Numerous new products were demonstrated in the Lattice vendor booth on the exhibit floor, including the LatticeECP/EC and LatticeXP FPGAs and the ispClock and ispPAC Power Manager mixed signal device families. The high performance DDR interface and in-system programmability of the newly announced LatticeXP products as well as the advantages of LatticeEC/ECP low cost FPGAs were the stars of the show at the Lattice booth. Many engineers requested ispLEVER and PAC-Designer software tool demos as well.

Lattice to Present at Mentor Graphics' User2User Conference

Lattice invites you to attend this unique conference organized and hosted by the Mentor User Group (MUG), April 27-29, 2005 in Santa Clara, CA. What makes this conference unique is that its organization, subject matter, and presenters are determined solely by the user group.

Lattice has been invited to present a DDR Interface technical paper. Lattice's dedicated DDR interface circuitry in the LatticeECP/EC FPGA family and new non-volatile, instant-on LatticeXP FPGA family will be highlighted. The technical discussion will feature Lattice's innovative solutions.

Attending the User2User conference is a valuable opportunity to mingle with engineers from all parts of the world and from all types of electronics companies. For more information or to register, visit the Mentor Graphics web site at www.mentor.com/user2user.

Lattice Offers Free On-Demand Web Seminars

Recent Lattice web seminars are available on-demand from the Lattice web site at www.latticesemi.com/events/net and are shown in the table

below. These one-hour web seminars are presented by Lattice technical staff and may include software demonstrations and question and answer ses-

sions. To view any of the web seminars, go to the webcasts section of the Lattice web site and select your topic of interest.

Seminar Title	Featured Product	Recording Date	Abstract
Reducing Dynamic Power Consumption through Voltage and Frequency Scaling	ispClock, ispPAC Power Manager	3/31/05	As the operating speeds of integrated circuits increase, the incremental power consumed by those devices (called "Dynamic Power Consumption") increasingly dominates the total power consumption of a board or system. To reduce overall power, system designers can minimize dynamic power by reducing the operating voltage or clock frequency during light processing periods. Learn how Lattice's programmable ispPAC Power Manager and ispClock devices can help you cut your power budget dramatically and how to design a board-level dynamic power management solution that is reliable, flexible, space efficient and easy.
Low-Cost, Flash-Based FPGAs Deliver "Instant-On" Performance	LatticeXP FPGAs	3/16/05	Low-cost FPGAs are increasingly used for low to medium density ASIC replacement. The new LatticeXP family brings non-volatility to low-cost FPGAs by combining flash and SRAM on a single chip, making it ideal for applications requiring high design security, minimized board-space, or "instant-on". Learn how to design with a single-chip, flash-based FPGA solution that is low cost, secure, space efficient, high performance and easy.
Low-Cost FPGA Design Optimization	LatticeECP/EC FPGAs, ispLEVER Design Software	2/2/05	Taking advantage of unique features in low-cost FPGAs allows you to integrate more functionality into smaller, less-expensive FPGAs that deliver higher performance. This NetSeminar demonstrates advanced design techniques and a timing closure methodology that leverages floorplanning, preferences, and critical path analysis that will get the most out of your low-cost FPGA designs using Lattice's ispLEVER design system. Learn design techniques to quickly create an FPGA solution that is more silicon efficient, higher performance, lower cost and faster to design.
LatticeECP/EC FPGA Design with ispLEVER	LatticeECP/EC FPGAs, ispLEVER Design Software	12/10/04	Lattice's ispLEVER digital tools suite supports all Lattice digital PLDs, including the new LatticeECP/EC FPGA device families, and provides all the features needed to develop a design from concept to programmed device. This demo provides an introduction to the LatticeECP/EC FPGA architecture, design flow and tools.
Embedding ASICs in a PLD	ORSPI4, ispLEVER Design Software	12/10/04	Lattice FPSCs pioneered the approach of putting ASIC embedded cores and FPGA gates on the same silicon die. Unlike ASICs with FPGA gates, FPSCs have a broad range of uses. The embedded cores hold industry standard IP, including bus interface, high-speed line interface and high-speed transceiver cores. When combined with programmable gates, FPSCs can be used in a variety of advanced system designs. This demo shows a sample implementation of SPI 4.2 and configuration of the ASIC block using ispLEVER development tools.

Lattice Listens

Q: Is there a way to optimize the performance of my counter without setting constraints on individual signals?

A: Because of the device independent nature of the optimizer in the ispLEVER tool suite, counters are often implemented in multiple levels of logic in the CPLD device architectures. The ispLEVER 5.0 tool suite has implemented a new constraint, COUNTER_OPT, solving this issue. This constraint is used to direct ispLEVER to produce the best counter performance. The constraint is assigned to output, bidirectional or node signals, directly in your VHDL or Verilog source code. The software will optimize these signals to provide counters with better performance. The syntax for assigning the COUNTER_OPT constraint is provided in the box at right.

Q: Can the LatticeXP on-chip Flash be programmed while the FPGA is running user configuration?

A: This is called background programming and it is fully supported by the LatticeXP. You may use either the dedicated JTAG pins or the sysCONFIG parallel port pins to read or write the on-chip Flash. Once you have loaded the new configuration into Flash, simply toggle the PROGRAM pin or cycle power to transfer the new code into the SRAM configuration memory. This is especially useful when you need to wait for the right moment to update the FPGA; perhaps you need to update all of your FPGAs at once, or you need to switch to a redundant card before doing the update. In any case, the transfer from on-chip Flash to SRAM takes a maximum of 1 millisecond and can be performed at a time of your choosing.

Q: Can I use the LatticeECP/EC PLL if my input signal is below the data sheet's frequency specifications?

Information Need	Resource
Technical Support	Tel: 1-800-LATTICE or (408) 826-6002 e-mail: techsupport@latticesemi.com
Software and Literature Download	www.latticesemi.com
European Literature Fulfillment	Tel: +44 (0)117 934 1600 FAX: +44 (0)117 934 1601 e-mail: euro.lit@latticesemi.com

```

VHDL
ATTRIBUTE COUNTER_OPT : string;
ATTRIBUTE COUNTER_OPT OF port_name: SIGNAL IS "Type";

Verilog Mentor Graphics
output [n:0] signal_name; //exemplar attribute signal_name COUNTER_OPT Type
reg [n:0] signal_name; //exemplar attribute signal_name COUNTER_OPT Type

Verilog Synplicity
output [n:0] signal_name /*synthesis COUNTER_OPT ="Type"*;
reg [n:0] signal_name /*synthesis COUNTER_OPT ="Type"*;

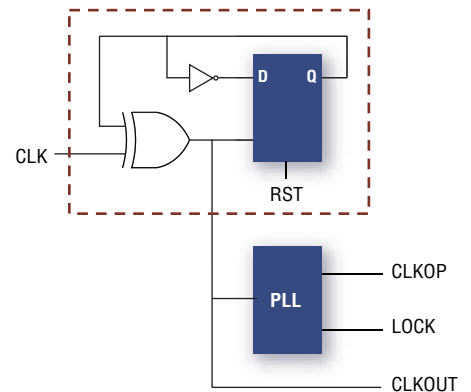
Legend
Type can be On or Off.
On - Directs the software to optimize specified signals for producing best counter performance.
Off - Disables this constraint. The software will perform normal optimization.
    
```

HDL Attribute Syntax

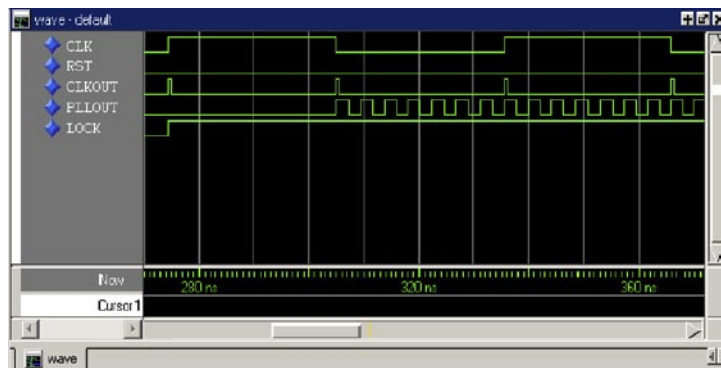
A: The LatticeECP/EC PLL must meet the data sheet specifications in order to ensure correct functionality. In order to use the PLL, you can increase the input frequency using logic. In the figure at right, the circuit outlined in red doubles the clock frequency. It does this by taking advantage of the routing delays of the device and the fact that the PLL does not require a clock input with a 50/50 duty cycle.

For this example, the design had an input frequency of 16MHz and the PLL output requirement is 229MHz. The logic is used to double the frequency to generate a 32MHz clock, which meets the PLL f_{in} specification.

The PLL can now be configured to produce a 229MHz clock with a 50/50 duty cycle. The results of a functional simulation of the circuit can be seen in the screen shot below.



Clock Doubling Design Example



Simulator Result for Clock Doubling Design

Lattice Literature

The following is a list of recently published documents, including descriptions and ordering numbers. On-line versions of these technical publications are available on the Lattice web site at www.latticesemi.com. Some of these documents are also available in print. To order print versions, call your local Lattice representative or Lattice's Literature Distribution Department at 1-888-477-7537 (outside the U.S. and Canada, call 503-268-8000) or order by FAX at 503-268-8556. In Europe, contact Lattice's European Literature Fulfillment Department by phone at +44 (0)117 934 1600, by FAX at +44 (0)117 934 1601 or by e-mail at euro.lit@latticesemi.com.

General Information

Title	Description	Web	Print	Order #
LatticeXP Family Handbook	Complete LatticeXP Family Data Sheet plus detailed technical notes on using the key features of this device family.	✓	—	—
LatticeXP Family Product Brief	Introduction to Lattice's new instant-on, single-chip FPGA with high security.	✓	✓	I0173
Lattice Product Line Card	Overview of featured product families: LatticeECP/EC, ispMACH 4000, ispXPLD 5000MX, ispClock and Power Manager.	✓	✓	I0172
XPIO™ 110XGS Transponder Board User's Guide	Guidelines for operation of the XPIO 110XGS Transponder Board.	✓	—	—
LatticeEC Standard Evaluation Board Revision B User's Guide	Guidelines for operation of the LatticeEC Standard Evaluation Board, Revision B.	✓	—	—
LatticeEC Advanced Evaluation Board Revision C User's Guide	Guidelines for operation of the LatticeEC Advanced Evaluation Board, Revision C.	✓	—	—

Data Sheets

Title	Description	Web	Print	Order #
LatticeXP Family Data Sheet	Full specifications for Lattice's new LatticeXP instant-on, single-chip FPGA family with high security.	✓	—	—
ispClock5600 Family Data Sheet	In-system programmable, zero-delay clock generator with universal fan-out buffer.	✓	—	—
ispPAC-POWR1208P1 Data Sheet	In-system programmable power supply sequencing controller and precision monitor.	✓	—	—
ORSPI4 Data Sheet	Full specifications for the ORSPI4: embedded SPI4.2 cores, 3.7Gbps SERDES, high-speed memory controller and FPGA.	✓	—	—

Technical Notes

Title	Description	Web	Print	Order #
LatticeECP/EC and LatticeXP sysIO Usage Guide	Describes the sysIO standards available for LatticeECP/EC and LatticeXP devices and how they can be implemented using ispLEVER design software.	✓	—	—
Memory Usage Guide for LatticeECP/EC and LatticeXP Devices	Guidelines for implementing the EBR and PFU based memories of LatticeECP/EC and LatticeXP devices using ispLEVER.	✓	—	—
LatticeECP/EC and LatticeXP DDR Usage Guide	How to utilize the capabilities of LatticeECP/EC and LatticeXP devices to implement both generic DDR and DDR memory interfaces.	✓	—	—
LatticeECP/EC and LatticeXP sysCLOCK PLL Design and Usage Guide	Describes the features and functionalities of the sysCLOCK PLL and its configuration in the ispLEVER design tool.	✓	—	—
Estimating Power Using the Power Calculator for LatticeECP/EC and LatticeXP Devices	How to use the ispLEVER Power Calculator tool to calculate power consumption in LatticeECP/EC and LatticeXP devices. Guidelines for reducing power consumption are also included.	✓	—	—
LatticeXP sysCONFIG Usage Guide	Covers all configuration options for LatticeXP devices.	✓	—	—
Lattice ispTRACY™ Usage Guide	Describes the functionality and usage of ispTRACY, a full-featured logic analysis tool for use in Lattice FPGA products.	✓	—	—

Lattice Literature, Cont.

Technical Notes

Title	Description	Web	Print	Order #
SPI Flash Programming and Hardware Interfacing Using ispVM System	Describes how a serial PROM can be emulated using a Lattice PLD and SPI Flash memory device to configure an FPGA in a standard master-serial mode.	✓	—	—
Using the LatticeEC Advanced Evaluation Board with the DDR Evaluation Bitstream	Describes the operation and use of a test bitstream for the DDR interface on the LatticeEC Advanced evaluation board.	✓	—	—
Evaluation Manual for LatticeEC Evaluation Boards	Detailed description of the PCI accessible resources inside the LatticeEC FPGA.	✓	—	—

Application Notes

Title	Description	Web	Print	Order #
ispPAC-CLK5620 Evaluation Board: ispPAC-CLK5620-EV1	How to use the ispPAC-CLK5620-EV1 evaluation board to configure and evaluate the ispClock5620 device.	✓	—	—

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