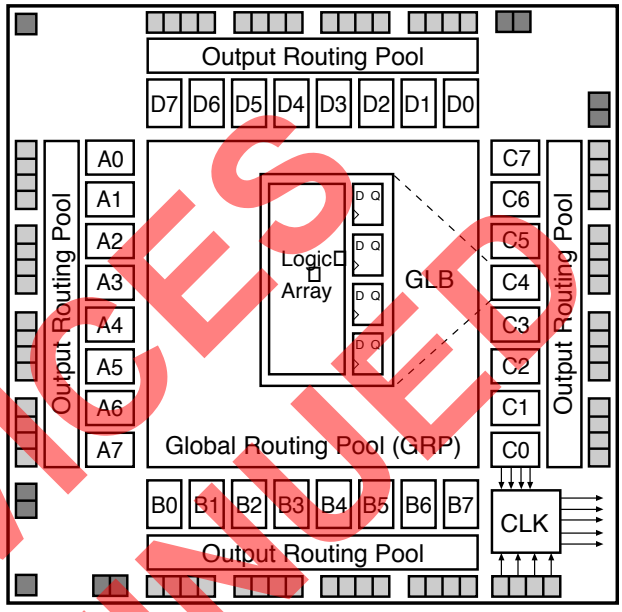
ispLSI® 1032

In-System Programmable High Density PLD

Features

- **HIGH-DENSITY PROGRAMMABLE LOGIC**
  - **— High Speed Global Interconnect**
  - **— 6000 PLD Gates**
  - **— 64 I/O Pins, Eight Dedicated Inputs**
  - **— 192 Registers**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Fast Random Logic**
  - **— Security Cell Prevents Unauthorized Copying**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— f_{max} = 90 MHz Maximum Operating Frequency**
  - **— f_{max} = 60 MHz for Industrial and Military/883 Devices**
  - **— t_{pd} = 12 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile E²CMOS Technology**
  - **— 100% Tested**
- **IN-SYSTEM PROGRAMMABLE**
  - **— In-System Programmable™ (ISP™) 5-Volt Only**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market, and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Prototyping**
- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **— Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **— Four Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**

Functional Block Diagram



Description

The ispLSI 1032 is a High-Density Programmable Logic Device containing 192 Registers, 64 Universal I/O pins, eight Dedicated Input pins, four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1032 features 5-Volt in-system programming and in-system diagnostic capabilities. It is the first device which offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems.

The basic unit of logic on the ispLSI 1032 device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. D7 (see figure 1). There are a total of 32 GLBs in the ispLSI 1032 device. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

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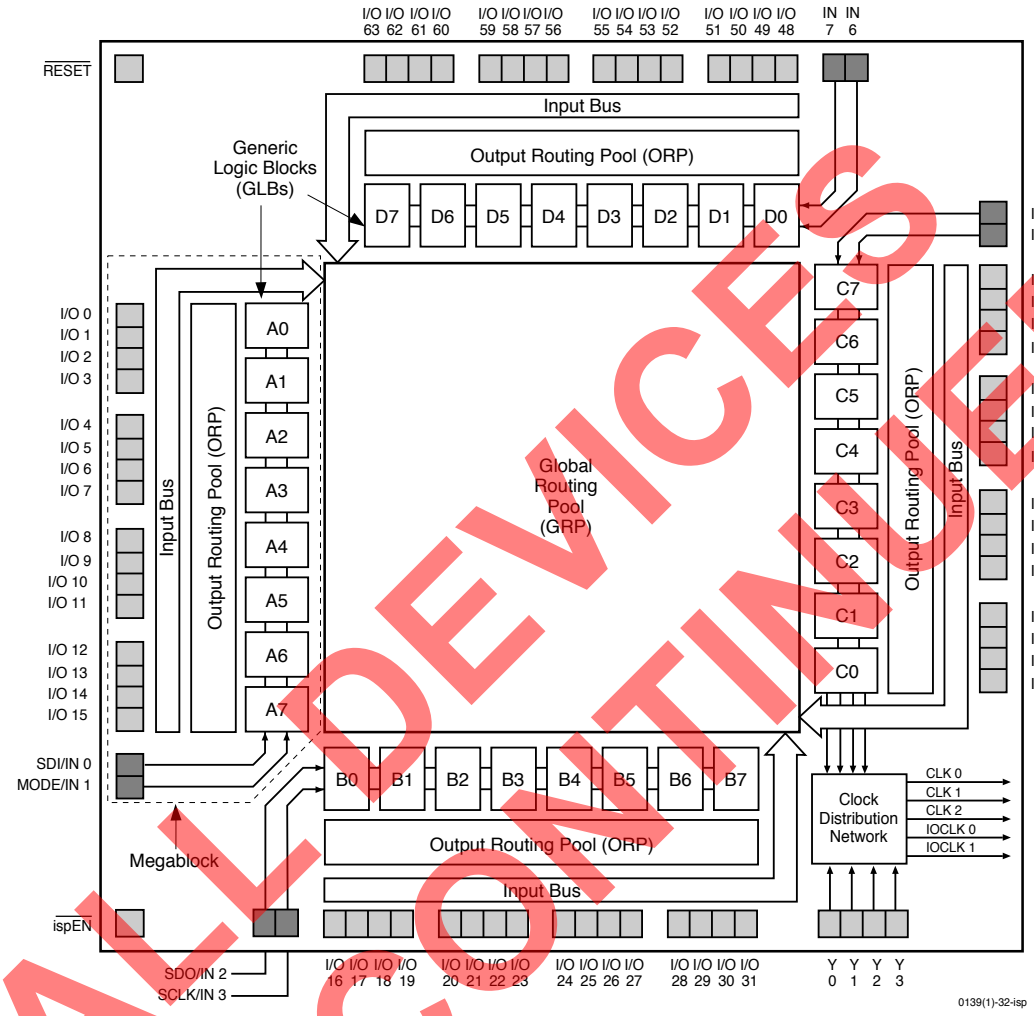
Functional Block Diagram

Figure 1. ispLSI 1032 Functional Block Diagram



The device also has 64 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. Additionally, all outputs are polarity selectable, active high or active low. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. The I/O cells within the Megablock also share a common Output Enable (OE) signal. The ispLSI 1032 device contains four of these Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 1032 device are selected using the Clock Distribution Network. Four dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (C0 on the ispLSI 1032 device). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to +70°C	4.75	5.25	V
		Industrial	T_A = -40°C to +85°C	4.5	5.5	
		Military/883	T_C = -55°C to +125°C	4.5	5.5	
V_{IL}	Input Low Voltage			0	0.8	V
V_{IH}	Input High Voltage			2.0	Vcc + 1	V

Table 2- 0005Aisp w/mil.eps

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER		MAXIMUM[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	Commercial/Industrial	8	pf	V_{CC}=5.0V, V_{IN}=2.0V
		Military	10	pf	V_{CC}=5.0V, V_{IN}=2.0V
C_2	I/O and Clock Capacitance		10	pf	V_{CC}=5.0V, $V_{I/O}$, V_Y=2.0V

1. Guaranteed but not 100% tested.

Table 2- 0006

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	—	Years
Erase/Reprogram Cycles	10000	—	Cycles

Table 2- 0008B

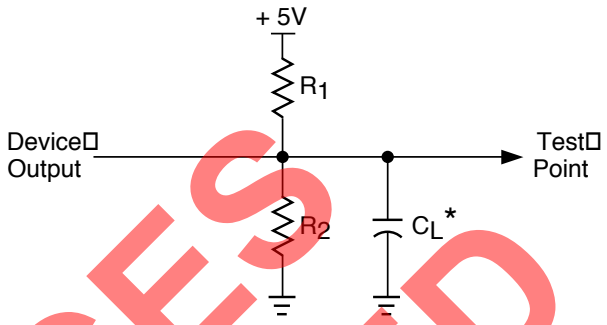
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See figure 2

3-state levels are measured 0.5V from steady-state active level.

Table 2- 0003

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

Output Load Conditions (see figure 2)

Test Condition		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH} - 0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} + 0.5V	470Ω	390Ω	5pF

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} =8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} =-4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}		–	–	10	µA
I_{IL-isp}	isp Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)		–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V		–	–	-200	mA
I_{CC}[2,4]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V	Commercial	–	130	190	mA
		f_{TOGGLE} = 1 MHz	Industrial/Military	–	135	220	mA

Table 2- 0007A-32-isp

1. One output at a time for a maximum duration of one second.
2. Measured using eight 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this datasheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum I_{CC}.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[5]	#[2]	DESCRIPTION[1]	-90		-80		-60		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	12	–	15	–	20	ns
t_{pd2}	A	2	Data Propagation Delay, Worst Case Path	–	17	–	20	–	25	ns
f_{max} (Int.)	A	3	Clock Frequency with Internal Feedback[3]	90.9	–	80	–	60	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	58.8	–	50	–	38	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle[4]	125	–	100	–	83	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	6	–	7	–	9	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP bypass	–	8	–	10	–	13	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	0	–	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	9	–	10	–	13	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	10	–	12	–	16	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	0	–	0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	15	–	17	–	22.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	10	–	10	–	13	–	ns
t_{en}	B	14	Input to Output Enable	–	15	–	18	–	24	ns
t_{dis}	C	15	Input to Output Disable	–	15	–	18	–	24	ns
t_{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	4	–	5	–	6	–	ns
t_{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	4	–	5	–	6	–	ns
t_{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2	–	2	–	2.5	–	ns
t_{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	6.5	–	6.5	–	8.5	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit counter using GRP feedback.
4. f_{max} (Toggle) may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions section.

Table 2-0030-32/90,80,60C

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-90		-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
t_{iobp}	20	I/O Register Bypass	–	1.6	–	2.0	–	2.7	ns
t_{iolat}	21	I/O Latch Delay	–	2.4	–	3.0	–	4.0	ns
t_{iosu}	22	I/O Register Setup Time before Clock	4.8	–	5.5	–	7.3	–	ns
t_{ioh}	23	I/O Register Hold Time after Clock	2.1	–	1.0	–	1.3	–	ns
t_{ioco}	24	I/O Register Clock to Out Delay	–	2.4	–	3.0	–	4.0	ns
t_{ior}	25	I/O Register Reset to Out Delay	–	2.8	–	2.5	–	3.3	ns
t_{din}	26	Dedicated Input Delay	–	3.2	–	4.0	–	5.3	ns
GRP									
t_{grp1}	27	GRP Delay, 1 GLB Load	–	1.2	–	1.5	–	2.0	ns
t_{grp4}	28	GRP Delay, 4 GLB Loads	–	1.6	–	2.0	–	2.7	ns
t_{grp8}	29	GRP Delay, 8 GLB Loads	–	2.4	–	3.0	–	4.0	ns
t_{grp12}	30	GRP Delay, 12 GLB Loads	–	3.0	–	3.8	–	5.0	ns
t_{grp16}	31	GRP Delay, 16 GLB Loads	–	3.6	–	4.5	–	6.0	ns
t_{grp32}	32	GRP Delay, 32 GLB Loads	–	6.4	–	8.0	–	10.6	ns
GLB									
t_{4ptbp}	33	4 Product Term Bypass Path Delay	–	5.2	–	6.5	–	8.6	ns
t_{1ptxor}	34	1 Product Term/XOR Path Delay	–	5.7	–	7.0	–	9.3	ns
$t_{20ptxor}$	35	20 Product Term/XOR Path Delay	–	7.0	–	8.0	–	10.6	ns
t_{xoradj}	36	XOR Adjacent Path Delay[3]	–	8.2	–	9.5	–	12.7	ns
t_{gbp}	37	GLB Register Bypass Delay	–	0.8	–	1.0	–	1.3	ns
t_{gsu}	38	GLB Register Setup Time before Clock	1.2	–	1.0	–	1.3	–	ns
t_{gh}	39	GLB Register Hold Time after Clock	3.6	–	4.5	–	6.0	–	ns
t_{gco}	40	GLB Register Clock to Output Delay	–	1.6	–	2.0	–	2.7	ns
t_{gr}	41	GLB Register Reset to Output Delay	–	2.0	–	2.5	–	3.3	ns
t_{ptre}	42	GLB Product Term Reset to Register Delay	–	8.0	–	10.0	–	13.3	ns
t_{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	7.8	–	9.0	–	12.0	ns
t_{ptck}	44	GLB Product Term Clock Delay	2.8	6.0	3.5	7.5	4.6	9.9	ns
ORP									
t_{orp}	45	ORP Delay	–	2.4	–	2.5	–	3.3	ns
t_{orpbp}	46	ORP Bypass Delay	–	0.4	–	0.5	–	0.7	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-90		-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Outputs									
t_{ob}	47	Output Buffer Delay	–	2.4	–	3.0	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	4.0	–	5.0	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	4.0	–	5.0	–	6.7	ns
Clocks									
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	3.6	3.6	4.5	4.5	6.0	6.0	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.8	4.4	3.5	5.5	4.6	7.3	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	0.8	4.0	1.0	5.0	1.3	6.6	ns
$t_{ioy2/3}$	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	2.8	4.4	3.5	5.5	4.6	7.3	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	0.8	4.0	1.0	5.0	1.3	6.6	ns
Global Reset									
t_{gr}	55	Global Reset to GLB and I/O Registers	–	8.2	–	9.0	–	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.