

## Introduction

When low-level or high-precision circuitry is being designed, a lot of care is usually given to the details of the circuit schematic and how the signal runs are routed. But the way the circuitry grounds are handled is as important as how the signal runs are handled. A small grounding error in just one location could potentially create long-term headaches once the board is powered up. Careful routing and decoupling of the power busses is also very important. This application note discusses a number of techniques for obtaining optimal performance from a printed circuit board layout involving analog parts. It is intended to help obtain the best performance possible from the ispPAC<sup>®</sup> family of programmable analog circuits. The differential instrumentation-amplifier inputs of the ispPAC10 and ispPAC20, and the excellent common-mode rejection that they provide, will be shown to assist in reducing many common layout problems. The on-chip gain-setting resistors will also prove to be advantageous. The guidelines in grounding, power distribution and layout contained in this application note will assist the reader in improving or alleviating many of these layout problems.

The topics below will be covered:

- A brief description of the ispPAC device family
- Grounding and ground planes
- Power planes and power decoupling
- Analog runs vs. digital runs
- The advantages of using differential circuitry
- Suggestions for reducing magnetically-induced interference.

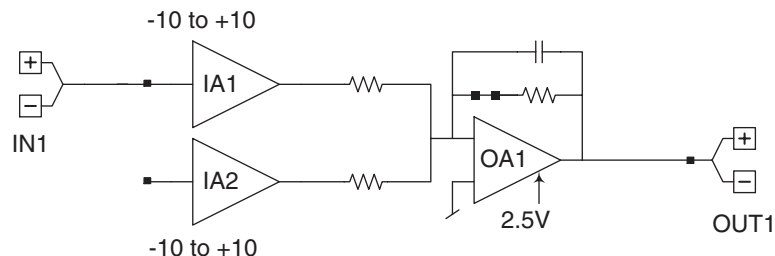
## ispPAC Background

The ispPAC family of Programmable Analog Circuits from Lattice Semiconductor represents a new level of integration and flexibility for general-purpose analog signal processing. It brings the concept of In-System Programmability (ISP<sup>™</sup>) to the world of analog circuits. Circuits can be designed and simulated using the Windows<sup>®</sup>-based PAC-Designer<sup>®</sup> software. Once the simulated performance is shown to be as desired, the design can be downloaded to the ispPAC device. The device's in-circuit performance, and even its functionality, can thus be changed without lifting a soldering iron or changing any external parts.

The basic ispPAC gain block is shown in Figure 1. The integrated programmable analog macrocells in this figure are collectively known as a PACblock<sup>™</sup>. The ispPAC10 consists of four identical PACblocks, and the ispPAC20 includes two of these blocks as well as an 8-bit DAC and two comparators. Each PACblock is composed of a differential-output summing amplifier (OA) and two differential-input instrumentation amplifiers (IA) with variable gains of  $\pm 1$  to  $\pm 10$  in integer steps. The OA's feedback path contains a fixed resistor, which can be switched in or out, as well as a programmable capacitor array that allows for more than 120 poles when the ispPAC device is used as an active filter. Each PACblock has the ability to sum two differential signals with independently selectable gain and inversion settings and to act as a gain element (with the feedback switch closed) or as an integrator (with the feedback switch open).

The gain settings, feedback, capacitor values and interconnects between PACblocks are configurable through nonvolatile E<sup>2</sup>CMOS<sup>®</sup> cells internal to the ispPAC devices. The device configuration is set by software and

**Figure 1. A Single PACblock**



# Analog Layout and Grounding Techniques

downloaded in less than 250 milliseconds via a JTAG-compatible ispDOWNLOAD<sup>®</sup> cable. Refer to the ispPAC10 Data Sheet for more details on the specifics of the device.

The following describes techniques for improving analog layouts in general and explains the advantages of incorporating the ispPAC devices.

## Grounding and Ground Planes

### System “Star” Grounds

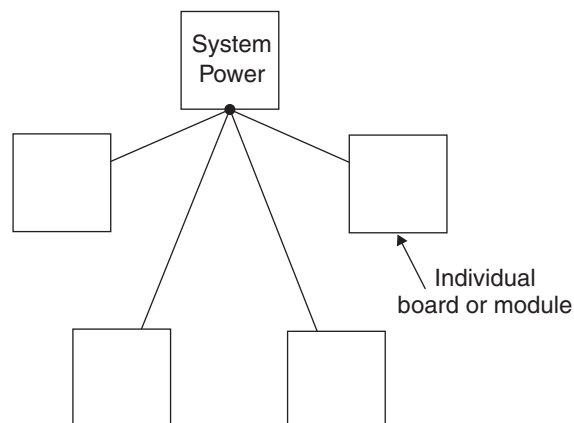
In equipment design, there are a number of different classes or types of grounds. Two of them are the “system ground,” which is the ground that is shared by all the boards or modules in the system, and the “board ground,” which is the ground as it exists on a given circuit board. The system ground should be connected to the various boards in a “star” fashion, with each board or module having its own ground or common return lead back to a central location that is the common reference point of the system power supply (Figure 2). These connections should be made with large-diameter buss wire or very wide PCB runs to reduce resistive and inductive losses. This “star” connection (so named because it looks like a star) prevents currents drawn by one board or module from modulating the current drawn by another board. In many systems, the grounding of the various boards can become somewhat of a problem, since cables running between these boards cause ground conflicts with the “star” ground system. The problems become even more acute if a number of individual systems or instruments are mounted in a rack, which is itself conductive and will have its own ground scheme. Cables running between these instruments will also cause a system ground conflict due to multiple, parallel ground connections (including the all-important grounds through the mains power cords). While this paragraph serves as an overview of system-level grounding issues, the scope of this application note is directed more towards individual circuits and boards than towards a large system.

### Board “Local” Grounds

#### *Current Return Paths vs. Ground Planes*

The common-return currents or grounding of individual components on a circuit board is the ground that is of most interest to circuit designers. It is well known that a circuit board run carrying a signal generates a return current back to the source. This return current follows the path of least resistance and would prefer to flow in a run directly underneath the signal run, for circuits on a printed circuit board. For this reason, single-layer layouts are

Figure 2. “Star” Grounding



almost always nearly impossible to make clean. Two-layer boards require great care in laying out return paths as well as signal paths in order to make them clean. Since wider runs usually have lower impedance, they may be more appropriate for a return path (the inductance of narrow runs can impede current flow, especially at higher frequencies). The optimum return path for a signal is a plane, where an entire layer is “poured” with copper and serves as a very low-impedance return path. There are many advantages to using a ground plane instead of ground return traces, including better performance due to the lower ground impedance and the better EMI/RFI performance of such boards. But there are some rules which should be followed in order to extract the best performance from such boards.

#### *Layout and Ground Plane Rules*

A primary layout consideration is that the analog and digital ground planes should not overlap. To that end, they should both be on the same PC board layer, separated by at least 0.1 inch. The analog circuitry and the digital circuitry should likewise be separated, over their respective ground planes. Placing analog and digital circuitry at opposite ends of a circuit board is an excellent way to begin. Do not surround the analog region with digital circuits or surround the digital region with analog circuits; it will be impossible to route clean runs through the digital area to the analog circuitry or to keep the analog and digital runs separated. Power supply circuits should be in a centralized area near the edge of the board so they can feed the digital and analog sections equally well. A location near the edge of the board allows any return currents generated in this area to return directly to the main supply without passing through the rest of the board. The analog and digital ground planes should be connected together at only one point; either at the local

# Analog Layout and Grounding Techniques

on-board power supply circuits or, preferably, where they leave the board to return to the main power supply. Some A/D converter manufacturers prefer that the analog and digital grounds be connected together at the ADCs. In this case, make jumpers available to try both choices to determine which has better overall performance. If there is more than one A/D converter on the board, make jumpers available at each A/D, as well as at the point where the grounds leave the board, to allow for testing to determine which connection gives the best results.

## **Keep Analog and Digital Areas Completely Separate and Non-Overlapping**

When placing and routing the analog and digital circuitry over their respective ground planes, there should be no overlap between any of the analog areas (ground or power planes or circuitry) and any of the digital areas to minimize induced noise. Do not cross signal runs between the planes unless absolutely necessary, for the same reason. Return currents will not be able to jump the gap between the planes and will have to travel long distances to be reunited with the signal currents, usually picking up unwanted noise along the way. The best designs have analog power planes and an analog ground plane that exactly overlap, and digital power planes and a digital ground plane that exactly overlap, with the best performance usually being obtained when the ground plane is immediately underneath the power supply plane. The large overlap area of these power and ground planes, combined with their close spacing, makes a distributed capacitance, which will be more effective at suppressing high frequency noise than individual, lumped capacitors. This helps to keep the analog power planes and ground plane quiet.

## **Ground Pins on Connectors**

In order to maintain a low-impedance ground connection back to the system power supply, it is usually necessary to use more than one connector pin for ground. In fact, one of the places where many of the board's runs have to be run in parallel is at the connectors, and additional grounds will provide additional shielding as well as giving a lower-impedance supply ground connection. There have been recommendations that 25%-40% of a connector's pins be dedicated to ground, with the ground pins being spread out among the connector pins. Depending on the metal-plating of the connector pins and the insertion force of the connector, a few pins may be adequate when the board is new but may corrode over time, increasing the ground resistance and thereby worsening the performance of the board. Having at least 25% of the pins dedicated to ground is a reasonable recommendation.

## **Power Planes and Power Distribution**

### **Which Supply to Use and Supply Decoupling**

Power leads coming onto the circuit board should be decoupled to ground at the point where they enter the board. That way, all return currents from the decoupling components return directly to the power supply without passing through the ground planes of the board. While inductive decoupling components (lossy ferrites or inductors with parallel damping resistors) or resistive decoupling components can be effective, the best designs route  $\pm 18V$  to  $\pm 24V$  to each board and use small regulators, along with decoupling, to derive  $\pm 12V$  to  $\pm 15V$  for the board or individual devices. The same scheme should be used for best performance from the single-supply ispPAC devices: route +8V to +15V to the individual boards, with separate +5V regulators and decoupling on each board. One of the advantages of using ispPAC devices in designs is the fact that they only require a single +5V supply, without the need to decouple positive and negative supplies. A/D converters and D/A converters, in particular, need regulators and decoupling close to them to reduce the possibility of noise coupling from the rest of the circuitry, if maximum performance is desired. Most A/D converters also have a low-current digital section that needs to be connected to the quiet analog supply and ground, usually through some decoupling. Having pins marked "DGND" on an A/D converter usually means that they are the IC's digital ground, not that they should be connected to the system's digital ground. Most A/Ds also specify that even their high-current digital sections should be connected to an analog supply and ground, using higher-power decoupling, to obtain best performance. In general, noisy digital supplies and ground need to be kept away from high-performance A/D converters, except in the area where the digital outputs are developed. In order to have analog power and grounds on their supplies but digital ground plane underneath their digital outputs, most A/D converters should straddle the split between the grounds in some fashion (see one example in Figure 7). Usually the manufacturer of the A/D converter will offer guidance in device layout to realize maximum performance from their part.

### **IC Decoupling**

All analog circuitry needs decoupling on its power leads to shunt both high-frequency and low-frequency noise to ground. It is generally recommended that designers use either a 0.1  $\mu F$  or 0.01  $\mu F$  capacitor to decouple the power pins of each analog IC to ground. At various distances, place larger value capacitors, usually 10  $\mu F$  to 47  $\mu F$ , in parallel with 0.1  $\mu F$  or 0.01  $\mu F$  units. In particular, high performance ICs need to have each supply decoupled to

# Analog Layout and Grounding Techniques

ground. The smaller value capacitor should be placed as close to the IC as possible, on the same layer as the IC (to avoid the inductance of feed-through vias). The leads on these capacitors must be kept very short. The best technique is to have the power feed from the power plane through a via to the capacitor and IC pins, with the capacitor between the via and the IC. The ground connection is particularly important, and should be made with three to four vias connecting to the capacitor and thus to the IC pins. The inductances of these vias are then effectively in parallel. See Figure 3 for examples of this technique. Surface-mount capacitors are best because their connection pads have almost no lead inductance. In addition, surface-mount electrolytic capacitors can be used for the 10  $\mu\text{F}$  to 47  $\mu\text{F}$  units. Both aluminum and tantalum capacitors are available in these values, with tantalum having the lower ESR but also being more prone to power supply transients or reversal. OS-CON dielectric capacitors have the lowest ESRs but are also more expensive than aluminum or tantalum.

## Assigning PCB Layers

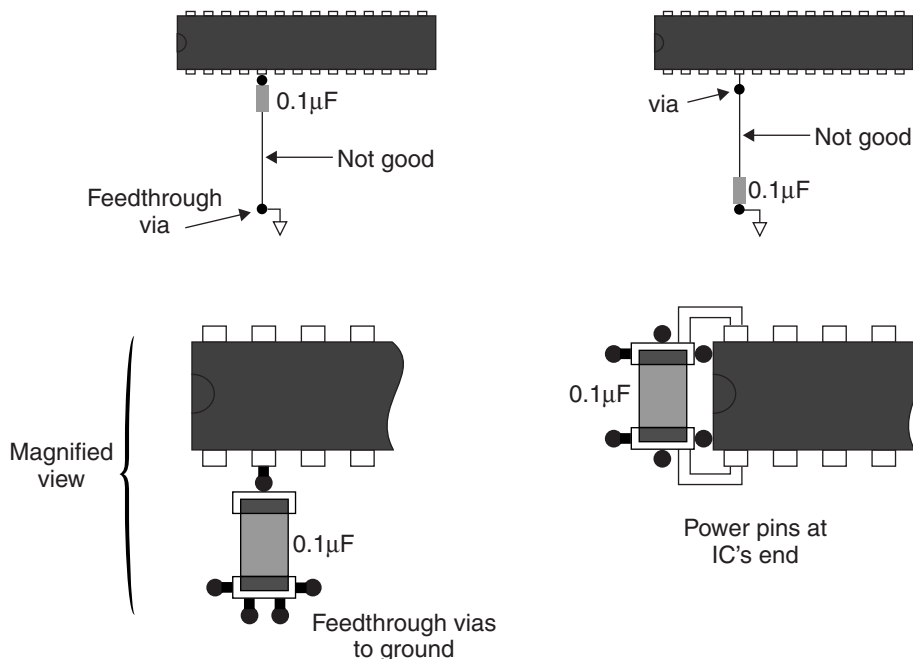
A typical four-layer board should be laid out with the signal runs on the outer layers and the power and ground planes on the inner layers. Many PC boards are thinner between layers 2 and 3, so that power and ground planes on these layers will have higher distributed capacitance ( $C = \epsilon A/d$ ). Placing the signal runs on the outer layers

makes the board easier to work on during prototyping. Having the planes underneath the signal layers also helps to provide a lower-impedance surface region and provides additional shielding between the signal layers. Printed circuit boards with more layers should still keep the power and ground planes in the center of the board, adjacent to each other.

## Analog Runs and Digital Runs

It is almost always necessary to keep digital runs away from analog runs. The fast rise times of digital signals cause them to more easily couple into adjacent runs. With 3.3V or 5V logic, a 0.2V spike from an adjacent digital signal won't cause a problem, but that same 0.2V spike will wreak havoc in an analog circuit. The longer the distance that two runs are run in parallel, or the closer they are to each other, the more coupling will occur. Such runs can even couple through adjacent layers of a circuit board. It is best to try to keep runs on adjacent layers at roughly right angles to each other. This technique usually facilitates easier layout and reduces crosstalk. Be aware that sometimes radiation from adjacent circuit boards can couple into some analog circuits and may require shielding or more careful layout. It has been shown that using copper fill between areas of signal runs reduces crosstalk and radiation if the copper fill is grounded (never leave it ungrounded). Also note that some digital runs (especially clocks) can couple into the  $V_{\text{REF}}$  pins of

Figure 3. Bypassing and Decoupling of IC Power Pins



# Analog Layout and Grounding Techniques

some A/D converters, causing “strange lumps” in the spectrum of the noise floor of the A/D. Keep all connections to  $V_{REF}$  pins very short and isolated from digital runs. In some designs, it may be necessary to run parallel sets of runs for long distances. Be sure to design the configuration of these conductors carefully to reduce the effects of crosstalk between the conductors. In some cases, it may be necessary to intersperse some ground runs between other runs to act as shielding. Also remember to terminate and, in some cases, back-terminate digital runs to control overshoot and undershoot if the runs have significant length (more than a few centimeters).

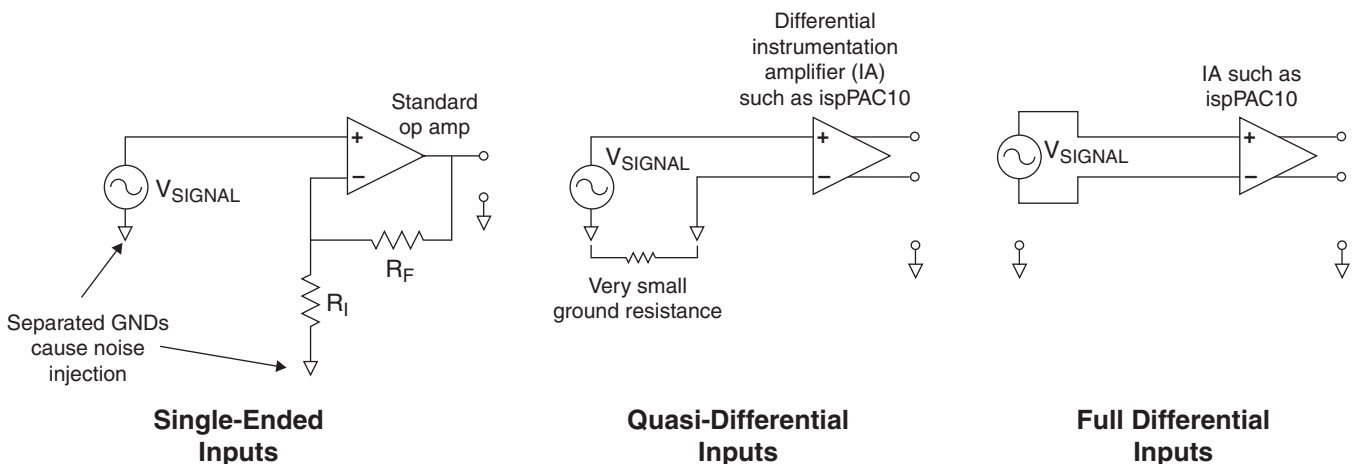
## Differential Circuitry

Because ispPAC technology utilizes differential techniques, it is worth explaining some of the advantages and key layout aspects of differential circuitry and comparing them to similar single-ended op amp circuitry. Differential circuitry is superior to single-ended circuitry for a number of reasons. The common-mode rejection of differential inputs lets balanced circuitry reject common-mode interference, including ground noise, that would be amplified by single-ended circuits. Also, a differential circuit’s balanced properties usually reduce non-linearities and improve distortion. In addition, some ICs with differential outputs (such as today’s single-supply DACs) have inherent common-mode output noise that is cancelled if the DAC is followed by a differential-input amplifier or filter. Because a differential signal’s two conductors carry a balanced signal, reduced EMI generation and reduced susceptibility to magnetic pickup (due to reduced loop area) are additional benefits of differential circuitry. Even

“quasi-differential” circuitry, with its ground taken adjacent to a single-ended source but shipped to a differential load as if it were the second half of a differential signal, is superior to single-ended circuitry. This is because the small common-mode interfering currents between the source and load are still reduced by the differential input. See Figure 4 for examples of these concepts. Note that the single-ended connection in Figure 4 is shown as a standard op amp, although it could also apply to single-ended connections into ispPAC gain blocks if the ground-referenced signals were instead referred to 2.5 volts. The details of the 2.5 volt input reference have been left out of Figures 4, 5 and 6 to improve the clarity of those drawings.

Figure 5, with more detail, shows how ground noise and other single-ended noise sources are amplified in single-ended circuitry but are rejected as common-mode signals in differential circuitry. In the figure,  $V_{NOISE}$  represents “ground loop” noise injected into the input signal path due to  $I_{GND}$  flowing through the distributed resistance  $R_{GND}$ . There are at least three flaws in the single-ended circuit: (1) both  $V_{SIGNAL}$  and  $V_{NOISE}$  are amplified by the circuit. (2) The gain is actually  $1 + R_F/(R_I + R_{GND})$  in the single-ended circuit, causing a slight error. (3) The voltage across  $R_{GND}$  due to  $I_{GND}$  (“ground-loop” current) gets added in series with the input (which is why it gets amplified, causing additional noise at the output). By contrast, in the differential-input amplifier circuit, (1)  $V_{NOISE}$  is a common-mode signal, which is reduced by the common-mode rejection of the differential input. (2) In the ispPAC devices, the gain is set by resistors internal to the amplifier and is unaffected by  $R_{GND}$ . (3) The voltage across  $R_{GND}$  is now also a common-mode

Figure 4. Improvement in Noise Pickup with Differential Connections



# Analog Layout and Grounding Techniques

Figure 5. Common-Mode Rejection and Ground Resistance

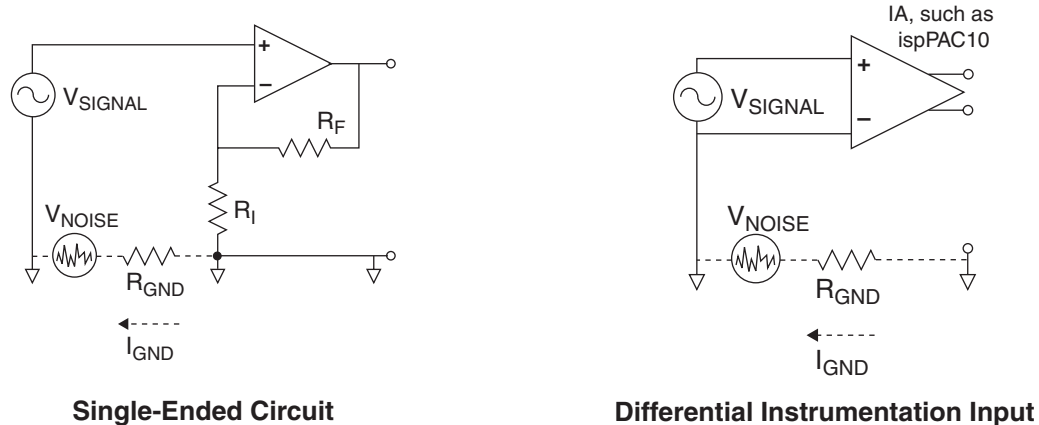
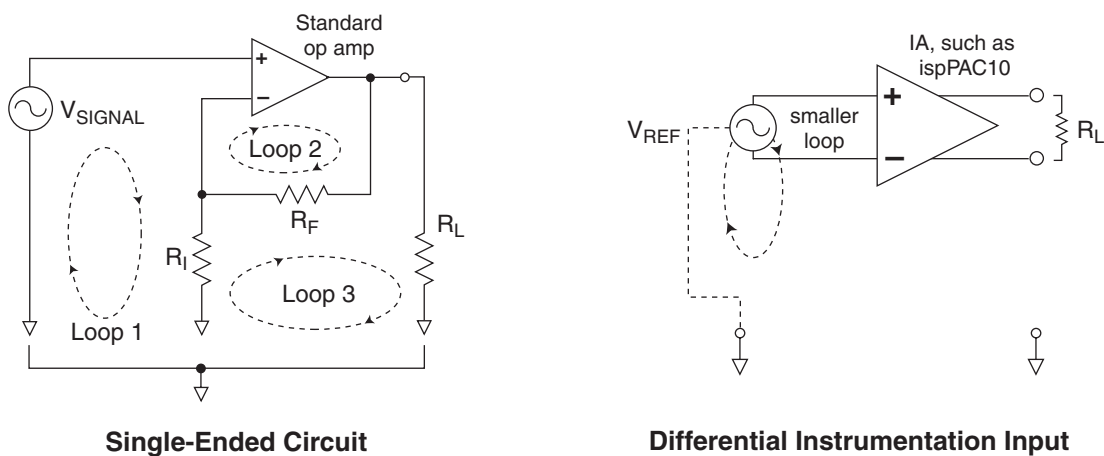


Figure 6. Magnetically-Coupled Interference



signal that is reduced by the differential input. These advantages are some of the main reasons for the increased use of differential circuitry, especially in mixed-signal systems. The ispPAC devices take advantage of these principles by using a fully-differential architecture with instrumentation amplifier inputs.

## Magnetically-Induced Interference

Differential devices also afford some protection against magnetically-induced interference, which can come from nearby power transformers or coils in switching power supply circuits or even from magnetically-deflected CRTs. Frequently, the most confusing task in magnetically-coupled interference is identifying the circuit loops which are picking it up. These loops, while usually unintentional, are due to the physical layout of the circuit's

components. A typical op amp circuit can have three inductive loops if it is not carefully laid out (Figure 6). The most significant of the loops is the one that involves the input circuitry (Loop 1 in Figure 6), because the noise it picks up is amplified by the circuitry. Noise picked up by Loop 2 and Loop 3 only appears in the output with a gain of one. Since magnetic pickup varies with the loop area and the number of flux lines crossing the loop, the most useful techniques for reducing magnetic interference (short of breaking the loop) are minimizing the loop area or orienting the loop parallel to the magnetic field. In the differential circuit with the ispPAC gain cells, having the feedback and input resistors on-chip reduces the areas of Loop 2 and Loop 3 to near zero. As mentioned above, differential input devices usually have reduced input loop area, since differential components are usually very close to each other. Reducing the loop area of the rest of

# Analog Layout and Grounding Techniques

the input circuitry is still an important tool in reducing magnetically-induced interference. If this does not reduce the magnetic interference enough, and if the circuitry cannot have its physical orientation changed, it may become necessary to use magnetic shielding (steel or mu-metal) between the magnetic source and the board.

## Summary

In this application note, techniques to improve circuit board layout have been discussed, including grounding and ground planes, power planes and decoupling, and circuit layout techniques. Figure 7 summarizes many of the points developed here. The differential nature and instrumentation-amplifier inputs of the ispPAC devices have been shown to make a significant improvement in solving grounding and layout problems. The techniques mentioned in this application note should prove beneficial in laying out a board without grounding or power-related problems, or in solving such problems in fewer board turns.

## Technical Support Assistance

Toll Free Hotline: 1-800-LATTICE (Domestic)  
International: 1-408-826-6002  
E-mail: [ispPACs@latticesemi.com](mailto:ispPACs@latticesemi.com)  
Internet: <http://www.latticesemi.com>

Figure 7. A Layout Using Many of the Points Given in this Application Note

