ISP Overview

February 2002

Introduction

In-System Programmable (ISP™) products from Lattice Semiconductor provide the ability to reconfigure the logic and functionality of a device, board or complete electronic system before, during and after its manufacture and shipment to the end user.

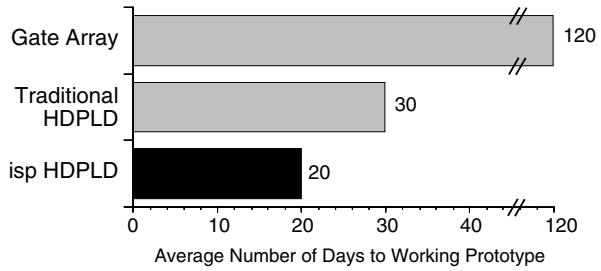
Lattice pioneered the ISP technology. ISP devices eliminate limitations associated with traditional programmable devices and deliver benefits in board- and system-level design, manufacturing and programming. With ISP devices, hardware is as flexible and easy to modify as software and design upgrades are simple. Because ISP devices can be treated like any other device on the printed circuit board (PCB), no special manufacturing flow is required to program ISP devices; standard logic level programming signals are easily generated by a PC, Sun Workstation, ATE (Automatic Test Equipment) or system embedded microprocessor. In pioneering ISP products, Lattice has developed an integrated solution of silicon, software and applications know-how that make ISP products practical.

Why ISP Products?

Time-To-Market

The drive for shorter time-to-market has fueled explosive growth in the use of PLDs. Based on user responses, ISP PLDs provide an additional 33% reduction in time-to-market over traditional programmable devices and more than 83% reduction in time-to-market compared to application-specific integrated circuit (ASIC) implementations (Figure 1).

Figure 1. In-System Programmability: Time-to-Market Advantage



Source: Independent survey of over 300 PLD users

Another indicator of ISP product momentum is the percentage of designers who say that the capability of in-system programmability influences their selection of a high density PLD. In 1990, only 8% of system designers said that ISP influenced their high density PLD decision. Today, it is a requirement.

Design Benefits

ISP products allow design, test and manufacturing engineers to reconfigure system features while the devices remain soldered on the circuit board. This capability revolutionizes design prototyping, board-level debug, system manufacturing, and system upgrades.

The Superior Prototyping Solution

During most system design cycles, major board building blocks such as the microprocessor and RAM are selected first, well before system logic decisions are made. When using Lattice ISP devices, the designer can fully populate a prototype board with the major building blocks, interconnecting all functions with programmable devices. Design changes can be made in minutes using Lattice software design tools. A download cable from a PC or workstation to the prototype board downloads the new design information into the device(s). This ability to modify system func-

tionality without changing components or PCB layout is only the first of many advantages afforded by Lattice ISP products.

Internal Test

Once the ISP PLD logic has been stabilized, the designer may use the ISP devices to debug other portions of the board. For example, a circuit board frequently operates in a system where it is supplied with stimulus from other boards. The designer can use in-system programmability to debug system-level operation more quickly by reconfiguring the ISP devices to force or redirect signals (e.g. clocks or control signals) into various portions of the board design. This ability to thoroughly check board designs saves precious time during system-level debug and translates directly into a competitive time-to-market advantage.

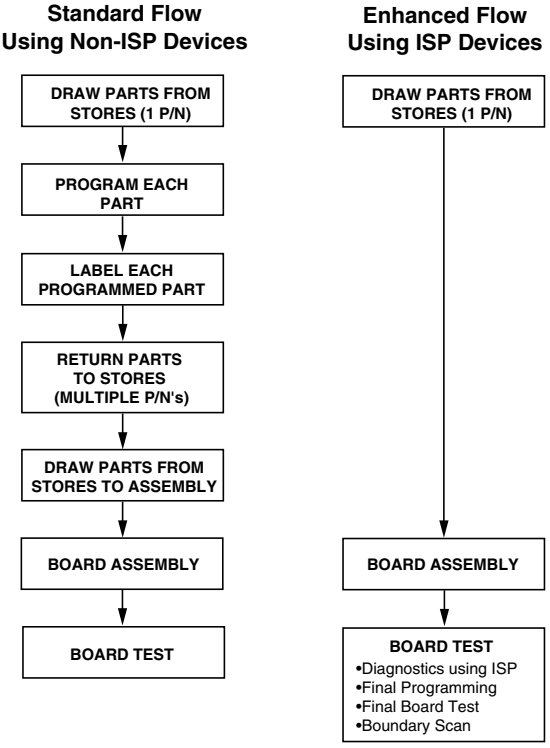
Board Reconfiguration and Field Upgrades

ISP devices provide an ideal way to reconfigure boards and/or upgrade product features in the field. With conventional technology, a system installed at a customer site is very expensive and difficult to upgrade to the latest hardware revision, to fix hardware bugs or to enable hardware options. With ISP devices, however, if a subsequent reconfiguration, upgrade or repair is required, a simple upgrade disk can be used, either in the field or the factory, to reconfigure the design (e.g. to modify memory refresh or control logic or analog filter coefficients). Updates via modem, serial link or a special ISP programming interface are possible depending on the system environment or requirements.

Manufacturing Benefits

ISP products are not only revolutionizing the world of design but also dramatically transforming the world of manufacturing. ISP devices support multi-function hardware designs that reduce system part counts and costs. ISP products also support reconfigurability for test which enhances board-level testability and, ultimately, system reliability. Finally, ISP devices allow the “standard manufacturing flow” to be simplified (Figure 2), reducing costs and enhancing system quality.

Figure 2. ISP Manufacturing Flow vs. Standard Flow



Multi-Function Hardware

ISP products can be used to exploit the concept of multi-function hardware: a single hardware design able to implement a variety of system-level functions via in-system programming. Multi-function hardware allows manufacturers to reduce the number of unique board designs used in a system, further simplifying the manufacturing flow.

Multi-function hardware dramatically lowers system-level costs by reducing the component count on the boards as well as reducing the number of different boards required to implement various system-level options.

A dual-processor board, intended to interface with several bus interface standards, illustrates these benefits. The traditional solution calls for dedicated logic for each of the bus interface standards, requiring either a unique board dedicated for each standard or a single board with additional logic. ISP devices allow the design of a single generic bus interface, which can be configured in-system to interface with each of the bus standards, saving components, and cost.

Reconfigurability for Test

ISP products facilitate board-level testing and increase system fault coverage without sacrificing board resources or real estate. A diagnostic test pattern can be temporarily programmed into the ISP devices to exhaustively exercise board-level functions. Additionally, with ispGDX® and ispGDS® devices, programmable signal routing can be exploited in the test environment to perform enhanced board-level test. For example, certain ISP devices may be configured by the tester to force test sequences into other portions of the board logic. The tester then monitors the response of this action and determines if the board passes or fails. This ability to detect board-level failures early in the manufacturing cycle reduces overall system cost. Once these detailed diagnostics are complete, the ISP devices can be reprogrammed to their normal logic configurations for final functional testing.

Boundary Scan

Complementing the ISP approach to board-level testing, IEEE Standard 1149.1 Boundary Scan technology (available with the MACH® 4 and 5, ispMACH™ 4A, 4000B/C, 5000VG, ispLSI® 1000EA, 2000VE/VL, 5000V, 8000/V and ispGDX/V families) enhances overall system quality. As component densities on the system boards increase, along with greater chip density and I/O, the ability to access and test critical nodes is impaired. With Boundary Scan Test, a serial interface through the test access port (TAP) simplifies field diagnostics and testing while costs are reduced. And because the same Boundary Scan serial path and control pins are used for implementing ISP programming, overall manufacturing costs are reduced as well.

Simplified Manufacturing Flow/ No Bent Leads

At present, there are no automatic handlers capable of handling the programming of high lead-count, high-density Quad Flat Pack devices. As a result, all non-ISP high lead-count devices must be programmed by hand using a standard programmer.

It is a difficult task to insert a high lead-count, small lead-pitch device into a programming socket adapter, program, label (or mark) and reinventory the device without bending the delicate package leads. These bent leads can result in poor coplanarity and bad solder connections, increasing the amount of board and system-level troubleshooting required.

ISP devices go directly from the receiving dock to the manufacturing floor for placement on the PCB, entirely eliminating stand-alone programming and mark operations and avoiding bent leads associated with misalignment of the device in the programmer socket. Unprogrammed ISP devices can be loaded into auto-insertion equipment and then placed directly onto the PCB without sockets or regard for the specific logic configurations. Individual device configurations can be downloaded from Automatic Test Equipment, PC, or workstation platforms at final board test. Programming of high density PLDs containing thousands of gates takes only seconds.

System Upgrades and Repair

Lasting benefits from the use of ISP devices can be realized even after systems are shipped. In-system reprogramming can reduce field maintenance costs through enhanced field diagnostic capability, less costly product feature

upgrades, and simpler maintenance procedures. Training, documentation and ongoing support can also be simplified by using the ISP approach to build in maintainability.

Applications

Lattice's breadth of ISP device options, together with their leading-edge performance and features, have resulted in the design-in of ISP devices into a wide range of electronic systems. These applications include:

- Multimedia Video Editing
- Electronic Test Equipment
- Network Routers and Bridges
- Cellular Telephone Base Stations
- Telephone Switching Systems
- Hardware Accelerators
- Memory Subsystems
- Multi-standard Video Frame Grabber
- Data Acquisition
- Image Processing

Why have designers embraced Lattice ISP products? For many, the manufacturing cost benefits, faster design and prototyping and the ability to reliably program high pin-count devices have been the most obvious benefits. ISP devices also provide the ability to reconfigure systems immediately prior to and after shipment, opening up additional possibilities.

For example, a very common but practical application comes from a company manufacturing traffic signal controllers. These controllers support priority "green lights" for emergency vehicles and buses through strobe light sensors that detect coded strobe sequences from the vehicles. The authorized sequences vary from city to city. ISP products allow the sequence detector to be reprogrammed easily at the time the signal controller is shipped to a particular area or after it is installed. The alternative of custom-coded, traditional PLDs would result in significant additional effort and expense to customize the hardware of each system.

ISP Products from Lattice

Lattice features the industry's largest in-system programmable product offering. Three methods of programming are used: ISP, ispJTAG™ and IEEE 1532. Table 1 lists the Lattice in-system programmable devices and the programming format supported. Proprietary Lattice ISP devices use the Lattice ISP state machine. See the document *Using Proprietary Lattice ISP Devices* for more information on programming these devices. ispJTAG devices use the IEEE 1149.1 Boundary Scan Test Access Port and TAP state machine for programming. More information on ispJTAG and IEEE 1532 programming can be found in *In-System Programming Usage Guidelines for ispJTAG Devices*. The abovementioned documents, device data sheets and additional information on all Lattice devices can be found on the Lattice Data Book CD-ROM or the Lattice web site at www.latticesemi.com.

Multiple Programming Platforms

Lattice ISP devices can be easily programmed in a wide variety of ways:

PC

Engineers save time and money by designing and programming logic on a single platform. Designers can enter and simulate designs using popular third-party CAE tools, automatically place-and-route the logic using Lattice design tools, and then download the programming files to ISP devices. With ISP products, programming is easy. The ispVM™ System software, in conjunction with the ispDOWNLOAD® cable, connects the PC parallel port to the ISP devices to give quick, easy and inexpensive programming of one or more ISP devices.

ATE

Lattice ISP devices can also be programmed at final board test on an ATE, completely eliminating the need for a third-party device programmer for production. This streamlines the manufacturing flow and allows programmable

devices for the first time to be treated like any other components on the board. To make the task easy, the ispVM System software includes ispATE®, a tester programming utility that is also incorporated into ISP Daisy Chain Download and LatticePRO download software to generate programming test vectors for many popular ATE vendors. ispATE can also generate test vectors for ispSVF™ which supports Serial Vector Format (SVF) for ispJTAG devices.

Embedded Processor

System Designers who want to be able to modify product features or upgrade their system hardware after the product has shipped to their customers will be interested in in-system programming using their product's own embedded processor. The product's embedded processor can be used to directly supply the ISP programming signals through a simple 4- or 5-bit port using ispVM™ EMBEDDED source code. Logic fuse maps and code can be stored in EPROM or other available system memory element. If the system has a modem or network link, remote download of new configurations from a central point is even possible. As a result, systems no longer become obsolete as soon as they leave the factory, but can adapt and change to meet customers' growing needs for years to come.

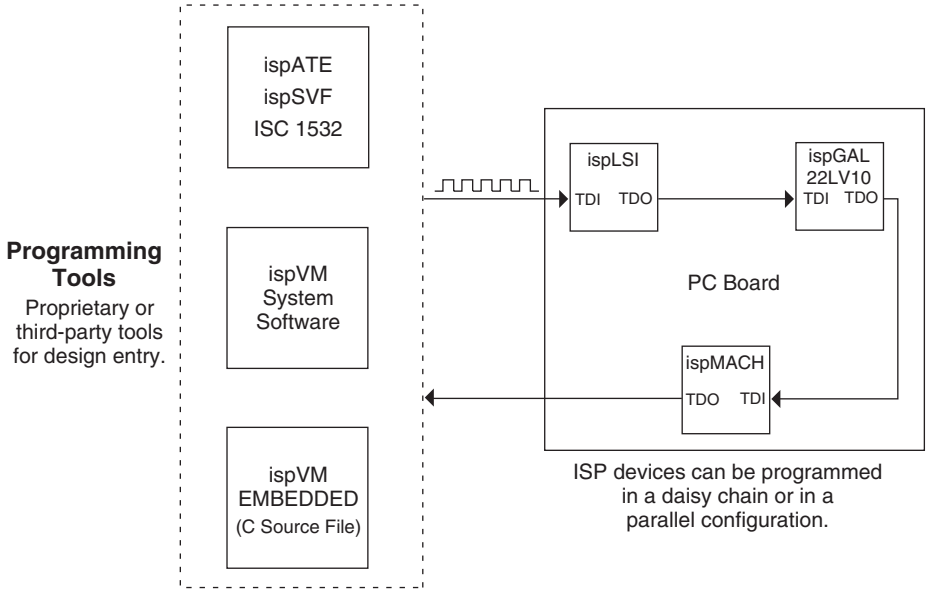
Third-Party Programmers

Finally, ISP devices can be programmed by a number of popular third-party programmers. In some cases, a user owns a third-party device programmer and is interested in the long-term benefits of ISP PLDs (like future field upgradability) but isn't ready to make the change yet. These users can still program ISP devices like any other PLD on their device programmer. If they need to change the device programming pattern, ISP products make the process a lot easier: no device desoldering, no board swapping, no wasted effort.

Table 1. Lattice In-System Programmable Products

Product	Programming Method	BSCAN Registers
ispLSI 1000EA Family	JTAG/IEEE 1532	Yes
ispLSI 2000E/V Family	JTAG/IEEE 1532	No
ispLSI 2000VE/VL Family	JTAG/IEEE 1532	Yes
ispLSI 5000/V/E Family	JTAG/IEEE 1532	Yes
ispLSI 8000 Family	ISP/JTAG	Yes
ispLSI 8000V Family	JTAG/IEEE 1532	Yes
ispMACH 4A Family	JTAG/IEEE 1532	Yes
ispMACH 4000	JTAG/IEEE 1532	Yes
ispMACH 5000VG	JTAG/IEEE 1532	Yes
ispGDX Family	ISP/JTAG	Yes
ispGDXV/A Family	JTAG/IEEE 1532	Yes
ispGDS Family	ISP	No
ispGAL22V10	ISP	No
ispGAL22LV10	JTAG/IEEE 1532	No
MACH 4 Family	JTAG	Yes
MACH 5 Family	JTAG	Yes
ispPAC Family	JTAG	No

Figure 3. ISP PLD Design and Implementation Flow



Once a JEDEC file is created, Lattice's programming tools allow programming of ISP devices on a PC, Sun Workstation, embedded processor or with ATE.

Lattice Design Tools

Lattice offers many powerful and flexible design tools for efficient device design. Refer to the Lattice CD-ROM or web site (www.latticesemi.com) for detailed information on Lattice design tools.

Technical Support Assistance

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