Applying the ispPAC30 to Data Acquisition Systems with Analog-to-Digital Converters

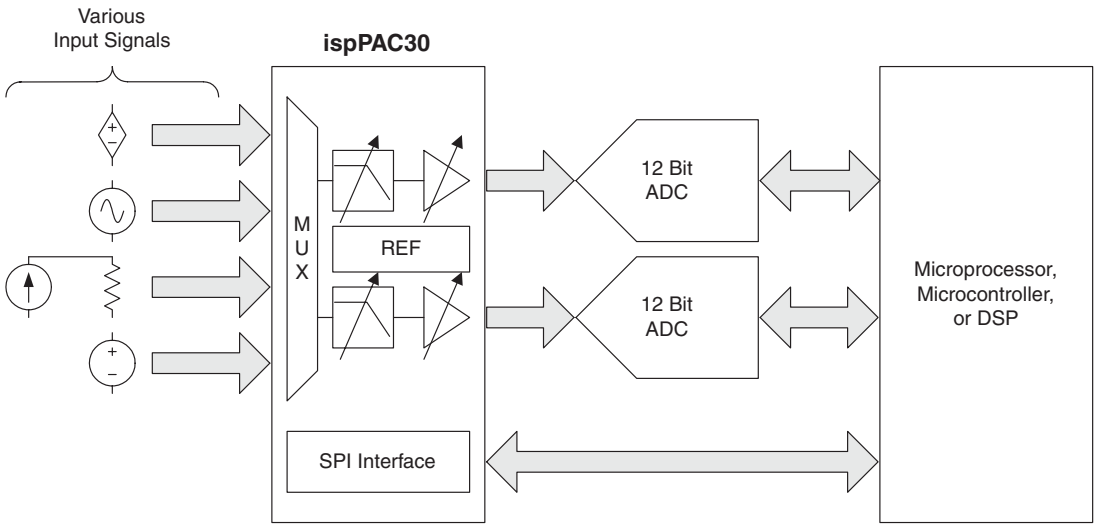
July 2002 Application Note AN6035

1. Introduction

Lattice Semiconductor's ispPAC®30 is a versatile analog IC targeted at applications in signal conditioning, control loops, and Analog-to-Digital Converter (ADC) front ends. This application note focuses on how the ispPAC30 can be used as a flexible solution for interfacing signals to ADCs. Figure 1 highlights the core components (input routing pool, shown as a MUX, adjustable references, adjustable filters, and adjustable gains) that make the ispPAC30 an attractive and logical choice for interfacing a variety of signal types. The ispPAC30 allows system designers to re-configure the analog front end to the ADC, using either E^{2}CMOS® or SRAM based configurations. This provides maximum system-level performance, adapts to changing input-signal situations, and can be easily customized for servicing multiple applications with the same board or core design.

Lattice Semiconductor also provides easy-to-use, Windows® based PAC-Designer® software that greatly simplifies analog design and simulation activities and reduces time to market.

Figure 1. Data Acquisition System Using an ispPAC30



2. Background

Lattice Semiconductor's Programmable Analog Circuits (PAC) technology eases the challenges when designing analog circuits requiring adjustable gain, offset, and filtering. The ispPAC30 is especially suited for interfacing analog signals with different parameters to an ADC, because of its complement of features. The list of features includes, but is not limited to, the following: input routing of four differential inputs, two MUXes, two channels of programmable gain with programmable low-pass filters, two voltage references, and single ended output amplifiers. All of the analog features of the ispPAC30 are controlled directly from the internal SRAM register. This SRAM register is loaded at power-up from a user defined configuration stored in on-chip E^{2}CMOS that was created using PAC-Designer (version 1.3 or later).

While the E^{2}CMOS register has a limited number of erase/write cycles (about 10,000), the SRAM register has no such limitations and can be modified using either the SPI (Serial Peripheral Interface) or the JTAG-TAP interfaces. The ispPAC30's In-System Programmability (ISP™) provides re-configuration in real-time, which can be utilized during prototype and development to adjust for different signal ranges or frequency response. The fully re-configurable solution offered by the ispPAC30 can also be incorporated into embedded systems, where a DSP or microcontroller can take full advantage of SPI to change (on the fly) configurations of gain, internal routing, MDAC set-

tings and output amplifier (OA) configuration. Application note AN6027, *Using SPI to Configure and Control the ispPAC30,* provides the required information to do all this and much more.

3. Interfacing to the ADC

This section describes the challenges of interfacing signals to the ADC and highlights the solutions that are well suited for the ispPAC30. Due to the wide variety of data acquisition systems, there are as many different challenges for interfacing as there are signals and sensors to measure. All data acquisition systems need the capability to convert one form of signal or another, so it can be analyzed, stored or transferred to another process. In a data acquisition system, the analog signals, either AC or DC measurements representing power, temperature, voltage, current, pressure or volume etc., are converted from the analog domain to a digital value. It is at the front-end of the ADC where we see the value of the ispPAC30. When considering interface options for the ADC, the following list of attributes should be considered and we will examine each one in the sections that follow; adaptability, frequency response, offset adjustment, gain control, multiplexed inputs, input and output impedance, and power consumption.

3.1. Adaptability

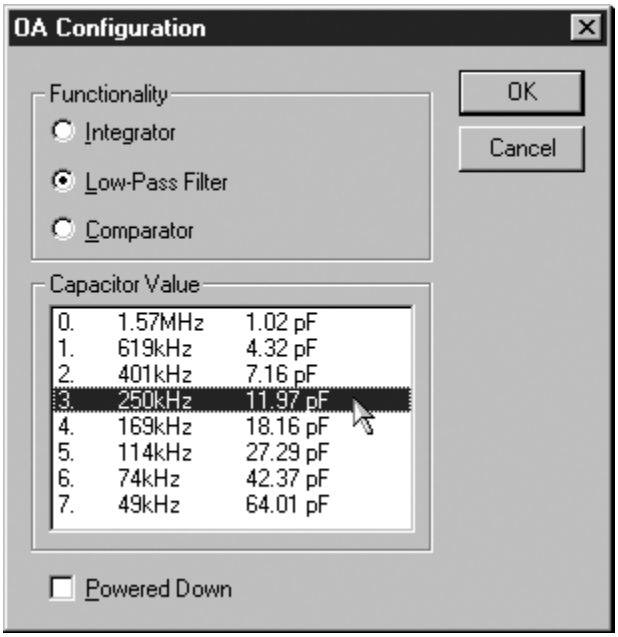
Lattice Semiconductor's In-System Programmability (ISP™) enables one to adapt circuits without having to modify the PCB. Adaptability offers benefits to all phases of the design cycle and beyond. Since the circuit behavior of the ispPAC30 can be adjusted electronically, the need to cut traces and add jumpers is reduced, or in many cases eliminated. Likewise, the need to make multiple passive component changes to fine-tune a circuit is greatly reduced. After the prototype has been verified, little or no changes may be needed in order to transfer the design into production. The system or board can be verified and modified during pre-production, or production test, and even after being shipped as a final product. After final development stages the adaptability is still of great value for being able to make a change if an outside signal or hardware change is made that affects the ADC interface.

3.2. Frequency Response

As with any ADC interface, the front end filtering is an important parameter to consider as the signal transitions to the converter. In order to prevent aliasing of the signal from the sampling of the ADC, an anti-alias filter (low-pass) is used to filter out or attenuate higher frequencies that may distort the sampled signal. The essential function of the anti-alias filter is to lower the bandwidth of the input signal below that of the sampling rate by at least a factor of two, in accordance with the Nyquist Theorem. In most applications the bandwidth is also driven by the need to filter out unwanted signals and to reduce the noise contribution. When the ispPAC30 is configured as a low-pass filter, the corner frequency is set using the on-chip capacitors in the feedback circuit of the output amplifier (OA).

Figure 2 illustrates how the cut-off or corner frequency can be selected from a PAC-Designer menu of eight specific frequencies ranging from 49kHz to 1.5MHz. The selections presented on the menu are designed to provide evenly spaced corner frequencies on a dB scale. This provides maximum coverage over the bandwidth of the ispPAC30. From the array of on-chip capacitors, the ispPAC30 places different values of capacitors into the feedback circuit, but does not use "switched-capacitor" technology to implement the low-pass filter. In a "switched-capacitor" filter, the input signal is modulated by the switching frequency. Thus, several disadvantages of this type of filter include the need for an external clock source, contamination of the input signal by harmonics of the switching frequency, and a post filter to reduce the switching feed-through. In contrast, the ispPAC30 uses a true time-continuous filter for greatest performance and lowest contribution of errors into the signal. Furthermore, the ispPAC30 capacitor array is trimmed at the factory to provide corner frequency accuracy of 3%. This allows a greater range in sampling than with 10% to 20% discrete components since one can sample all the way down to 2x the corner frequency instead of to within 10% or 20% of it.

Figure 2. Setting Low-Pass Filter Corner Frequency Using PAC-Designer Software



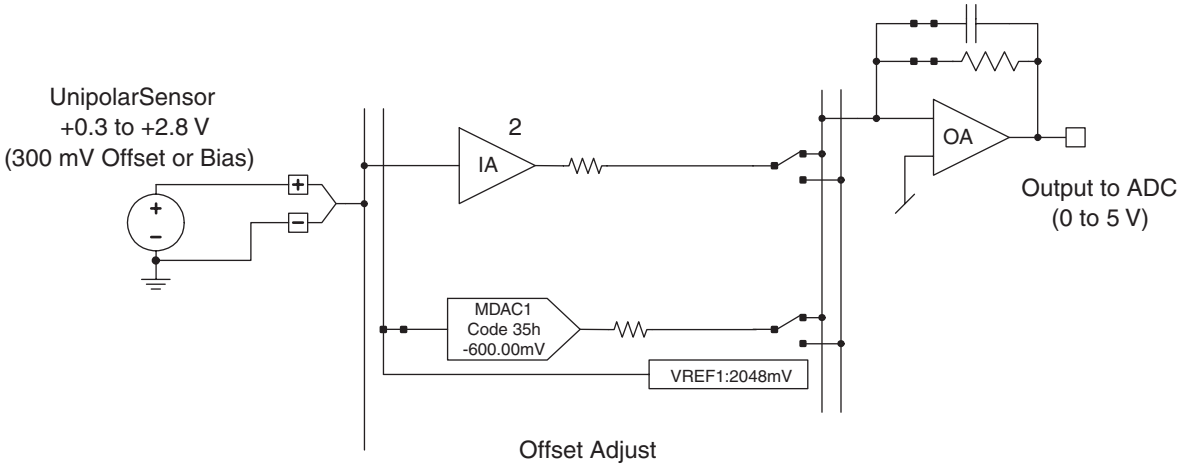
3.3. Offset

Along with the AC properties of the sampled signal at the ADC, it is important to consider the DC offset caused by the signal source and/or associated circuitry. The offset can be caused by component mismatch, sensor environments, sensor bias, or other circuit conditions such as time or temperature. Regardless of the source of the DC offset, in many cases, it does not represent the signal of interest and if its amplitude is significant, it must be removed from the signal prior to amplification, conversion and analysis. This can easily be done using the programmable precision references and amplifiers within the ispPAC30. Two independent voltage references reside within the ispPAC30 and each one has seven selectable values (see Figure 5) ranging from 64mV to 2.5V. The output of each precision voltage reference can be connected to the inputs of the respective MDAC (multiplying digital to analog converter) or IA (instrumentation amplifiers), or both. By combining the MDAC and IA outputs at the input to the output amplifier (OA), the programmable voltage references can be used to add or subtract a wide range of offsets. The combination of IA gain values, MDAC settings, and voltage references results in over 1,000 different values that can be used to adjust offset.

Figure 3 shows an example of how the reference and the MDAC can be used to remove a 300mV DC offset from the input signal. The 2048mV reference is inverted and adjusted by MDAC1 to -600mV to counter the 300mV sensor offset that is gained by a factor of two. Note that the maximum input signal (2.8V) amplified by the IA gain of two would result in a voltage of 5.6V. To understand how this is possible inside a 5V device please see Appendix A, where a part of the ispPAC30 internal circuitry is discussed. The flexibility of the ispPAC30 provides the designer many choices for adjusting system offset, not only at design time, but also at test or system run time. Just like all the other features of the ispPAC30, the voltage references, IA gains, and MDAC settings, can be set from E^2CMOS (nonvolatile storage) or adjusted from the SPI interface in real-time.

In contrast to system-level offsets discussed above, the ispPAC30 has a separate on-chip self-calibration circuit. This circuit performs an automatic offset trim (called Auto-Cal) during power-up. Auto-Cal can also be initiated after power-up by activating the CAL-pin, or sending the SPI calibration instruction. This feature allows for the best offset performance of the ispPAC30 regardless of configuration, temperature, and other factors. For additional information regarding this feature, please refer to the ispPAC30 data sheet.

Figure 3. Using VREF and the MDAC to Cancel Sensor Offset



3.4. References

Most ADCs accept an external precision reference to set the full-scale range of the input signal. The ispPAC30's precision reference can be selected and then modified (fine-tuned) using the MDAC (see Figure 4 through Figure 6). This is similar to what was done in the offset section. As shown in Figure 4, VREF1 is set to 1024mV and MDAC1 fine tunes the voltage to 1.0V. The OA serves as a buffer and provides typical output drive of +/- 30mA. The ispPAC30 also has a fixed 2.5V reference that is available at the $VREF_{OUT}$ pin with less drive than the OA (please consult the ispPAC30 data sheet for design limits). Figure 5 shows the 1024 mV reference voltage selected from the list of seven possible values. Note that in Figure 6, the PAC-Designer dialog box presents both the decimal and hex code for the MDAC as well as the resulting voltage, that is based upon the input voltage reference.

Figure 4. VREF and MDAC Provide a Programmable Precision Voltage Reference

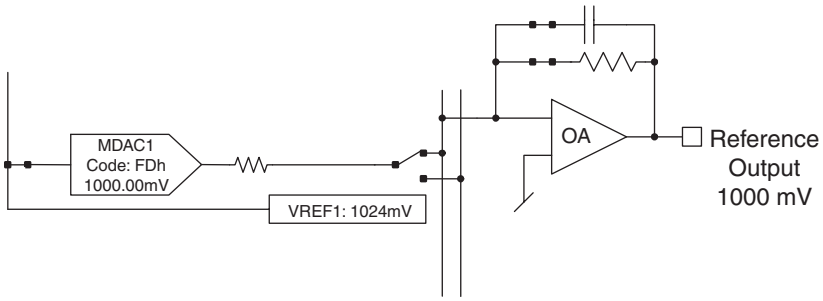


Figure 5. Setting the VREF Voltage

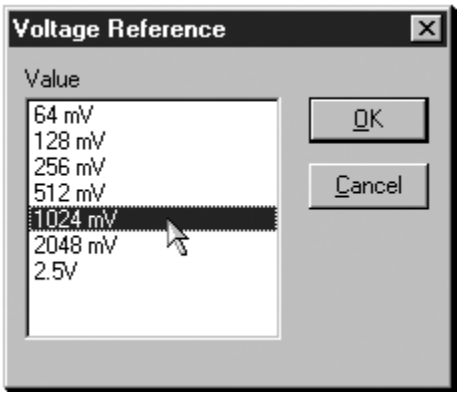
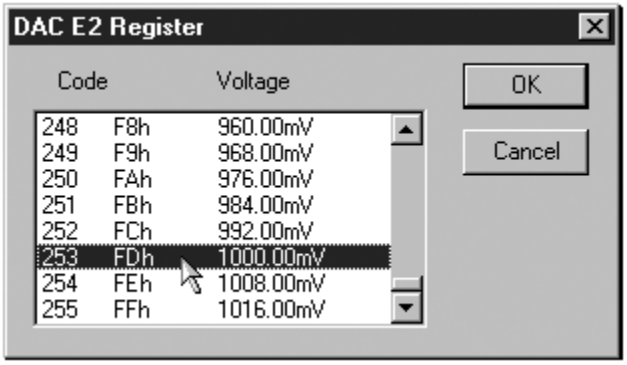


Figure 6. Setting the MDAC Code and Voltage



3.5. Gain Control

The ability to adjust gain to accommodate dynamic system requirements is an essential attribute of a well-designed analog front end. Programmable gain enables a system to scale the input signals, based on changes in the environment, to the full range of the ADC. Gain control with the ispPAC30 can be carried out in several different modes. The gain of each instrumentation amplifier (IA) is programmable in integer steps from 1 to 10 with positive or negative polarity. In addition to the IAs, there are two multiplying digital to analog converters (MDAC), whose inputs can be routed from any of the four inputs. The gain of the MDAC can be represented by the following equation where "Code" represents an eight-bit value (0 to 255). Thus there are 256 gain steps from -1.0 to +1.0, including zero.

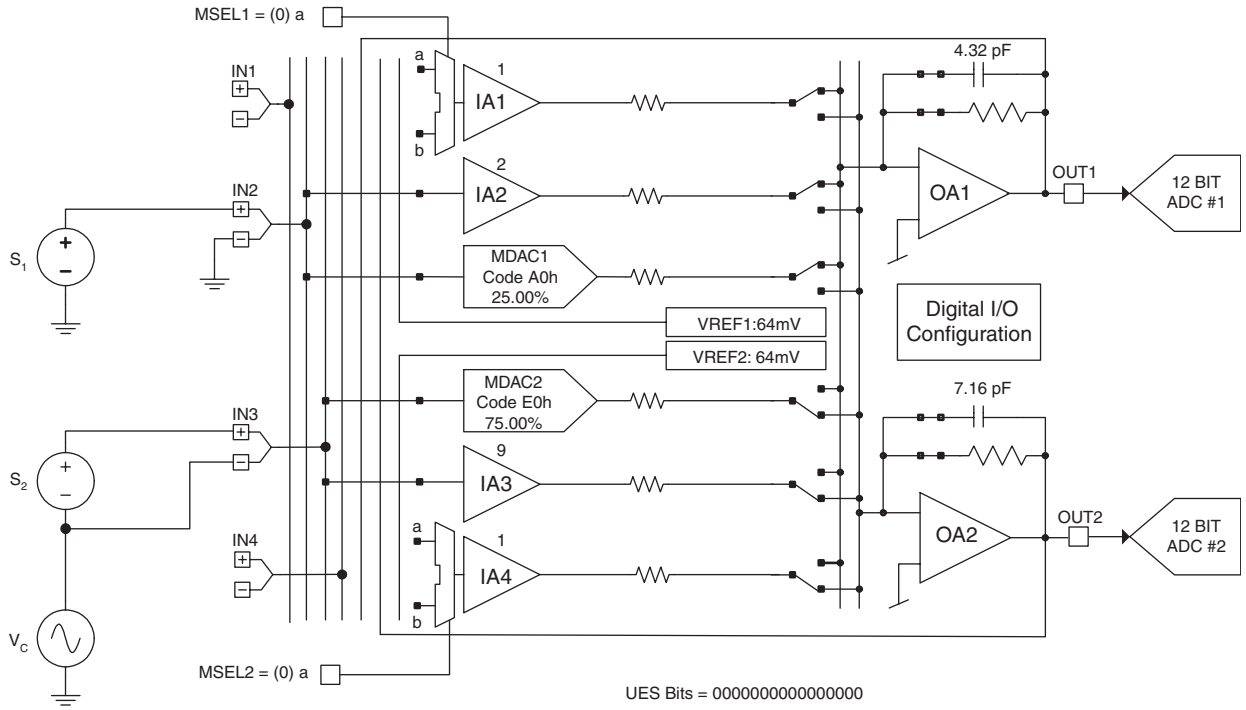
$$Gain_{MDAC} = \left[\frac{Code}{128} - 1\right] \quad (1)$$

Using these modules (IA, MDAC) individually or combined, a large range of gain can be implemented with very fine resolution.

To illustrate the feature of programmable gain, Figure 7 shows the full PAC-Designer schematic of the ispPAC30 with symbolic signal sources connected to the inputs, and ADCs connected to the outputs. A single-ended signal source (S_1) is connected to the (+) pin of input #2. The input routing pool passes the signal from input #2 to both IA2 and MDAC1. The summing node routing pool combines the IA and MDAC outputs into the input of OA1. IA2 is set to a gain of +2 and MDAC1 is set to a gain of +0.25 (Code = 160). Their collective gains result in an overall gain of +2.25. In Figure 8 we see how the PAC-Designer dialog box reflects the input signal type to the MDAC (compare to Figure 6) and provides a list of available gains (shown as percentages).

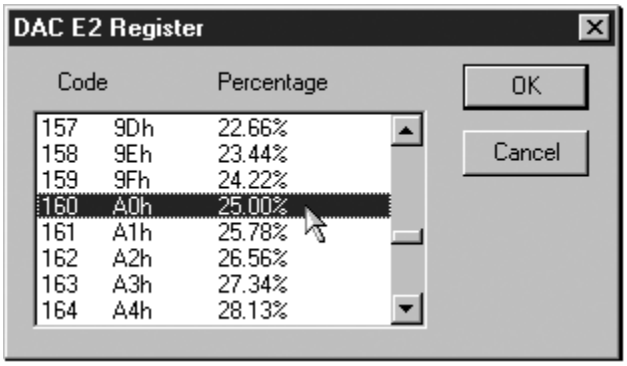
The second signal source (S_2) in Figure 7 is connected differentially to input #3, and then routed to both IA3 and MDAC2. These respective gains are set to +9 and +0.75 (Code = 224) and are summed by OA2 to provide a gain of +9.75. Note that the differential input does not amplify the common voltage source (V_C), that may result from ground loops or ground shifts. Figure 7 also illustrates the low-pass filter function of the OAs (4.32pF on OA1 and 7.16pF on OA2, corresponding to 619kHz and 401kHz respectively).

Figure 7. Two Channels with Fractional Gains



In either of the two examples above, we could add a second or third IA for additional gain. Thus the range and resolution of programmable gains obtained using the ispPAC30 are both wide and very fine.

Figure 8. Setting the MDAC Code and Percentage



3.6 Higher Gains

To expand upon the basic gain setting features described above, we will now look at how the ispPAC30 can address situations that require voltage gains of 40, 100, or more. A gain of 42 can be obtained by setting gain of all four of the IAs to 10 and both MDACs to a gain of 1 and summing into one OA. If the input is a very small DC signal, the output of an OA can be routed directly (using the input routing pool) to the input of one or more IAs, to cascade or multiply gains. For example, a 10 mV input signal is routed to IAs 1 and 2, both set for a gain of 10 and summed into OA1, which produces a 200 mV signal. This is routed back around to IAs 3 and 4, both set for a gain of 10 and summed into OA2. This results in a final output of 4.0V and a gain of 400. Because the OAs are single ended amplifiers and the ispPAC30 is a single supply part, a slightly different approach is required for AC signals. Each OA will need to have a DC bias added to their summing nodes so they can represent both the positive and negative portions of the input signal. Without this bias, only the positive portions of the input signal would be amplified, and the negative portions would reside below ground. A bias value of 2.5V is implemented in Figure 9 (using VREFs

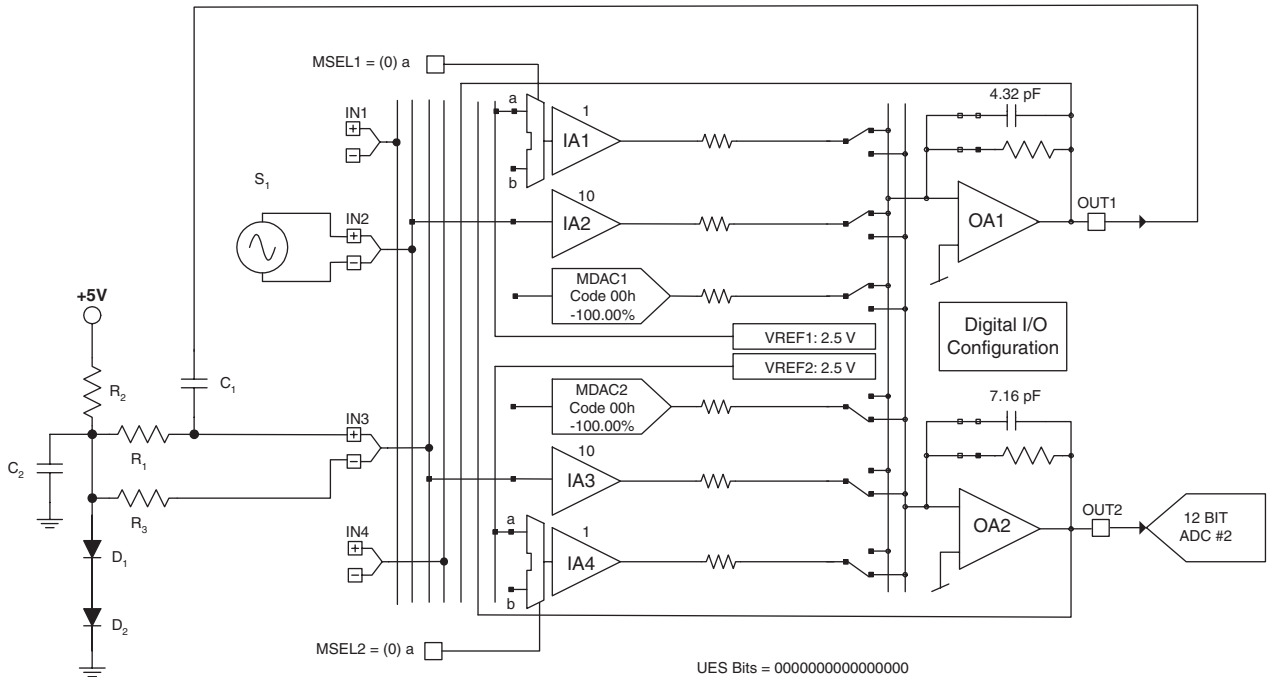
and IAs) to provide maximum output swing (+/- 2.5 V above and below the 2.5 V bias point). After adding this DC bias to the output of OA1 we must remove it before passing the signal to the inputs of the cascaded IAs. Otherwise, a minimum gain of +2 would place the second OA at +5 V. The DC bias present in OA1 is easily removed using an external high pass filter, as shown in Figure 9. R_1 and C_1 combine to form a first order high-pass filter that blocks the 2.5V bias from OA1. For example, a 10Hz corner frequency (f_C) can be obtained using C_1 of 10 μF and R_1 of 1600Ω. Other corner frequencies can be obtained from the following equation:

$$f_C = \frac{1}{2\pi R_1 C_1} \quad (2)$$

Diodes D_1 and D_2 provide an inexpensive (1N4148) and ideal low-impedance 1.4V bias for the ispPAC30 inputs (centered in the 2.8V input range). R_2 limits the idle current of the diode chain (typical values of 2 to 10 mA can be obtained with resistance values of 2k to 360Ω respectively). Capacitor C_2 filters the 1.4V reference and, for good dynamic performance, the time constant R_2C_2 should be ten times greater than R_1C_1. Resistor R_3 biases the (-) input to the same potential as the (+) input (the virtual ground of 1.4V). To null any offset in the input bias currents R_2 and R_3 should be of the same value (10% is adequate because the ispPAC30 input bias currents are in the pA range). Note that this same 1.4V input circuit can also be applied to other AC sources that may need a DC level shift.

The combination of adjustable IA gain and MDAC trim provide designers with flexible solutions to the wide variety of gain and offset configurations. All of these features are fully configurable using E^2CMOS for non-volatile storage, or SRAM registers for real-time changes.

Figure 9. Cascading the ispPAC30 for Voltage Gains of 100 or More

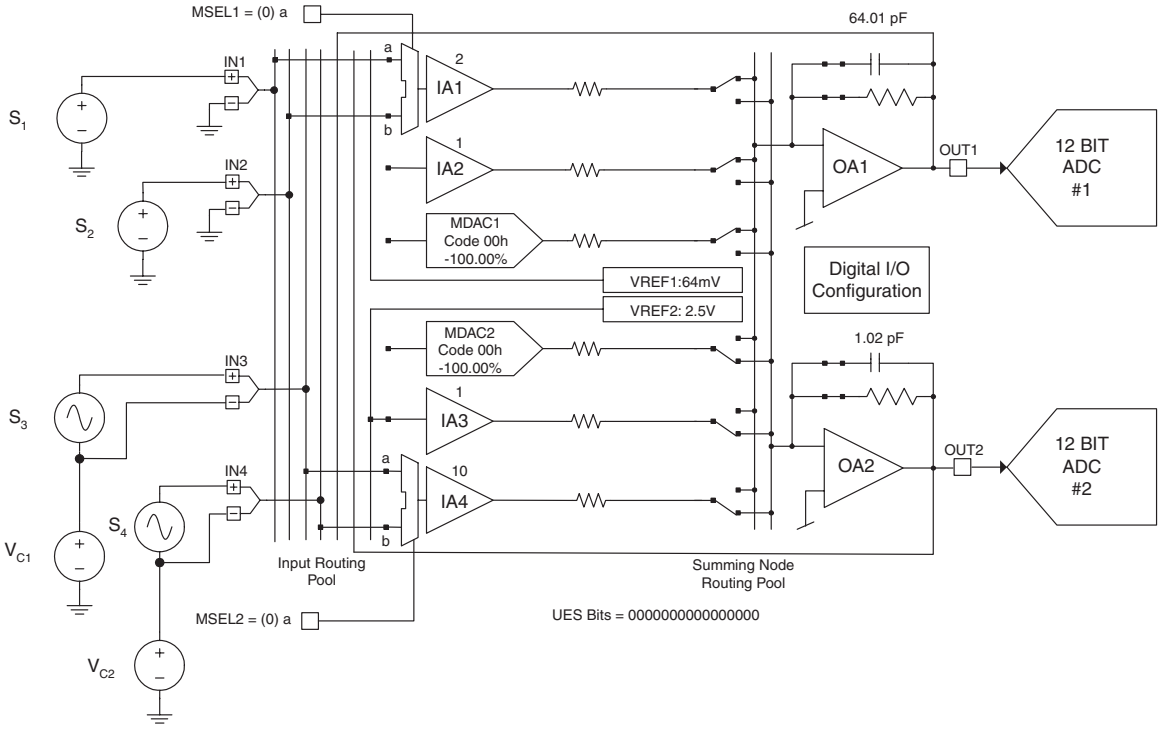


3.7. Multiplexing Signals

Many data acquisition systems use a multiplexer (MUX) so that a single ADC can measure several input signals in a sequential fashion. The ispPAC30 has three mechanisms to MUX signals from the input pins to the output pins and they are: two-input MUX, input routing pool, and the summing node routing pool. There are two dedicated MUXes, one for IA1 and one for IA4. The “a” and “b” inputs of each MUX may be connected to the four differential inputs, the precision voltage reference, or either of the two OAs.

In Figure 10 we see two single ended DC sources (S_1 and S_2) connected to the inputs (+) 1 and (+) 2. Then the input routing pool takes the signals to MUX1 inputs “a” and “b” respectively. In the lower portion of the figure, two differential AC sources (S_3 and S_4) are connected to the inputs 3 and 4. Again the input routing pool takes the signals to MUX2 inputs “a” and “b” respectively. Assuming the amplitude of the AC signals to be small, IA4 is set to a gain of 10. Because the ispPAC30 is a single supply device and the OAs are single ended, VREF2 and IA3 are configured to center the output at midpoint, providing a virtual ground at +2.5V. Each MUX may be controlled independently and directly by its MSEL pin, which has programmable polarity and can be driven with standard 3.3V or 5V logic levels. Each MUX can also be controlled indirectly by modifying the respective polarity bit using SPI (see application note AN6027, *Using SPI to Configure and Control the ispPAC30*). The input routing pool can also be modified by SPI to dynamically reconfigure the inputs of the MUXes, IAs, and MDACs. While the summing node routing pool is used primarily to connect the outputs of the IAs and MDACs to either of the two OAs, it can also be modified by SPI to redirect signals.

Figure 10. Dual MUXes Select from Four Input Sources



The input MUXes can also be used to connect a known reference or calibration signal. The known reference can be switched in using the MSEL pin and then the ADC can be calibrated to the known good signal level. This method will allow a microprocessor to record and store a value, then mathematically calibrate a given constant for gain or offset error. The input MUXes and internal routing of the ispPAC30 broaden the applications and increase the functionality of the inputs without adding external circuitry nor do they impact signal quality in any way.

3.8. Input Impedance

Input impedance is an important consideration for analog front ends. It is desirable to have high input impedance to prevent loading the source and introducing measurement errors. The differential and common mode input resistance, for both the IAs and MDACs in the ispPAC30, are 10^9 Ω (minimum). This magnitude of input resistance is sufficiently high that only applications measuring very small signals from a very high impedance source would be affected by it. If an input is routed to all four IAs and both MDACs, the resulting input resistance would still exceed 10^8 Ω. The input pins have a small capacitive load of 2 pF (typical). To put these values in perspective, a standard oscilloscope probe presents more of a load to a source than the ispPAC30 inputs. In standard op-amp circuits, the input and feedback networks determine the input impedance and frequency dependence. Thus, the input impedance can vary as a function of either gain or frequency and may reduce the accuracy of the measurement by load-

ing down the source. However, with the ispPAC30, this is not the case because the integrated differential instrumentation amplifiers maintain their very high input impedance regardless of gain and frequency settings. Also note that the inputs can accurately sense signals at ground and even a few hundred mV below ground.

3.9. Output Impedance

The output impedance is also an important parameter to consider and many times is overlooked in a data acquisition system. The input of the ADC and the output of the device driving it must be examined together to determine the maximum sampling frequency of the system. The dynamic input of most ADCs is primarily capacitive and the output of most op-amps is resistive (or low impedance current source). Thus, a minimum time constant exists which corresponds to a maximum sampling frequency. For the ispPAC30, the output impedance is very low and has the capacity to source or sink up to 30 mA. The increment of time (Δt) required for the ADC input voltage to change (ΔV) is a function of the maximum drive current (I) and the input capacitance (C), as shown in the following equation.

$$\Delta V = \frac{I\Delta T}{C} \tag{3}$$

Solving for time and converting to the maximum sampling frequency (f_S) is fairly straightforward as shown below:

$$f_S = \frac{1}{\Delta t} = \frac{I}{\Delta VC} \tag{4}$$

As a worst case example, assume the voltage must swing the full range (5V) and the ADC input capacitance is 300 pF. Using the 30mA drive of the ispPAC30, the resulting maximum sampling frequency is 20MHz. Therefore, the ispPAC30 is an ideal ADC front end for applications that implement over-sampling and digital filtering techniques.

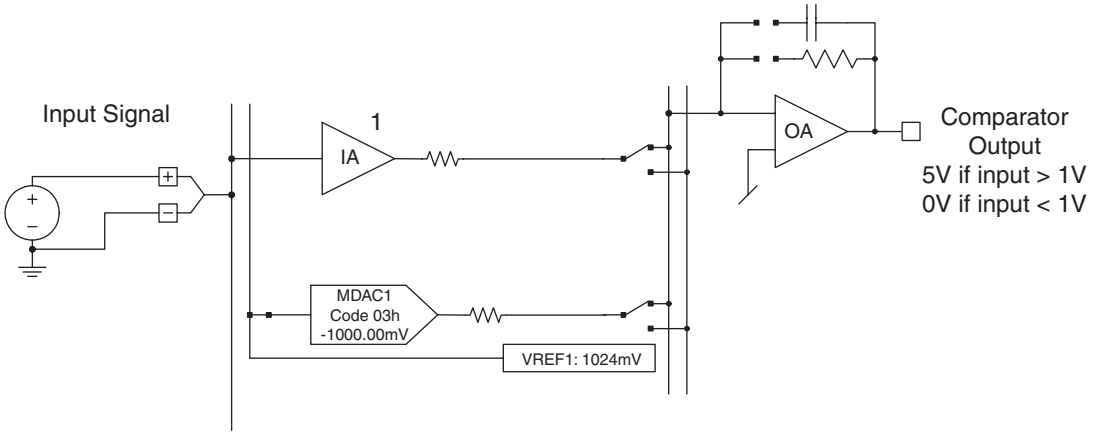
3.10. Low-Power Modes

The ispPAC30 can be used in applications that require power conservation. The architecture is set up internally to automatically disable sub-circuits that are not part of the signal path. For example, if an IA is not connected to any signal at its input, it is internally shut down to minimize power consumption. Additionally, each OA can be powered-down when not in use. When the OA is powered down, the output is disabled and has a high impedance. Thus, other circuits could be switched into the node for calibration or control (based on the application). The entire device can also be powered-down by activating the PD-pin (active low), or sending the corresponding SPI instruction. In this mode, the digital circuits remain active waiting to respond to the SPI power-up instruction or the de-activation of the PD-pin.

3.11. Over-range Detection

The ispPAC30 architecture allows the designer the capability to configure one or both of the output amplifiers to function as a comparator. As shown in Figure 11, the reference and MDAC are used to set the threshold or trip point. When the OA is configured as a comparator it only has a single input which still serves as a summing node. When the sum is greater than zero, the output is +5V, and when the sum is less than zero, the output is at ground level. An example application using this technique is monitoring a signal for a maximum value. The output of the comparator can then be used to signal an over voltage or out of range condition. Under processor control, this feature can be used for auto-ranging or over range monitoring.

Figure 11. Over-Voltage Comparator



4. Summary

The ease of use and highly reconfigurable architectures highlighted in the previous sections has shown the ispPAC30 as a valuable solution that integrates multiple features for an ADC front-end. We have seen that the ispPAC architecture provides adaptability during and beyond the design phase of a project. As an anti-alias filter the ispPAC30 provides a selectable first order low-pass filter. This device is also very configurable when it comes to gain, offset adjustment, and providing precision voltage references. As a multiplexer, there are the built-in MUXes, or using SPI and SRAM, the whole device is a multi-point cross-switch. The input impedance is very high and the output impedance is very low. The inputs can sense signals slightly below ground for either single ended or differential signals. And the ispPAC30 offers several power conservation mechanisms. The table below confirms that the ispPAC30 solution is superior to a typical discrete circuit. The discrete solution would (vary depending on implementation) require over 20 op-amps, four programmable gain networks, four 6-input differential MUXes, two 10-bit DACs, two adjustable voltage references, and numerous MUXes, resistors and capacitors.

Table 1. Comparison of ispPAC30 to Discrete Solution

Feature	ispPAC30	Discrete
Adaptability	Excellent	Poor
Frequency Accuracy	Excellent	Good
Offset Adjustment Range	Excellent	Poor
Gain Resolution	Excellent	Good
Differential Multiplexing	Excellent	Good
Input impedance	Excellent	Excellent
Output impedance	Excellent	Excellent
Differential / Single Ended	Excellent	Good
Power Down Capability	Excellent	Poor
Ease of Design	Excellent	Poor
Cost	Excellent	Poor
Board Real Estate	Excellent	Poor

Technical Support Assistance

Hotline: 1-800-LATTICE (Domestic)
1-408-826-6002 (International)
e-mail: ispPACs@latticesemi.com

Appendix A. Transconductance Amplifiers within the ispPAC30

For the sake of simplicity, all of the schematics for the ispPAC30 are drawn to show the internal signals as single ended voltage sources. In reality, the outputs of both the IAs and MDACs are differential voltage to current amplifier modules (as illustrated in Figure 12). The differential current outputs are summed into the input nodes of the OA. The OA then buffers the combined signals and presents it to the output pin. To maintain signal integrity and low distortion, the current drive capability of the IAs is designed to exceed the value required to pass signals within the supply range. In fact, one can take advantage of this headroom with a penalty of an additional gain error of 3% (total 6%) and the output currents can represent an equivalent voltage of +/- 8.5V (obtained for example by an input of 2.125V amplified by a gain of 4). If this current is not countered by another IA at the summing nodes, the OA will saturate at 0 or 5V (based on the polarity). Understanding these inner workings of the ispPAC30 enable offset or bias adjustments that actually exceed the supply by 3.5V.

Figure 12. Example of the Differential Internal Circuitry of the ispPAC30