



# LatticeMico System Software Release Notes for Lattice Diamond 2.0.1

The LatticeMico System Software includes changes to the Lattice Mico System Builder (MSB) and Software Project Environment (C/C++ SPE) for Lattice Diamond® version 2.0.1.

## What's New in LatticeMico System

- ▶ Updated LatticeMico EFB for MachXO2 component as follows:
  - ▶ Added support for User-Managed Timer Reset mode.
- ▶ Updated C/C++ SPE Help (changed **Run > Debug** to **Run > Debug Configurations**).
- ▶ Updated LatticeMico32 Tutorial (changed **Run > Debug** to **Run > Debug Configurations**).

## Release Compatibility

LatticeMico System Builder platforms developed prior to the release of Lattice Diamond 1.1 (or ispLEVER 8.1 SP1) may need to be analyzed and subsequently updated. Users who open a platform containing one of the components listed below, at the version shown or older, will be given the option to update the platform:

- ▶ SPI Flash v3.2
- ▶ DMA v3.1
- ▶ UART v3.4
- ▶ GPIO v3.1

Users who choose to update a platform with a newer version of these components may need to make modifications to their C/C++ source code. It may also be necessary to update any RTL source code instantiating the LatticeMico System Software generated platform.

To get an understanding of how the newer version of these components affects the C/C++ and RTL code please read LatticeMico32 Technical Note [1221](#). It has a complete description of the changes made, the situations where there will be an impact your existing design, and instructions on how to update your design if it is required.

---

## Trademarks

Lattice Semiconductor Corporation, L Lattice Semiconductor Corporation (logo), L (stylized), L (design), Lattice (design), LSC, CleanClock, Custom Mobile Device, DiePlus, E<sup>2</sup>CMOS, Extreme Performance, FlashBAK, FlexiClock, flexiFLASH, flexiMAC, flexiPCS, FreedomChip, GAL, GDX, Generic Array Logic, HDL Explorer, iCE Dice, iCE40, iCE65, iCEblink, iCEcable, iCEchip, iCEcube, iCEcube2, iCEman, iCEprog, iCEsab, iCEsocket, IPexpress, ISP, ispATE, ispClock, ispDOWNLOAD, ispGAL, ispGDS, ispGDX, ispGDX2, ispGDXV, ispGENERATOR, ispJTAG, ispLEVER, ispLeverCORE, ispLSI, ispMACH, ispPAC, ispTRACY, ispTURBO, ispVIRTUAL MACHINE, ispVM, ispXP, ispXPGA, ispXPLD, Lattice Diamond, LatticeCORE, LatticeEC, LatticeECP, LatticeECP-DSP, LatticeECP2, LatticeECP2M, LatticeECP3, LatticeECP4, LatticeMico, LatticeMico8, LatticeMico32, LatticeSC, LatticeSCM, LatticeXP, LatticeXP2, MACH, MachXO, MachXO2, MACO, mobileFPGA, ORCA, PAC, PAC-Designer, PAL, Performance Analyst, Platform Manager, ProcessorPM, PURESPEED, Reveal, SiliconBlue, Silicon Forest, Speedlocked, Speed Locking, SuperBIG, SuperCOOL, SuperFAST, SuperWIDE, sysCLOCK, sysCONFIG, sysDSP, sysHSI, sysI/O, sysMEM, The Simple Machine for Complex Design, TraceID, TransFR, UltraMOS, and specific product designations are either registered trademarks or trademarks of Lattice Semiconductor Corporation or its subsidiaries in the United States and/or other countries. ISP, Bringing the Best Together, and More of the Best are service marks of Lattice Semiconductor Corporation.

Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.