Release Notes for ispLEVER 8.1

Welcome to ispLEVER®, the complete design environment for Lattice Semiconductor FPGAs. This version of ispLEVER adds a variety of enhancements to make designing for Lattice Semiconductor programmable devices easier than ever. The design tools also include support for the latest Lattice Semiconductor devices. See “What's New in ispLEVER” on page 2.

Some of the changes affect how you import designs from previous versions of ispLEVER. For more information, see “Using a Project from an Earlier Version” on page 3.

Known issues and workarounds are described in the Lattice Forums on the Lattice Semiconductor Web site:

www.latticesemi.com/latticeforums

Under “Questions & Answers,” find “ispLEVER Known Issues” and click on the version number.

Under Design Tools and IP, click **ispLEVER** for the latest questions and answers. You can also ask questions in the Lattice Forums.

Lattice Semiconductor offers a rich variety of information sources, from the Help system to tutorials to online discussions. The easiest way to reach them all is through the online Help. The first topic in “Introduction to ispLEVER Documentation” provides links to all the other sources of information.

If you are new to ispLEVER, the “Quick Start Guide for ispLEVER Software,” also available through the Help, provides a quick and easy introduction to the design process using ispLEVER design tools.

What's New in ispLEVER

This release of ispLEVER provides a variety of new features in the following areas. See the online Help for details.

Operating Systems UNIX is no longer supported by ispLEVER.

New Device Support Preliminary support with bitstream file output is available for the following devices:

- LatticeECP3-17EA

Command Line The command line program formerly called MEMEDIT has now been enhanced and has been renamed MEDIT. The functionality includes the ability to create an output .mem file in another format other than what the file was originally created in. For example, if it was in hexadecimal, you can output it in binary. This feature is implemented in the ispLEVER interface with the Memory Initialization tool. For more details, see Running MEDIT from the Command Line.

Design Planner Advanced PIOs DRC Check has been added to help ensure error-free placement and routing.

IPexpress IPexpress™ contains numerous improvements to existing modules.

ispVM System The ispVM® System software has been upgraded to version 17.8. The USB port driver for the ispDOWNLOAD USB cable now supports 64-bit Windows Vista and Windows 7 operating systems.

PAC-Designer (Available only in the Windows version.) PAC-Designer has been updated.

Project Navigator A new property, Generate PUR in the Netlist, was added to control whether the Generate Timing Simulation Files process writes PUR instances to the Verilog/VHDL backannotation netlist.

I/O Assistant has been enhanced to check that the clock placement for generic DDR interfaces on LatticeECP3 will result in legal clock routing.

I/O Assistant also has a new process for IBIS Model generation.

Simulation and Synthesis Tools Synplify® for Lattice is no longer available. However, the Synopsys® Synplify Pro® for Lattice synthesis tool is still included with ispLEVER and has been updated. If you were using Synplify for Lattice, your project will automatically start using Synplify Pro in ispLEVER 8.1. If Synplify works better than Synplify Pro for your project, call Lattice Technical Support to report the gap.

(Windows version) The Aldec® Active-HDL™ Lattice Edition simulator has been updated.

Using a Project from an Earlier Version

If you want to work on a design project created with an earlier version of ispLEVER, start with the following procedures. These procedures adapt the project for the following changes in ispLEVER.

Find out which version of ispLEVER your project was created with. Then work through the changes for every later version, starting with the earliest and going to the most recent. For example, if your project was created with ispLEVER 7.2, you would start with the changes for 8.0. After completing those changes you would work on the changes for each later version (8.1).

Starting in ispLEVER 8.1 Synplify for Lattice is no longer available. If you were using Synplify for Lattice, your project will automatically start using Synplify Pro in ispLEVER 8.1. If Synplify works better than Synplify Pro for your project, call Lattice Technical Support to report the gap.

There has been an enhancement to the LatticeECP3 PLL library element (EHXPLLD) to improve simulation accuracy of PLL configurations where the feedback path is driven by a PLL port other than CLKOP. However, this enhancement can cause certain existing LatticeECP3 designs that use PLL to generate a MAP error:

```
ERROR - map: The CLKFB of EHXPLLF component 'EHXPLLD_TX/
PLLInst_0' has feedback connection, but the FEEDBK_PATH
property has a value of 'CLKOP' that does not match
connectivity.
```

Regenerate the LatticeECP3 PLL using IPexpress if either:

- The PLL is driving the PLL feedback from a port other than CLKOP (for example, CLKOS). This will improve the simulation accuracy.
- You experience the MAP error above.

The MAP error can occur on certain Lattice IPs targeted to LatticeECP3:

- DDR3 1.0
- SPI4 2.6
- TSMAC 3.2

These IP will be updated and made available through IPexpress. To clear the MAP error, check for an update and regenerate the IP.

A manual workaround exists that does not require regenerating the IP. Contact Lattice Technical Support for details.

Starting in ispLEVER 8.0 There have been many enhancements for LatticeECP3. For a full explanation of migrating a LatticeECP3 design from ispLEVER 7.2 or earlier, see TN1180, “LatticeECP3 High-Speed I/O Interface.” Following is a summary of the migration issues.

Targeting LatticeECP3-70E or -95E:

- DDR interfaces should be rebuilt using IPexpress to ensure robust behavior.
- The design must be rerun through MAP and PAR. A new design rule check blocks designs that do not use direct routing for clocks in DDR interfaces. This ensures robust behavior of the DDR interface. However, it may require changing the pinouts to allow direct clock routing. Contact Lattice Technical Support with issues.

Targeting ECP3-150EA:

- DDR interfaces must be generated from IPexpress. Existing DDR interfaces will likely not work in newer versions of ispLEVER. This change opens up access to the enhanced DDR features of EA devices.
- The design must be rerun through MAP and PAR. A new design rule check blocks designs that do not use direct routing for clocks in DDR interfaces. This ensures robust behavior of the DDR interface. However, it may require changing the pinouts to allow direct clock routing. Contact Lattice Technical Support with issues.
- If using a PCS module from IPexpress for a protocol other than PCIe, the module must be regenerated so that the calibration value for loss of signal is optimally set for EA devices.

Starting in ispLEVER 7.2 The way in which TRACE reports interclock domain transfers between unrelated clocks has changed. Two clock signals are defined as unrelated if they are not driven by the same clock input pad and you have not defined a relationship between them using the CLKSKEWDIFF preference.

Prior to ispLEVER 7.2, data transfers between unrelated clocks were reported as if those clocks were related and had a skew of 0. In ispLEVER 7.2 and later, data transfers between unrelated clocks are not reported. If you want to have those transfers reported, they must define a clock relationship between the two external clocks using the CLKSKEWDIFF preference. This updated behavior in TRACE avoids needlessly over-constraining a design. For example, data crossing between two asynchronous clocks should be analyzed during simulation. Static timing analysis cannot be used to guarantee proper operation. So, the former default constraint added no value, and could negatively impact design performance.

For designs with unrelated clock signals, this updated TRACE behavior in ispLEVER 7.2 and later reduces the number of paths reported and results in a higher f_{MAX} if those paths were the most critical paths in the pre-ispLEVER 7.2 design. The following is an example from the new Clock Domains Analysis section in the Trace report where two clocks are considered unrelated and the data crossing between them is not reported.

```
Clock Domain: Comclk_i_int   Source: Comclk_i.PAD
  Not reported because source and destination domains are
  unrelated.
  To report these transfers please refer to preference
  CLKSKEWDIFF to define external clock skew between clock
  ports.
```

For designs where two unrelated clocks did actually have a relationship, and that relationship was zero skew, you must now add an explicit CLKSKEWDIFF preference to the logical preference (.lpf) file as follows to get the equivalent analysis that was done prior to ispLEVER 7.2:

```
CLKSKEWDIFF CLKPORT "clock1" CLKPORT "clock2" 0ns;
```

The Clock Domains Analysis section will list all data transfers between clocks that are not reported because the clocks are considered unrelated. You should verify that all of these clock pairs are actually unrelated. A good design practice is to verify the proper operation of data crossing unrelated clock domains using simulation.

Starting in ispLEVER 7.1 The default simulator and synthesis tool are Aldec Active-HDL Lattice Edition and Synopsys Synplify Pro for Lattice, respectively. There are also other improvements that affect the use of timing preferences and some aspects of LatticeSC/M projects (see below).

If you convert from:

- ModelSim® Lattice to Active-HDL, replace any ModelSim .do scripts with equivalent Active-HDL macro commands. See the Active-HDL Help. Recompile the design with Active-HDL.
- Precision® RTL Synthesis to Synplify, replace any Precision attributes with equivalent Synplify attributes. See the Synplify Help. Rerun synthesis (the Build Database process in Project Navigator) with Synplify.

For Synplify Pro synthesis processes, the Run Retiming property has been replaced by Pipelining and Retiming. No matter how Run Retiming was set previously, the current ispLEVER software automatically sets the Pipelining and Retiming property to its default value of Pipelining and Retiming.

A more powerful TRACE engine makes placement and routing much faster and uses less memory. To take full advantage of faster run times, use the more efficient logical equivalents of physical timing preferences MULTICYCLE, OFFSET, MAXDELAY, DEFINE STARTPOINT, DEFINE ENDPOINT, BLOCK, and DEFINE PATH.

Several IP have corrections and enhancements that require replacing them. If your design uses any of the following IP from ispLEVER 7.0 SP2 or earlier, download and install the latest version of the IP:

- CSC
- DDR1
- DDR2
- Ether_10G
- FIR
- HiGig_MAC
- PCI_MT33
- PCI_T33
- PCI_MT66

- PCI_T66
- SPI4
- MACO DDR/DDRII
- MACO PCIE
- MACO RLDRAM
- MACO SPI4

The options for the Consistent Bus Name Conversion property changed from True/False to Synplify, Precision, Lattice, and None. No matter how the property was set previously, the current ispLEVER software automatically converts it to None. The Consistent Bus Name Conversion property is associated with the following processes:

- Build Database
- Assemble Database
- Build Toplevel Database
- Compile EDIF File

If you have a LatticeSC/M project that uses an:

- Edge clock (ECLK), regenerate your design from source in the new version of ispLEVER. If you need to convert an existing pre-7.1 .ncd for use in the new version of ispLEVER, contact Lattice Semiconductor technical support for assistance.
- SDR or DDR module netlist with AIL=ON and a user-defined delay (DELAY block), regenerate the netlist with the latest version of IPexpress. Or, you can manually edit your netlist to change FDEL0 to FDEL24 because valid values are now 8-29, and 24 is recommended.

For LatticeXP2 designs, the RAM_DQ and RAM_DP_TRUE modules no longer support the Write Mode option: Read Before Write Operations. Previously Read-before-write was supported for memory configurations in multiple of x9 data width for LatticeXP2. If read-before-write is used in a pre-ispLEVER 7.1 .lpc file, it will be caught by the design rule check (DRC) during mapping and the warning message will instruct you on how to proceed.

Starting in ispLEVER 7.0 SP2 The default value of the DCSMODE attribute in the DCS (Dynamic Clock Selection) library macro changed from POS to NEG. If your design includes the DCS macro and you did not specify the DCSMODE value, manually set it to POS.

Starting in ispLEVER 7.0 SP1 The master clock frequency for LatticeECP2/M S-Series devices is limited to six options for encrypted and unencrypted bitstreams. If your design is for a LatticeECP2/M S-Series device, select a master clock frequency in the Design Planner's Global Preferences sheet and regenerate the bitstream.

Also, if the S-Series design includes EDIF from IP modules that you intend to convert to .ngo files (with the Build Database process or edif2ngd), re-create the EDIF using the current version of ispLEVER.

Starting in ispLEVER 7.0 Device databases for LatticeECP2M, LatticeSC/M, and LatticeXP2 projects use a different format that improves memory use. The database is updated automatically when the project is first opened. You will need to rerun processes starting with Map Design. In block modular projects, rerun processes starting with Map Design on all sub-modules. We recommend making a copy of your original project because the new database cannot be used with previous versions of ispLEVER.

Starting in ispLEVER 6.0 The ModelSim .udo file does not have the vsim command. This prevents the file from being overwritten by the Project Navigator when the target device is changed. If the design includes a ModelSim .udo file, open it with a text editor and remove the vsim command.

Starting with ispLEVER 5.1 Two preference files are used instead of one: a logical preference file (.lpf) and a physical preference file (.prf). Your preference inputs are written to the .lpf file, and the Map Design process creates the .prf file. The .prf file contains only physical preferences.

To migrate designs created with ispLEVER 5.0 or earlier:

First, make the change to the .udo file described above.

1. Create a backup copy of your design. Once migrated to the current version of ispLEVER, the earlier version will not be able to open the design.
2. Open the project in the new Project Navigator.

   A message stating that the current version of ispLEVER requires the .lpf file appears.
3. Click **Yes**.

   The logical preferences from the earlier .prf file are copied to a new .lpf file.
4. In SYSCONFIG preferences that have a “SPI3” mode value for the CONFIG_MODE keyword, change the value to “SPI”. You can change the value in both the .lpf and .prf files using a text editor, or with the Design Planner's Spreadsheet view.

Contacting Technical Support

Online Forums The first place to look. Lattice Forums contain a wealth of knowledge and are actively monitored by Lattice Applications Engineers.

Telephone Support Hotline Receive direct technical support for all Lattice products by calling Lattice Applications from 5:30 a.m. to 6 p.m. Pacific Time.

- For USA & Canada: 1-800-LATTICE (528-8423)
- For other locations: +1 503 268 8001

In Asia, call Lattice Applications from 8:30 a.m. to 5:30 p.m. Beijing Time (CST), +0800 UTC. Chinese and English language only.

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