ispLEVER 8.0 Release Notes for LatticeECP3 Migration

November 2009 **Release Notes RN01**

Instructions to Migrate Existing LatticeECP3 Designs to ispLEVER 8.0

ispLEVER® 8.0 is a significant upgrade particularly for LatticeECP3™ users. Some steps must be taken to migrate existing LatticeECP3 designs to ispLEVER 8.0. You can continue to use both LatticeECP3 "E" and "EA" devices in version 8.0. There are many more details in TN1180 (version November 2009 or later), LatticeECP3 High-Speed I/O Interface, but following is a summary of the steps.

Note. These steps differ slightly between the "E" devices (ECP3-70E and ECP3-95E) and the "EA" devices (ECP3-150EA).

Remember – always make a backup copy of the design before migration.

- When a project that has been created in a release previous to ispLEVER 8.0 is opened, there will be a dialog box which informs you that this design must be recompiled. Recompiling will create new design files, and avoid using older design files that are no longer compatible with ispLEVER 8.0 tools.
- The process will automatically reset back to the Synthesis step. The user initiates the actual recompilation processing (e.g. starting the Place & Route process will start the Synthesis, MAP and PAR processing).
- It may be necessary to also regenerate some Modules or IP which have been used in the design to successfully recompile. See specific details for the "E" and "EA" devices below.
- It is highly recommended that all Modules or IP which use DDR or PCS/SERDES be re-generated under version 8.0.
- "E" Devices:
  - Rerun MAP and PAR and check pinout. A Design Rule Check (DRC) has been added to report (and block design implementation) whenever at least one general route segment is used within the clocking network for DDR interfaces. General routing used on the clock network can reduce the robust operation of the DDR interface. Pin placement must be altered as necessary to clear this DRC (a DRC failure will not allow the design to continue in the flow and generate a bitstream). If you are unable to clear this DRC, contact Lattice Technical Support.
  - Highly recommended for existing DDR interfaces: any DDR interface that is used should be generated from IPexpress™. The interfaces from IPexpress have all been validated to run at speed on hardware. Therefore, replace each existing hand-coded DDR interface with the equivalent interface from IPexpress.
- "EA" Devices:
  - Same as "E" devices above. The same DRC has been added to "EA" devices. Re-generation of DDR interfaces from IPexpress is mandatory for "EA" devices as some of the primitive library elements used for "EA" have changed in ispLEVER 8.0. IPexpress will generate interfaces using the latest library element definitions.

Additional LatticeECP3 Support Details

- **General**: All users targeting the LatticeECP3 device family are strongly encouraged to update to ispLEVER 8.0.
- **Pin locking prior to design complete**: It is common to want to lock pins prior to design completion to get a start on board design and manufacturing. The IO Assistant flow allows users to run an incomplete design through PAR to verify their pinout is legal. However, with DDR interfaces on LatticeECP3, this will not complete all the design rule checks. Therefore, the IO Assistant flow should not be used, and instead, designs should be run through regular PAR. The final design does not need to be done, but it must be complete in that there are no dangling nets. See the section titled, "Steps to Generate a Valid Pinout for a High-Speed DDR Interface" in TN1180, LatticeECP3 High-Speed I/O Interface for more details.

- **DDR – general**: Use the circuits that are generated from IPexpress. These have all undergone extensive testing through static timing analysis and operation on the board. Deviating from these interfaces must only be done with direct Lattice Technical Support. Therefore, if you believe that you need to deviate from these interfaces, contact Lattice Technical Support.
- **DDR3**: Continue to contact Lattice Technical Support if you are planning to implement DDR3 in the LatticeECP3.
- **PCI Express Interface Support (PCS/SERDES)**: The LOS Threshold value has been adjusted for PCS Modules created from IPexpress for the PCI Express protocol. Previously, users could choose between a value of 2 or 3. Now, only a value of 2 can be chosen. It is recommended that such PCS Modules are re-generated if a value of 3 was previously used. This is not a requirement – designs using 3 will be allowed through the ispLEVER 8.0 flow.

Technical Support Assistance

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Revision History

Date	Version	Change Summary
November 2009	01.0	Initial release.