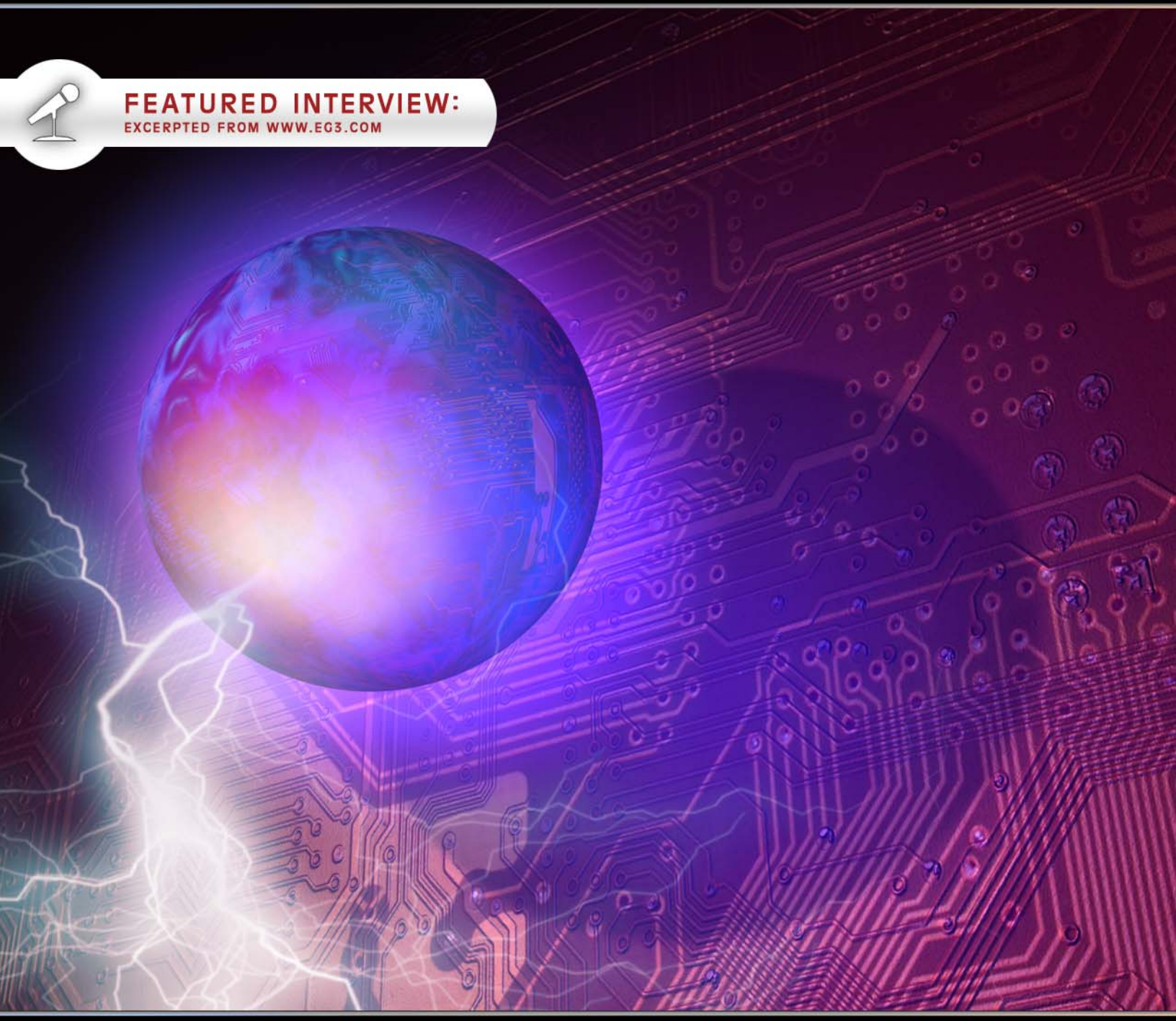
INSIDERS' GUIDE:

FPGAs, TOOLS, AND BOARDS



FEATURED INTERVIEW:
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Prepared by:
eg3.com
Jason McDonald, Senior Editor

eg3.com
tel: 510.713.2150
email: info@eg3.com
web: http://www.eg3.com

LATTICE SEMICONDUCTOR CORP.: TRUE NON VOLATILE AND FULL FEATURED, ECONOMICAL FPGA'S

1 October 2008: True Non-Volatile and Full Featured, Economical FPGAs

INTERVIEWEE. DOUG HUNTER
DIRECTOR OF CORPORATE MARKETING
TEL. 503-268-8000
EMAIL. doug.hunter@latticesemi.com
COMPANY. LATTICE SEMICONDUCTOR
WEB. http://www.latticesemi.com/

Q. **Obviously, the two giants in FPGA are Altera and Xilinx. Help us help our readership by giving us a few bullet points of how Lattice is unique and different in your technology offerings.**

A. A primary focus of ours is non-volatile FPGAs. By combining SRAM and Flash memory on a single die, we provide single chip, instant-on and highly secure design solutions.

We also focus on FPGAs that combine economy with high-end features such as 3.125Gbps SERDES, DDR2 and full-feature DSP.

More specifically, for single chip, high security and instant-on operation, the LatticeXP2™ is the industry's only true 90nm non-volatile FPGA solution. For economical FPGAs with SERDES, high memory content, high end DSP or DDR2, the LatticeECP2M™ is the industry-leading device.

Lattice also provides the Lattice ispMACH® 4000ZE, an ultra low-power CPLD family, and the Lattice MachXO™ "crossover" PLD that combines the benefits of CPLDs and FPGAs. Our product portfolio also includes innovative programmable mixed signal products for clock and power management applications.

Q. **When we talked about this interview, beforehand, you indicated that Lattice takes a lot of pride in producing affordable FPGAs that are "fuller featured." Can you expand on how your products provide more features at a lower cost for FPGA-based projects?**

A. When Lattice entered the FPGA market there were already entrenched competitors. To be successful, we chose to develop highly differentiated products that delivered a compelling value proposition to our customers. So, we focused on two key differentiators – non-volatility and economy --and set about developing technology and products in each area.

Traditionally, FPGA companies have focused on two basic product lines: low-cost devices with reduced features, and high-cost devices that are feature rich. Historically, low-cost FPGAs were little more than stripped down versions of higher end devices. So the value proposition was "spend less, get less." Not very compelling. We saw an opportunity to fill a void in the market by developing an economical, feature rich FPGA product line. We were able to do this by designing these FPGAs from the ground up. From initial planning with customers through architectural definition, design and choice of manufacturing process technology, we designed our economy FPGAs with the features system designers agree are essential to high-volume applications, and delivered them at a price that has finally made widespread adoption of high-volume FPGAs economically attractive. Some of the techniques that make this possible include the use of

compact wirebond, rather than flip chip, packaging, hybrid analog digital SERDES for an area savings of approximately 60% and considered architectural decisions, such as optimized, selective support for distributed memory. Also, while competitive devices were using expensive proprietary boot PROMs to load the configuration, we designed our FPGAs to work with inexpensive third party SPI memories, at a cost per bit many times lower than the proprietary boot PROMs.

Q. **Tell us a little bit about the software tools that come with Lattice. Are they free? How do they compare with those of Xilinx or Altera?**

A. Lattice provides a variety of FPGA and CPLD software design tool suites so that our customers can choose the one that best fits their needs and budget. We also provide a design tool suite for our mixed-signal products, and an Integrated Development Environment (IDE) for our Mico32 embedded microprocessor, the industry's only open source microprocessor.

Two of our tool suites, ispLEVER Starter and ispLEVER Classic, are downloadable from the Lattice website at no cost. Our flagship, full featured tool suite, ispLEVER, is $1295 and is available in Windows, UNIX and Linux versions.

New users who previously have designed with Xilinx or Altera tools are able to adapt quickly to Lattice tools. Unlike Xilinx and Altera, though, we include within our tool suite synthesis and simulation tools, optimized for Lattice devices, from EDA industry leaders Aldec and Synplicity. We believe that a combination of industry-leading front-end tools with our own proprietary back-end tools is a powerful value proposition for our customers. Our tool set includes many unique capabilities, including our Power Calculator, which allows a customer to specify parameters such as voltage, temperature, process variations, air flow, heat sink, resource utilization, activity and frequency, which in turn calculates a device's static (DC) and dynamic (AC) power consumption. Our Reveal logic analyzer is our next-generation in-system logic analysis tool that uses a signal-centric model for embedded logic debug. Our ORCAstra software is a Windows-based graphical user interface that enables configuration of the operational modes of our FPGAs by programming control bits into on-chip registers. This new ability to explore configuration options quickly, without recompiling the FPGA design, dramatically speeds design validation.

Q. **One area that Lattice has had early leadership in is in "non-volatility." Can you explain the reasons why FPGA developers might prefer non-volatility, and what Lattice offers that leverages this desire?**

A. Non-volatile technology has always been the technology of choice for programmable logic because it provides unique system-level benefits such as a single-chip solution, instant-on capabilities and high security. While historically there has been a significant price premium for non-volatile devices, Lattice provides this sophistication without significantly impacting the cost or performance of the product.

It's important to understand that true non-volatile FPGAs employ high-performance, embedded Flash memory technology. We have worked closely with our foundry partner Fujitsu to develop proprietary embedded Flash technologies that enable exceptionally high performance.

"Instant-on," a feature that allows an FPGA to be used immediately upon startup, is essential in many applications. Typical SRAM FPGAs require 10s to 100s of milliseconds at startup using external boot PROMs. This prevents the use of SRAM FPGAs in certain critical control logic sections of systems that must be "live" immediately upon the application of power. Lattice has

developed proprietary circuit design techniques that allow its non-volatile devices, such as our LatticeXP2 and MachXO, to become active virtually instantly after startup (~1-2 mS).

Design security is also a key advantage of our non-volatile FPGAs, in two distinct ways. First, our embedded Flash memory allows the entire user design to be stored in on-chip Flash memory, enabling a space saving single-chip solution. The configuration bitstream is never exposed, as it is when using SRAM FPGAs with boot PROMs. It is virtually impossible for a hacker to access the configuration data of a non-volatile FPGA.

Second, our embedded Flash memory allows us to support true AES encryption of the configuration bitstreams. It supports the storage of a user-programmable, on-chip 128-bit encryption key. Once this key is stored on-chip, the user can encrypt the configuration bitstream for a given design and transmit it to the FPGA (over unsecured transmission lines). Once on chip, the bitstream is decrypted using the stored AES key, and is never exposed off-chip.

There are other FPGAs that are called non-volatile, but they are not true single-chip, embedded Flash solutions. Instead, they combine two independent chips (a Flash memory and an SRAM-based FPGA) in a single package using a stacked die technology. Compared to true non-volatile FPGAs, these hybrid products have severe limitations.

Q. **How do the pros of "non-volatility" compare and contrast with the (renewed) interest in CPLDs?**

A. CPLDs such as our MachXO and ultra low-power ispMACH 4000ZE devices are by definition non-volatile, so they offer the same benefits of a single-chip solution, instant-on capabilities and design security.

Programmable logic users now require higher macrocell densities. However, CPLDs have not been economically feasible beyond ~512 MCs. To address this need, we developed our MachXO crossover family by combining these two complementary differentiators and extending our FPGA architecture to a very low-density range. We have been able to extend the logic density range for CPLDs to over 2,000 Logic Cells (roughly equivalent to ~1,200-1,500 macrocells) while substantially improving both cost and performance. As a result, CPLDs are now attractive design solutions for a variety of applications.

Q. **Finally, what sort of online resources can you point us to where one can learn more about Lattice? Are there particular webcasts, white papers, tutorials or other items online that a developer can investigate before having to make a commitment to Lattice? (Please give us the exact URLs, if available).**

A. Technology & Market Solutions:
http://www.latticesemi.com/solutions/index.cfm?source=topnav

Webcasts:

http://www.latticesemi.com/corporate/webcasts/index.cfm

Non-Volatile FPGAs:
http://www.latticesemi.com/products/fpga/xp2/index.cfm?source=topnav

Low Cost FPGAs: http://www.latticesemi.com/products/fpga/ecp2/index.cfm?source=topnav

High-End FPGAs:

http://www.latticesemi.com/products/fpga/sc/index.cfm?source=topnav

Ultra Low Power CPLDs:

http://www.latticesemi.com/products/cpldspld/ispmach4000ze.cfm?source=topnav

Intellectual Property:

http://www.latticesemi.com/products/intellectualproperty/index.cfm?source=topnav

Design Tools:
http://www.latticesemi.com/products/designsoftware/isplever/index.cfm?source=topnav

Q. **Thank you for this interview.**