

Microcontrollers & Obsolescence: The FPGA Solution

Product obsolescence will continue to occur in the transportation market but there are solutions readily available using FPGAs coupled with microcontroller IP. Kerry Howell says Lattice has a solution.

An End of Life, EOL, notice for a component in production is one of the worst that a manufacturer can receive! Several popular microcontroller and microprocessors have been designated EOL over the last few years, as semiconductor suppliers consolidate and prune their product portfolios. Historically, affected manufacturers have had two options: a last time buy or a product redesign. But last time purchases lock up working capital and for a redesign, a simple board layout change to support a different part is easy. However, choosing a new microcontroller family requires substantial software engineering time.

Software compatibility is the major hurdle in choosing a different microcontroller family. Most companies have a large investment in the implementation, testing and verification of their software, so changing to a new architecture typically requires a complex and costly software port. If the change is made in the middle of a production cycle, special care must be taken to make sure there are no incompatibilities between the hardware platforms.

Finding The Third Alternative

One engine control systems manufacturer recently found itself facing an EOL. The manufacturer's design team determined it would take multiple man years to port the existing 15 year old code to a new architecture and perform all functional testing.

Also, because the software teams were already working on other projects, additional resources would have to be hired to work on the conversion program. After evaluating the time and costs associated with the architecture changes, this manufacturer looked for a solution that would be code and functionally compatible with the existing system.

The 'third alternative' solution was based on a non-volatile FPGA such as the LatticeXP2, coupled with a third party Intellectual Property, IP, core that would be compatible with the existing microcontroller. Digital Core Design, DCD, a Lattice partner, had a microcontroller core similar to that requested by the manufacturer and it proposed modifying its existing core to

match the execution and peripheral set found on the obsolete device, as shown in Figure 1.

For the manufacturer, the new solution and the original system had to work identically. The external and internal timing, as well as processor functionality and even the same binary program had to run without modification.

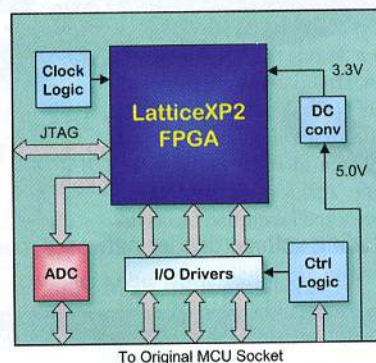
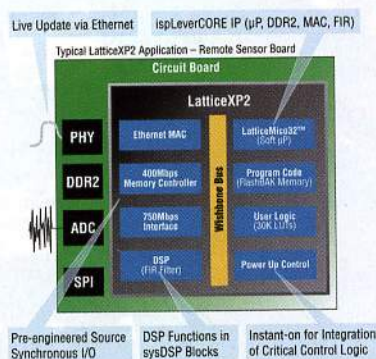
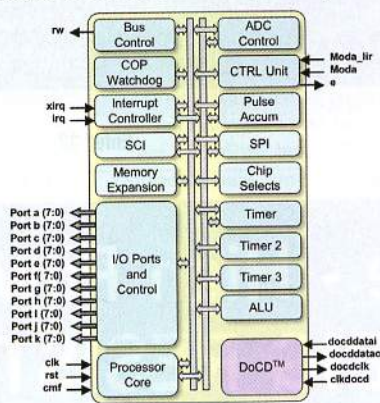
This compatibility requirement also included software timing loops embedded in the legacy processor code. On the hardware side, the solution had to fit in the same footprint as the original MCU and connect to the same interfaces. In addition, there was also a big requirement for high security against unauthorised configuration changes.

The System Solution

The non-volatile LatticeXP2 FPGA integrates SRAM and Flash memory in a single die. At power-on, the FPGA operating configuration is copied in a massively parallel fashion, from the Flash into the SRAM and this, as shown in Figure 2, allows the device to be initialised and ready to operate in less than 2ms.

The instantly on feature allows the non-volatile FPGA to easily replace the ASSP microcontroller

Top to bottom, figures 1, 2 and 3 respectively.



because the application doesn't have to wait while the FPGA configuration is loaded from an external memory.

The Flash based FPGA also includes several security features within its logic to prevent unauthorised read-back or modification of the internal memory configuration. This makes sure that there will be no unauthorised duplication or tampering with the internal Flash configuration.

With the replacement hardware identified, matching the software functionality of the original microcontroller was the final step. DCD fulfilled this need largely by using existing tested and verified peripheral cores from its own extensive library. There were a few peripherals that were new, however, and great care was taken to match the requirements of the original microcontroller.

Because digital FPGAs do not have on-board analog converters, the biggest challenge was that the original MCU included eight analog to digital converter channels. DCD met this challenge by writing IP that used the same software interface - control and data registers - to the internal bus and that could be connected with a variety of external serial and parallel ADCs. Then all that was required was to select an ADC with the same conversion timing and accuracy as the original MCU.

The final solution used by the manufacturer is the small mezzanine board shown in Figure 3. It contains the LatticeXP2 FPGA, the ADC device and a clock generator. A PLCC connection allows direct interfacing with the manufacturer's PCD and provides a pin for pin direct replacement for the original MCU. Having the boot memory on-chip reduces the board device count and allows for a smaller final solution.

Product obsolescence will continue to occur in the transportation market but there are solutions readily available using FPGAs coupled with microcontroller IP. The instant-on LatticeXP2 FPGA provides a secure and small footprint solution that also has the long life requirements needed in the transportation market. DCD microcontroller IP is a quick and cost-effective way to replace existing MCUs, while retaining exact software compatibility with the original design.

Having a pin compatible solution allowed the manufacturer's design team to focus its efforts on validating the IP core inside the FPGA, instead of performing a full hardware and software redesign and validation.

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