Modular AdvancedTCA FRU power management architecture

By Shyam Chandra

Managing payload power supplies by addressing such tasks as sequencing and supervision in an AdvancedTCA Field Replaceable Unit (FRU) is quite demanding. Traditional single function power management ICs cannot address the requirements, so designers offload some of the payload power management functions to the onboard Intelligent Platform Management Controller (IPMC) microcontroller. Here we will examine the AdvancedTCA compliant power distribution architecture and describe a modular approach to integrate payload power management with the platform management section.

An AdvancedTCA-compliant system consists of one or more subracks with multiple hot-swappable line cards. A line card compliant with the AdvancedTCA standard (an FRU) must implement a basic set of management functions for its power feed, cooling, and interconnection requirements, among others. The IPMC handles these management functions.

PICMG 3.0 specifies the implementation of a hierarchical management architecture in which a shelf manager communicates with the on-FRU IPMCs in that shelf through the Intelligent Platform Management Bus, or IPMB. When the FRU is plugged into the backplane, and before turning its payload on (payload refers to the application-specific function implemented in a FRU), the onboard IPMC sends the FRU card details to the shelf manager. The shelf manager then instructs the IPMC to turn the payload on. If a wrong card is plugged into the backplane, the shelf manager instructs the IPMC not to turn on the payload, protecting other FRUs in the shelf. All FRUs should implement the basic management architecture per the PICMG 3.0 specification in order to be AdvancedTCA-compliant.

Most FRUs have two connectors, Zone 1 and Zone 2. The Zone 1 connector provides the -48 V power supply for the FRU. The Zone 2 connector is used for inter-FRU payload communication. The Zone 1 connector also supplies the connection to the IPMB, which is based on the I2C bus specification.

The -48 V power supply from the backplane is used to generate the main payload power supply voltage (usually 12 V) through an isolated DC-DC converter. This 12 V supply bus is used to generate all payload-specific supply voltages on the circuit board. The 12 V supply is also used to power the IPMC through the management supply.

The PICMG 3.0 standard specifies the functionality of the hot swap controller

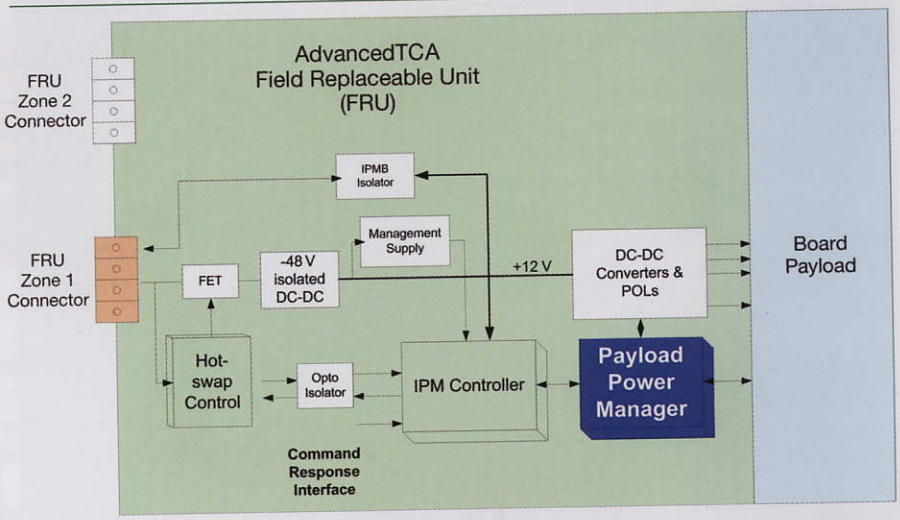

Figure 1

Figure 1 shows the four main blocks controlling the power distribution:

- Hot swap controller, FET, and isolated DC-DC converter
- Intelligent Platform Management Controller (IPMC) Management Supply
- Payload Power Management Controller and Payload DC-DC converter and Point Of Load supplies (POLs)
- Board payload

and the IPMC. However operation of the payload Power Management Controller or payload DC-DC converter depends on the actual payload circuitry, and these are not covered by the specification.

Hot swap controller

The -48 V from the Zone 1 connector powers an isolated DC-DC converter shown as "-48 V isolated DC-DC" through a series pass FET. The hot swap controller, which controls the series pass FET, limits the inrush current when the FRU is plugged into the shelf backplane. After the current inrush event, the hot swap controller turns the -48 V power feed on fully to the isolated DC-DC converter by turning the FET on. The isolated DC-DC converter generates 12 V and 3.3 V for the payload and for the management control circuitry, respectively. The AdvancedTCA standard specifies almost all functions of the hot swap controller.

Intelligent Platform Management Controller

The IPMC is a microcontroller used to control the power to the board payload and manage the board's interconnect needs and cooling requirements. When the FRU is plugged into the backplane, the IPMC first communicates with the shelf manager. Depending on the shelf manager's instructions, the IPMC controls the power feed to the payload through the payload Power Management Controller. Additionally, the shelf manager can also determine whether to reset the FRU main processor (CPU), using either Cold Reset or Warm Reset. The IPMC also measures various power supply voltages, currents, and temperature and logs them into a central repository, the Sensor Data Record (SDR). The communication protocol between the IPMC and the shelf manager (instruction handling, data structures, state machines, and SDR) is specified fully by the AdvancedTCA standard and is common to all the AdvancedTCA FRU implementations independent of the payload functionality.

Payload Power Management Controller and payload DC-DC converters

The number of power supply voltages generated in an FRU is determined by the payload circuitry. These payload power supplies should be turned on/off in a sequence determined by the payload ICs. To ensure reliable operation, all payload power supply voltages and currents should be monitored for faults. In the case of a fault, a supervisory signal should alert the onboard CPU and have the IPMC record supply faults. In extreme cases, the supply for the payload should be shut off to prevent damage to the board.

The functions of the payload Power Management Controller are:

- Manage onboard DC-DC controllers – soft start, sequencing, tracking, margining, trimming, and the like
- Generate all power supply relevant status and control logic signals – reset signal generation, supply over-voltage/under-voltage and over-current fault indication (supervision), and voltage/current measurement
- Control the main supply power feed for the AdvancedTCA payload and, for AMCs individually, short circuit protection and power feed to the AMCs

Typical Payload Power Management Controller implementation

On average, AdvancedTCA FRUs have 6 to 10 power supply rails. The power management functions can be quite complex and often require a PLD or a microcontroller, in addition to common single-function power management ICs, such as supervisors, reset generators, and hot swap controllers.

Figure 2 shows the power management controller with the main payload power supply (+12 V) shown on the top left.

The payload Power Feed Control block turns the payload power supply on to the payload circuitry when instructed by the IPMC and controls the power feed to the AMCs. Usually this block is implemented using a number of hot swap controller ICs.

After the 12 V bus is turned on, all payload DC-DC converters should be turned on in a manner that meets the sequencing or tracking requirements of the payload circuitry. Because these requirements vary during the board debug process, the sequencing algorithm is usually implemented in the IPMC microcontroller or in a PLD, which enables easy alteration to the sequencing algorithm.

After the board is turned on fully, the power supply voltages are monitored for faults. When a power supply fault occurs, the main processor is interrupted to safely terminate its current process before the entire board is shut down. This power-fail alert is also sent to the IPMC for the shelf manager updates. If the supply failure is severe, the IPMC may decide to shut down payload power supplies.

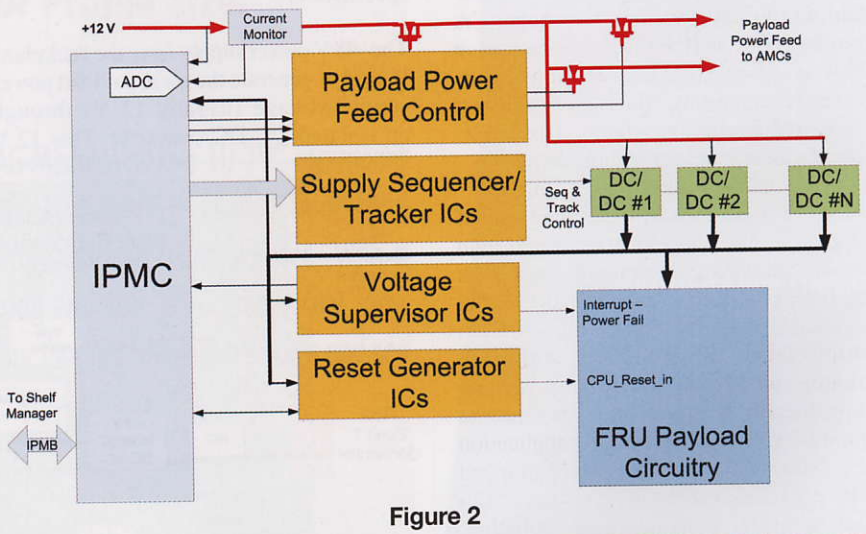

Figure 2

Some of the IPMC commands require multiple actions performed in a sequence. For example, executing the "Turn the Payload Power on" instruction requires the following functions:

1. Turn on the Payload Power (+12 V) feed MOSFET.
2. Once the payload voltage reaches its operating threshold, turn on individual DC-DC converters, following the required power supply sequencing rules for that FRU. If any power supply develops a fault during turn on, immediately turn off all supplies and inform IPMC of the failure.
3. After all the payload power supplies are turned on, generate a Cold Reset signal. Sometimes this signal requires pulse stretching of about 100 ms after the supplies are turned on.
4. Send a "Success" status response back to IPMC.

The purpose of the reset generator is to generate a CPU reset after all the power supplies are turned on. The IPMC may also be required to reset the CPU when instructed by the shelf manager.

The main purpose of the IPMC is to perform the PICMG 3.0-specified platform management functions. To be compliant, the IPMC should implement elaborate protocols, state machines, and decoding of predefined instructions. The on-chip ADC is used to measure all the power supplies and currents on the board and log them in Sensor Data Records (SDRs).

Often, designers use the software flexibility provided by the IPMC microcontroller to perform payload-specific power management functions such as payload power sequencing. Or designers could task the IPMC with initiating shutdown when a supply fails or when there is an over-current fault. In some cases, the microcontroller is also burdened with trimming power supplies through DACs.

The software on the IPMC should be tested thoroughly to ensure that the board is compliant. Once the IPMC software is certified, any modifications to the software will require a complete retest to ensure compliance.

Adding the payload power management functions to the IPMC makes the design FRU-specific. Each FRU design should be tested separately for IPMC compliance. This time-consuming chore involves repeated testing against standards. Further, the power management algorithm may have to be changed to meet the requirements of a new version of an onboard ASIC, that results in an IPMC software change and a retest for compliance.

Monitoring for faults in software creates additional overhead and may slow the microcontroller's response to communication protocol. This application also requires a microcontroller equipped with an on-chip multichannel high accuracy ADC with analog multiplexing. Depending on the payload, the increased code length due to Payload Power Management (PPM) may demand a more expensive microcontroller with increased memory resources.

Modularity has its advantages

Following is a description of a modular FRU payload power management section, with the platform management (IPMC) and the PPM separated. This method uses as an example Lattice Semiconductor's programmable Power Manager IC (Power1220) to implement the PPM.

The proposed solution (Figure 3, next page) is a modification of the power management control shown in Figure 2. In this solution, the IPMC performs only the platform management functions and directs the Power1220 IC to perform all of the PPM functions. Figure 3 shows the IPMC (implemented in a microcontroller). Figure 3 also shows the programmable PPM Controller (implemented in the Power1220 IC) and FRU payload circuitry, DC-DC converters, and MOSFETs.

The microcontroller implements only the PICMG 3.0-specified Intelligent Platform Management functions. All real time payload power management functions, such as controlling payload power feed, power sequencing, voltage and current monitoring, and generating cold and warm reset to the payload, are performed by the block FRU Payload Power Manager Power1220 IC. The IPMC simply sends commands to the PPM using the I2C bus. Some of the proposed standard commands are "Turn Payload Power on," "Turn Payload Power off," "Generate Cold Reset," "Generate Warm Reset," "Margin supplies Up/ Down," and "Turn AMC Power Payload power on/off."

The PPM interrupts the IPMC when it detects any power supply faults. The IPMC builds the SDR by using the Analog to Digital Converter (ADC) built into the payload Power Manager IC.

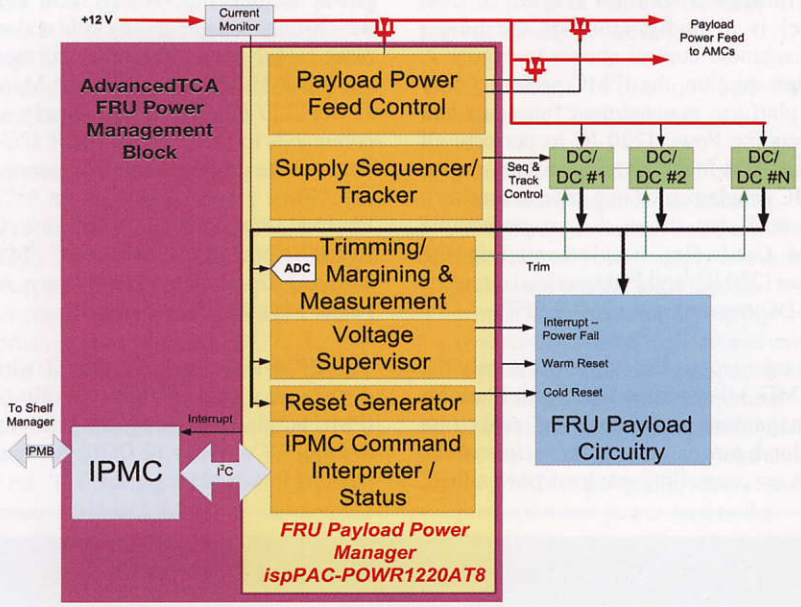

Figure 3

The IPMC platform management software, including the PPM commands, is tested once to ensure conformance with the PICMG 3.0 standards. The design is then typically used across all FRU designs. The FRU-specific payload power management is now handled by a simpler programmable IC such as the Power1220.

AdvancedTCA FRU-specific Payload Power Management

The Power1220 IC (PPM) uses its on-chip 48-macrocell CPLD to implement the functions of the sub-blocks, shown by the block "FRU Payload Power Manager Power1220." The payload power feed sub-block directly controls the MOSFETs to turn the payload power rail on/off. Typical power dissipation of AdvancedTCA board payloads is 100 W or more. To meet this power demand, the 12 V bus should be capable of supplying more than 8 A. In order to turn on such high currents, the PPM has to make sure that the MOSFET operates within its safe operating area – a function performed by multiple hot swap controller ICs.

The supply sequencer and tracker function, implemented in the on-chip PLD, controls the turn on/off sequence of all payload DC-DC Converters. Frequent changes to the sequencing algorithm during the debugging phase can be addressed simply by altering the state machine code.

The IPMC can measure all power supply voltages and currents using the on-chip 10-bit ADC through the I2C bus. The Power1220 has multiple digital feedback control loops and DACs on-chip to support trimming and margining of up to 8 DC-DC converters.

The power supply under- and over-voltage faults on up to 12 rails are monitored using 24 on-chip programmable threshold precision (Typ. 0.2 percent) comparators. This feature integrates the function of many

supervisor ICs. Because the threshold of each of the comparators is programmable, it can be used to monitor various supply rails without using external potential dividers. The reset generator also uses the same programmable threshold comparators to generate the CPU reset signal. One of the on-chip timers provides the reset pulse stretching function.

The Command Interpreter block of the PPM is used to translate standard commands from the IPMC into multiple control signals for each of the five main blocks within the PPM.

The Power1220 provides a 48-macrocell CPLD, 12 analog inputs with 24 programmable threshold comparators, 6 digital inputs, 20 outputs (including 4 charge pumped MOSFET drivers), 8 DACs with 8 digital closed loop control blocks, and 4 programmable timers on-chip to implement all functions of the PPM shown in Figure 3.

Reduced time to market

With the modular approach, designers can focus on getting the IPMC software tested for compliance once and then use it across all their FRU designs, as opposed to performing compliance testing for each FRU. Frequent changes to the Power Management algorithm are addressed by modifications to the state machine algorithm in the PPM, instead of changes to the IPMC software. This means that retesting against IPMC compliance is not required, which reduces time to market.

Adapting quickly

The IPMC software can be modified to accommodate evolving standards or enable the FRU to interface with different shelf managers. In such cases, the board testing for payload power management need not be performed, reducing the time required to address operating environment changes.

Reduced cost

The modular design uses the on-chip ADC of the Power Management IC, eliminating the need for a microcontroller with an on-chip ADC. This also enables the use of lower cost microcontrollers with smaller on-chip memory.

The cost of the PPM section also shrinks because a Power1220 device cost effectively integrates many hot swap controller ICs, supervisor ICs, reset generator ICs, and a CPLD, saving board space. Further, the cost of the DC-DC converters can also be reduced by using the trim and margin feature provided by the Power1220 IC.

Increased software and hardware reliability

The modular approach separates the standards-related software from the board-specific power management algorithm and enables independent modifications to each section. Test coverage is increased, resulting in improved software reliability. The Power1220 integrates multiple ICs, leading to improved hardware reliability. Because the Power1220 enables improved monitoring coverage of all supply rails, overall functional reliability also increases.

The proposed modular approach with IPMC and programmable payload power management solution using the Lattice Power1220 IC increases flexibility and fault coverage. The same microcontroller (with fixed software) and the Power1220 IC can be used to implement complete platform management and meet vastly different PPM requirements across FRUs.

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