Designing low cost FPGAs into femtocells for home

It looks likely that femtocells will be deployed in every home which means there will be pressure to minimise cost, and designers are looking at FPGAs as the solution, say **Van Macomb and Ron Warner**

Access point basestations or femtocells, designed for home and indeed office use are seen by the network operators as a way for increasing the overall coverage of future wireless networks. This is particularly important as the demand for increased data rates both in the uplink and downlink paths continues to increase.

Femtocells are small form factor basestations designed to fit into a home or office environment and support a handful of subscribers. A variety of deployment scenarios, encompassing rural settings as well as suburban and city dwellings are envisioned.

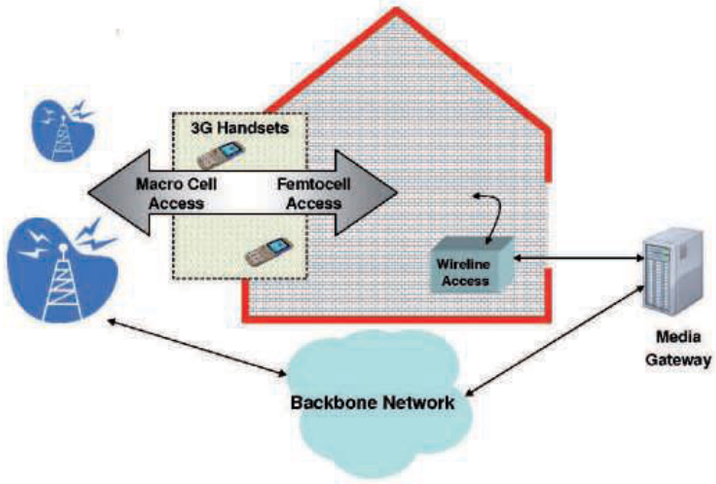
Figure 1 shows how a typical network could be configured.

Some believe that femtocells are poised to become the ultimate delivery vehicle for wireless infrastructure expansion because:

Wireless network capacity is expanded on a local as-needed basis

The backhaul bottleneck is bypassed as consumers link their femtocells to their own wired connection.

Most importantly CAPEX costs are shifted to the consumer



Using this simplified definition, it is clear that a femtocell basestation must support the same high level, functional features as traditional basestations.

The home environment simplifies some of the requirements of a femtocells, this opens several options at the device level.

First, a femtocell is intended only to support a handful of users, which greatly reduces the overall system processing requirements. Second, femtocells need only support mobility as it applies to people walking about their homes not in cars or trains. This greatly simplifies the search algorithms needed to support them.

These two major differences make it possible to implement a Femtocells basestation using just a handful of chips (Figure 2 on page 13).

Some of the problems associated with the home are - firstly what are the various backhaul technologies that consumers will plug into (FTTx, Ethernet, ATM, DSL, etc.), and how does that impact the femtocell design?

Second, what are the air interface standards that need to be supported? Although most of the discussion here is focused on WCDMA/HSPA and CDMA/EV-DO, the massive footprint of deployed GSM technology requires a look at supporting this standard as well. And if WiMAX and WiFi femtocell designs gain traction, should these also be supported?

At the same time, some of the complexities associated with having a base station in the home, such as security, access control, interference with the macro cell, handouts and handins have yet to be resolved. All of these variables again underscore the need for flexibility in architecting femtocells.

With the anticipation deployment of femtocells in every home comes the inevitable pressure to minimize cost.

Price targets for a complete femtocell in the range of $100 to $200 are being discussed. These price points are well below the cost of today's full featured, flagship FPGAs.

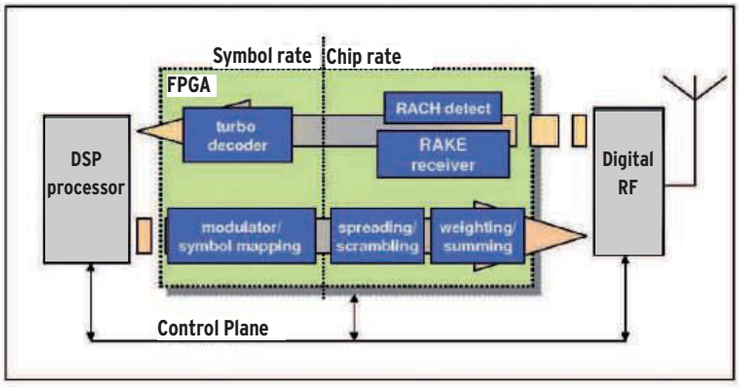
Fortunately, this relatively new base station architecture is emerging at a time when low cost FPGA architectures have rapidly grown in popularity, to the point that they now represent approximately 25 per cent of the overall market. FPGA vendors ➜

Designing low cost FPGAs into femtocells

have developed low cost FPGA fabrics with embedded features such as DSP blocks, embedded memory and even high-speed serialiser/deserialiser (serdes) devices that support the performance requirements of wireless Baseband processing at a fraction of the cost of full featured, high-end FPGAs.

FPGAs and DSPs have been co-processing partners in wireless applications for many years. With the advent of low cost, feature rich FPGAs and processors specifically developed for wireless applications, this symbiotic relationship remains viable for anticipated high volume femtocell applications. These scaled down processors offer the functionality needed to support the reduced requirements of a smaller basestation and are significantly less expensive than their highly integrated counterparts.

For example, baseband chip rate processing can be partitioned such that a Rake Receiver, RACH detector, spreading, scrambling and channel weighting/summing functions are all offloaded from the processor to a hardware implementation.



A femtocell architecture.

Additionally, symbol rate processing functions such as a turbo decoding, modulation and symbol mapping also are viable candidates for hardware acceleration.

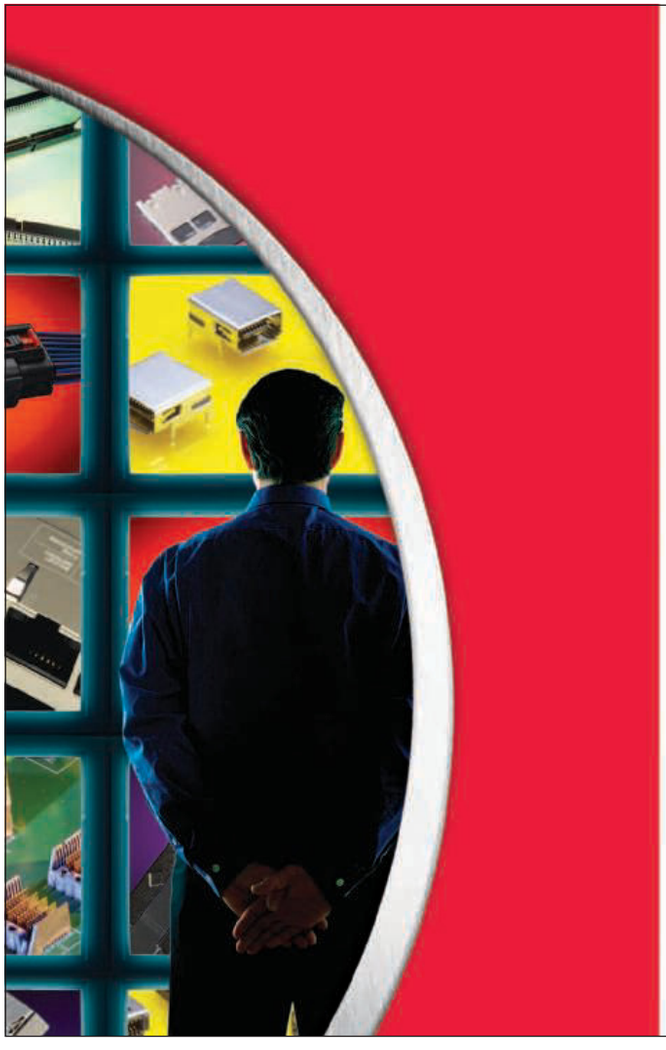
FPGAs make a hardware-based design approach such as this attainable in a single, highly integrated, low cost device. This is made possible by providing traditional, high-end, feature rich functionality such as embedded DSPs, memory blocks and high-speed serial interfaces, at price points that allow system designers to keep pace with the aggressive pricing in the femtocell market.

Most importantly, operators have stated that the femtocell must meet certain cost targets to be successful. Low cost FPGAs are now available that provide the necessary serdes, programmable logic and DSP functionality to support femtocell implementations at price points that were previously unachievable with high end FPGAs or ASSP/FPGA combinations.

These FPGAs combine programmable logic with embedded features such as DSP blocks, embedded memory and serdes. In conjunction with specialised processors, these new low cost devices are an attractive solution for femtocell implementations.

Wireless equipment vendors have relied on FPGAs to implement multiple functions as technology has evolved. Femtocells represent another step in this evolution. These advantages include rapid time to market, the ability to accommodate changes in the specification without modifying hardware, the flexibility to implement differentiating features and integrating multiple functionality onto one chip: all at cost points that still support high volume, low cost deployment.

Van Macomb and Ron Warner work for Lattice Semiconductor



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