Power consumption reduction for portable FPGA designs

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A critical design factor is reducing power consumption, particularly for hand-held devices and similar products. Power-aware design techniques along with estimation methodology help designers meet the operating specifications of targeted FPGA devices.

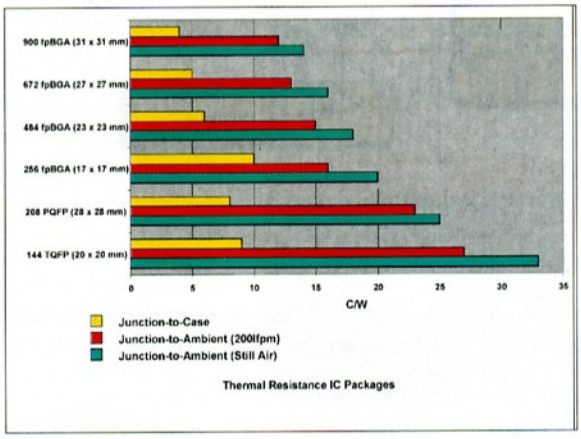

Figure 1. Thermal resistance (qJA and qJC) characteristics across a range of IC packages

■ Power management is an important consideration for FPGA designers, especially for those designs that target portable, battery-powered products. Designers are now expected to develop lower-power designs, produce better power estimates earlier in the design flow, and manage and sequence a variety of core and I/O voltages that often accompany FPGA implementations. The use of power-aware design techniques can help reduce power consumption, increase the reliability and lower the cost of production with leaner power supplies and fewer cooling requirements. Wasted power in a device manifests itself as heat, so understanding FPGA thermodynamics will help the designer identify high-impact, low-effort methods to reduce this. Total power is a function of certain types of sub-power producers along with the characteristics of the process node and device packaging.

The AC portion of the power consumption, associated with used resources, is the dynamic part of power consumption. AC power dissipation is directly proportional to the frequency and activity at which the resource is running and the number of resource units used. Power consumption can be influenced by lowering supply voltage (the largest factor), switched capacitance, switching activity of nodes, or frequency of signal transitions. CMOS FPGAs contribute to power dissipation from two primary sources: static and dynamic. Power is expressed as joules/second or watts given the equations:

$$P_{Static} = VI = \frac{V^2}{R}$$

$$P_{Dynamic} = \frac{1}{2}\beta C V_{DD}^2 F$$

Where:

β= switching activity per node, C= switched capacitance, F = frequency (switched events per second)

The relative contribution of P_{Static} versus $P_{Dynamic}$ varies by process node. Static consumption represents a fraction of the total power dissipation in 130 nm and 90 nm devices. Most energy is consumed due to dynamic switching activity and by charge/discharge of load capacitances, which is largely a function of the user design. This convention changes at 65nm process nodes and smaller. AC power dissipation is directly proportional to the frequency and activity at which the resource is running and the number of resource units used. The $P_{Dynamic}$ equation illustrates how power consumption is influenced by supply voltage (the largest factor), switched capacitance, switching activity of nodes and frequency of signal transitions. At smaller geometries the physics of transistors change such that static leakage is much more significant. The crossover point where static power overtakes dynamic power is 65 nm. Lattice Semiconductor and other FPGA suppliers address these issues largely in their respective fabrication processes and with the transistor mix used with each device.

As FPGA technology process geometry shrinks, designers naturally benefit from the reduced power consumption of smaller transistors and IC dies. However, this benefit is usually offset to some degree by increased clock speeds and larger designs. The relative contribution of the FPGA architectural element also changes between process nodes. While overall power consumption may drop in a 90nm device, the relative amount represented by I/Os increases significantly. This will influence what the power reduction strategy will be for a particular device family.

Heat, the by-product of work performed by an IC, must be addressed with techniques to ensure an FPGA will operate within the junction temperature specification. Thermal management is indispensable when using the IC for high power applications or using it under a high operating temperature. To avoid reliability issues, semiconductor vendors specify a maximum allowable junction temperature in device data sheets. Designers should always

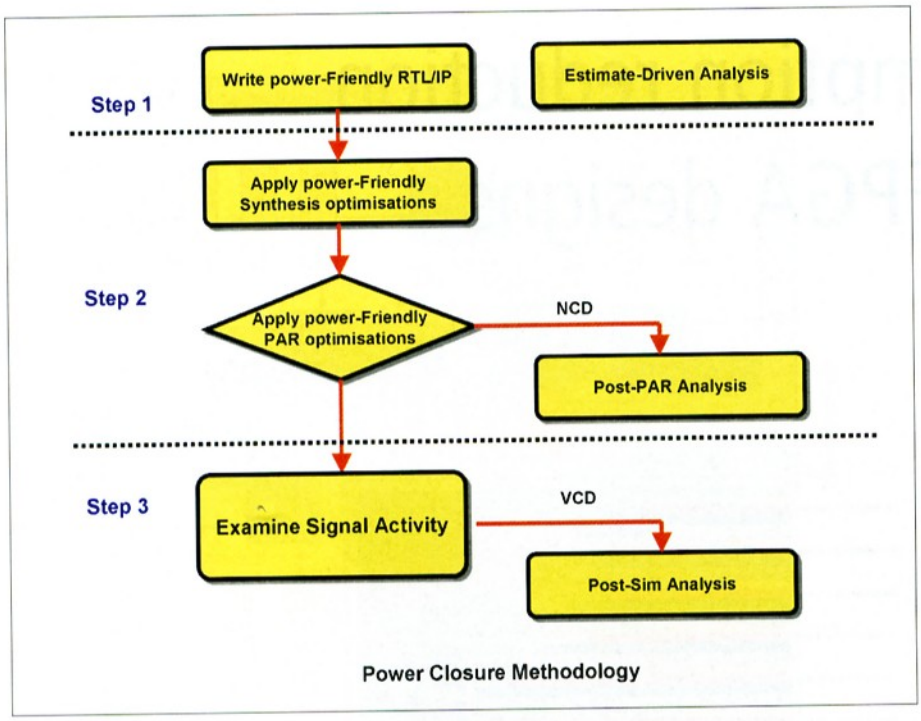

Figure 2. The three different steps of power-closure methodology

complete a thermal analysis of their specific design to ensure that the device and package do not exceed this specification. Factors such as die size, paddle size, airflow, power applied, PCB design and the application itself all contribute to the equation.

Although total power, ambient temperature, thermal resistance and airflow all contribute to device thermodynamics, the junction temperature (Tj) is the key to device operation. For example, the allowed junction temperature range for the LatticeECP2/M with a variety of architectural blocks including DSP, memory and SERDES I/O, is 0°C to 85°C for commercial devices and -40°C to 100°C for industrial devices. AC characteristics are guaranteed when the device is operated in these ranges. The reliability limit of junction temperature for this generation of device technology is 125°C. Awareness of the Min/Max numbers for supply voltages may help the designer reduce static power.

The concept of thermal resistance is used when considering heat dissipation. In an IC, thermal resistance (θ) indicates the steady state temperature rise of the die junction above a given reference for each watt of power (heat) dissipated at the die surface. Its units are oC/W. The most common examples are θ_{JA}, Thermal Resistance Junction-to-Ambient (in °C/W) and θ_{JC}, Thermal Resistance Junction-to-Case (also in °C/W). Another factor is θ_{JB}, Thermal Resistance Junction-to-Board (in °C/W). In addition to the device and package, the thermal characteristics of a circuit depend on the operating temperature, device power consumption and the ability of the system to dissipate heat. The maximum junction temperature of a device can be calculated as shown:

$$T_J = T_A + P * \theta_{JA}$$

$$T_J = T_C + P * \theta_{JC}$$

$$T_J = T_B + P * \theta_{JB}$$

where T_J, T_A, T_C, and T_B are the junction, ambient, case (or package) and board temperatures (in °C) respectively. P is the total power dissipation of the device. θ_{JA} is commonly used with natural and forced convection air-cooled systems. θ_{JC} is useful when the package has a high conductivity case mounted directly to a PCB or heat sink. θ_{JB} applies when the board temperature adjacent to the package is known. For the power (P=Vcc * Icc) factor, I_{CC} may be estimated from the power consumption section of individual device data sheets or as an output of power estimation software. Figure 1 illustrates thermal resistance (θ_{JA} and θ_{JC}) characteristics across a range of IC packages and demonstrates the benefits of certain package types and airflow versus a still air environment. When beginning a system design, engineers must make sure devices will operate at specified temperatures within the system environment. With FPGA power estimation tools, the designer can predict device thermodynamics and estimate the dynamic power budget. The ability to estimate a device operating temperature prior to board design also allows the designer to better plan for power budgeting and airflow.

Given a target application where the designer must account for power consumption, a power-closure methodology (figure 2) should be adopted. In the first step the designer should look for opportunities to create power-friendly RTL. High-impact, low-effort practices include targeting embedded blocks, gray encoding of smaller FSMs and organising blocks in a manner such that area optimisation will not overly impact performance. If the FPGA is a higher-density, 90nm device, I/O programming and switching should be given extra scrutiny to save power. Next, power-friendly synthesis and place and route optimisations such as register retiming and area optimisation should be applied. Finally, a robust test bench that reflects actual operating conditions will help build an accurate activity-factor and toggle-rate factors for post-simulation analysis with the power estimation software.

There are several design techniques that can help reduce overall system power consumption. The first are static power reduction methods. Use sleep mode if available because during sleep mode the standby current is reduced by over 1000X. Power supplies do not have to be switched if they are in their operating range. Reduce operating voltage and use VCC & VCCJ at the lower end of the device specification.

Minimise the operating temperature using the following methods. Use packages with lower thermal impedance that can dissipate heat better, place heat sinks and thermal planes around the device on the PCB and use airflow techniques such as mechanical guides and fans. Reduce switched capacitance and frequency of I/Os. Decouple I/Os when in sleep mode, if this is not possible, power down the core and leave the VCCO applied. Reduce I/O voltage swing and keep I/O drive as low as possible. For example, if driving 3.3V CMOS, try using 2.5V-3.0V VCCO. This can degrade noise immunity, but can help power. Use lower voltage standards with I/Os. Use slew rate controls to reduce output-switching current. Some FPGAs provide control over the LVCMOS or LVTTL output buffer that can be configured for either low noise or high-speed performance.

Dynamic (AC) reduction methods can be performed as follows. Enable synthesis area optimisation. Reduce the span of the design across the device. A more closely placed design utilizes fewer routing resources for less power consumption. Target embedded ASIC blocks for example the EBR, DSP and PCS blocks of modern FPGAs will have lower consumption over generic LUT/register logic. Use signal-encoding optimisation of counter/FSM modules. For example, a 16-bit binary counter has, on average, only 12% activity factor and a 7-bit binary counter has an average of 28% activity factor. On the other hand, a 7-bit linear feedback shift register (LFSR) can toggle as much as 50% activity factor, which causes higher power con-

sumption. A Gray code counter, where only one bit changes at each clock edge, will use the least amount of power, as the activity factor is less than 10%. Use optimum clock frequency; determine if a portion of the design can be clocked at a lower rate, which will reduce power. Use clock-gating optimization. As clock signals are a major contributor to power dissipation because they switch at all times, clock gating can help reduce excessive switching in synchronous registers. Gate clocks prior to primary/secondary route resources of the FPGA. Use time division multiplexing (TDM) type arithmetic and synchronous versus asynchronous counter implementations.

Like simulation, FPGA thermal analysis is a verification flow that runs parallel to traditional FPGA implementation tools. For example, in the ispLEVER design tools flow for Lattice FPGAs, designers can estimate power consumption at any stage: pre-synthesis, post-route and post-simulation with the power calculator application. FPGA power estimation software tools typically allow designers to estimate power consumption at three different levels of accuracy. 1. Estimate-driven, where utilised resources and toggle activity are manually entered, 2. Post-PAR (place and route), where post place and route resources are imported for a more accurate utilisation model, and 3. Post-simulation, where toggle activity produced by an HDL simulator is imported for a more accurate activity factor and toggle rate model.

The power calculator uses input parameters such as device characteristics, voltage, temperature, device variations, airflow, heat sink, resource utilization, activity and frequency to calculate the device power consumption. The calculator reports both static (DC) and dynamic (AC) portions of the power consumption and the predicted junction temperature (TJ). Pre-synthesis, switching activity is estimated with the activity factors of logic blocks and the toggle rates of I/Os. If the power calculator is used after place and route, the actual device utilization can be imported through the native circuit description (NCD) database. Power calculation is most accurate when the system uses the post-map, post-place or post-route NCD results. An optional value change dump (VCD) file containing activity factors and toggle rates based on simulation results will further increase accuracy. ■

Product News

■ Intersil: multiple output controllers for POL applications

Intersil has introduced a pair of multiple-output standard buck ICs that integrate critical power management functions to lower the number of components and save valuable board space. The triple and dual output regulators provide a single, high-efficiency power solution for a variety of point-of-load applications. The ISL8501 and ISL8510 feature a 5V fixed input voltage capability and variable input voltage ranges up to 25V. These flexible voltage ranges make these devices ideal for a wide range of point-of-load applications such as 5V FPGA/CPLD and DSP power supplies, 12V telecom/datacom power supplies and 24V battery-powered handheld applications.

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■ IR: integrated DC-DC regulator family for space constrained applications

International Rectifier, has introduced the SupIRBuck family of wide input, single output synchronous buck voltage regulators for high density, high performance data center and consumer applications. The IR38xx SupIRBuck family of point-of-load voltage regulators integrates IR's HEXFET trench technology MOSFETs and a synchronous buck control IC in a compact 5mm by 6mm Power QFN package, shrinking the silicon footprint.

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