

Enabling Next-Generation Wireless-Base-Station Connectivity



By Ron Warner and Sid Mohanty, Lattice Semiconductor

As the demand for connectivity increases, so too does the pressure on wireless providers to deliver affordable services, yet remain profitable. A key factor affecting profitability for the service provider is the cost of the network. With infrastructure evolving to support an ever-expanding subscriber base, it becomes increasingly important for the service providers to keep their network costs in check while maintaining - and often improving - their service statistics.

The Open Base Station Architecture Initiative (OBSAI) was established by wireless OEMs - including LG, Nokia, and Samsung - to develop a set of specifications for the configuration and interconnect of BTSs (base transceiver stations) from a set of common modules (see Figure 1). The standardisation of the interfaces results in more fierce competition among silicon and solutions providers, which reduces the overall cost for equipment vendors and shortens time-to-market.

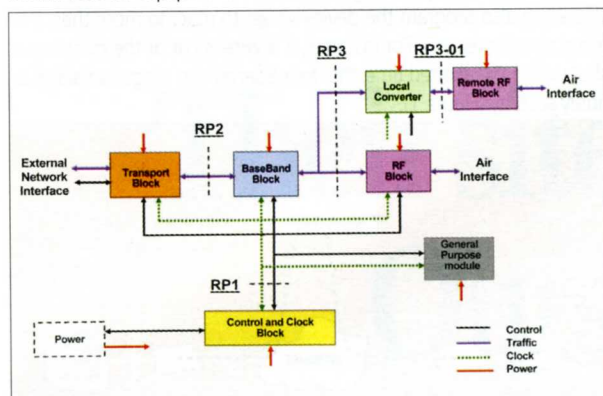


Figure 1: The OBSAI BTS architecture.

Internal interfaces between BTS functional blocks are designated as reference point 1 (RP1), reference point 2 (RP2) and reference point 3 (RP3). The RP1 specification includes control data and clock signals to all blocks. The RP2 specification specifies the user-data packets between the transport block and the baseband block, and the RP3 provides the specification for the user interface and signaling data between baseband block and RF block.

The importance of the RP3 interface has increased with the advent of distributed base-station architectures and remote radio heads. These new networking topologies employ a single baseband block to

control multiple RF blocks, both in point-to-point configurations as well as networked topologies. Figure 2 is an example of the architecture of a BTS with remote RF units (RRUs). To address these new configurations, the RP3-01 protocol specification, an extension to the RP3 protocol specification of the OBSAI family of specifications, was defined. It specifies support for several RRU topologies, including the aforementioned point-to-point connection between a BTS and an RRU, as well as chain, tree-and-branch and ring topologies. In addition to supporting data transfers to multiple RRUs, the RP3-01 extension also provides the capability to map RP1 control messages into the RP3 baseband link. This capability is critical in these newer configurations in order to minimise the number of connections needed for both data and control-message distribution.

⇒ Low-cost FPGAs implementing OBSAI

FPGA devices can play a key role in enabling the next generation of wireless equipment. As wireless protocols evolve and as requirements change, FPGAs provide a quick and flexible platform that allows faster time-to-market. These devices with SERDES allow for the easy implementation of multi-rate protocols, since the updated physical rates and the protocol logic required can be provided to the customer as a soft FPGA IP update. Constant infrastructure upgrades are part and parcel of the wireless-infrastructure market. Given their flexibility, FPGAs have always been popular for wireless implementation. However, their higher costs have made them less than optimal for cost-sensitive wireless designs. Until recently, equipment vendors that wanted to use FPGAs for wireless implementations had to select expensive high-end products because these were the only devices that offered the embedded SERDES needed to support the physical-layer requirements of the OBSAI specification. The net result was a higher total cost of implementation for the manufacturer. Consequently, these costly FPGA implementations were used only for prototyping; typically, the equipment vendor converted to an ASIC-based design for high-volume production. The recent introduction of low-cost FPGAs with embedded SERDES provides equipment designers with the flexibility that accelerates time-to-market and cost

on their implementation requirements. An FPGA implementation with the OBSAI solution, divided into hard and soft IP as well as user-specific logic, is shown in Figure 3.

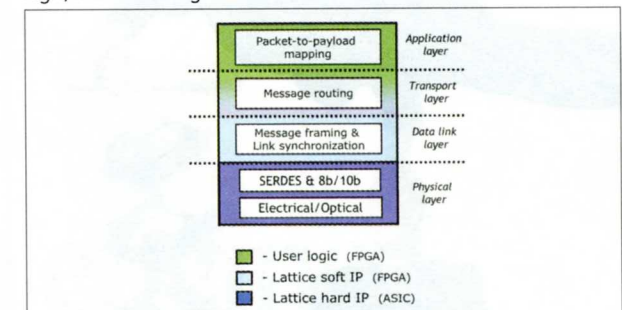


Figure 3: Partitioning of a OBSAI protocol stack.

⇒ Advantages of programmability

ASICs and ASSPs have always been popular for implementing complex functions at reasonable costs. However, the changing telecom marketplace has put a squeeze on equipment vendors and their ability to dedicate time and resources to develop ASIC solutions. ASSP vendors have also been hit hard during the most recent industry downturn, leaving fewer viable players in the marketplace. Also, open-industry specifications like CPRI and OBSAI have created a level playing field, since equipment designers can choose solutions from among a number of different sources. A key differentiator is in the flexibility of the available solution. FPGAs offer designers this flexibility, while also providing an upgrade path as industry specifications change or requirements are updated. For applications that involve emerging specifications, or where custom logic is desired, programmability is both a key advantage and a necessity for the designer. Programmability offers system designers the luxury to incorporate vendor-specific logic in the application layer, and at the same time provides the flexibility to provide multi-rate as well as newer standards as they evolve (or as existing standards are extended). The embedded hard-IP portion of the LatticeECP2M device

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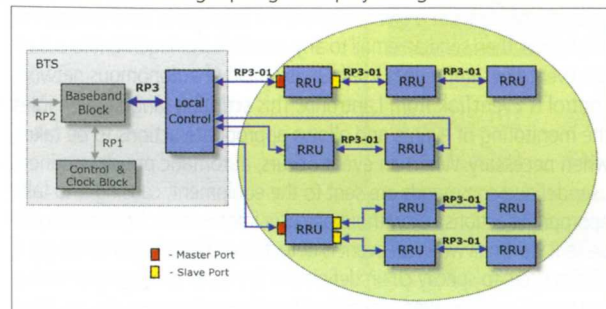


Figure 2: An example of the RP3-01 architecture.

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The ECP2M SERDES-based FPGA supports the physical-link layer, the data-link layer and the transport layer of the OBSAI-RP3-01 specification. It also can handle the three standard bit rates of the OBSAI specification (768, 1536, and 3072 Mbit/s). Control and status parameters specifying core functionality are managed via bit-mapped I/O that may be hard-wired or interfaced to programmable registers. This provides users with optimal flexibility in defining static and/or dynamic management of the various functional parameters needed for their particular applications. A GUI-selectable option generates configurations based

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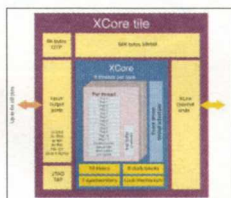
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Software Defined Silicon

flexibility and performance merged together

Bristol-based start-up XMOS Semiconductor has received test chips for its first generation of Software Defined Silicon (SDS) products, a new class of programmable semiconductor that it hopes will merge the advantages of programmable logic with those of standard cell. The devices have been produced by TSMC on its 90nm G process. Central to the technology is a compact, event-driven, multi-threaded processor called XCore. With up to 500MIPS to share across up to 8 threads, the processor core's engine can implement a range of complex hardware functions. Access to its computational and control capabilities is through a simple-to-follow embedded-software design flow. By using C-based behavioural languages, designers will be able to map white-board functional specifications into silicon. The processor is coupled to the outside world through a set of event-driven input-output ports, and inter-thread communication is provided by XLink, a channel mechanism that allows threads and cores to interact at the hardware level. The company believes that its solution will offer OEMs the means to realise their system designs without being tied down by the volume, time-to-market, and initial expense issues inherent in ASIC designs and without the power-consumption and performance limitations of an FPGA. Engineering samples are expected to be available by summer 2008.

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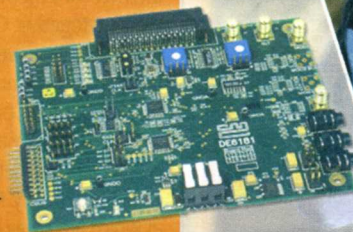
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