

Improve PC-Board Reliability by Adding Power Analysis to the FPGA Design Flow

Advances in FPGA analysis software make it an effective tool for modeling and managing power consumption.

Traditionally, field-programmable-gate-array (FPGA) designers have been concerned with timing and area efficiency. Now that FPGAs are more often replacing application-specific standard products (ASSPs) and application-specific integrated circuits (ASICs), however, designers are expected to develop lower-power designs and produce more accurate power estimates. Advances in FPGA analysis software provide an accurate and flexible means to model power consumption in a variety of operating environments.

Power analysis—like functional and timing verification—has emerged as a parallel verification track to the design flow (see Figure 1). Early power analysis may rely on simple utilization and signal-activity estimates provided by the designer in “what-if?” scenarios. Later, post-layout device information and signal activity recorded by gate-level simulation will become available. At that point, power estimates become far more accurate.

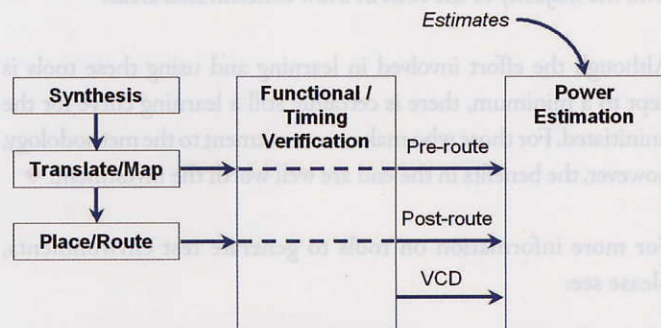


Figure 1: Power estimation parallels the traditional verification flow.

FPGA power calculators estimate device power consumption. They also enable the designer to import placed and routed designs and to specify parameters like voltage, temperature, process variations, air flow, heatsink and resource utilization, and activity and frequency. These parameters are applied to develop as accurate a model as possible within a variety of design environments.

BASIC POWER CALCULATION

Most FPGA power-analysis tools report both the dynamic (AC) and static (DC) portion of power dissipation. Static current is comprised of the leakage current through the device. Static

current/power is based on the temperature, process and voltage parameters, and conditions for the device. It is highly dependent upon temperature, which has a circular dependence upon the thermal characteristics of the device-board combination. Static power also is the leakage through all of the power supplies.

The dynamic portion of power consumption is the power consumed by the used resources while they're switching. The dynamic portion's power dissipation is directly proportional to the frequency at which the resource is running as well as the number of resource units used.

DC power is derived from the following equation:

$$\text{Total DC power (device)} = A e^{BT}$$

where:

A is the process-dependent parameter.

B is the temperature-dependent coefficient.

T is the junction temperature of the device.

AC power is derived from the following equation:

$$\text{Total AC power (resource)} = K_r * f_{MAX} * AF * N_r$$

where:

K_r is the power constant for the resource in mW/MHz.

f_{MAX} is the maximum frequency at which the resource is running. Frequency is measured in Megahertz.

AF is the activity factor for the resource group. The activity factor is a percentage of the switching frequency.

N_r is the number of resources used in the design.

The FPGA routing interconnect is a major contributor to overall power consumption. It is proportional to the capacitance of the metal layer and toggle rate.

The activity-factor percentage (AF%) is defined as the percentage of frequency (or time) that a signal is active or toggling the output. Most resources associated with a clock domain are running or toggling at some percentage of the frequency at which the clock is running. Users of the power-analysis tool can enter this parameter as a percentage manually. Or they can import the activity based on simulation results. AF accuracy,

which is typically imported from simulation results, depends on clock frequency, stimulus to the design, and the final output. If no simulation results are available, the general recommendation for a design occupying roughly 30% to 70% of the device is to provide an AF% between 15% and 25%. AF can be calculated for each routing resource—output or PFU.

I/Os consume a significant portion of the power in a device. They can be configured as sequential or combinatorial for the given design. The activity of combinatorial I/Os is determined by the signals provided by the user (in the case of inputs) or as an output of the design (in the case of outputs). The rates at which I/Os toggle define their activity. The output toggle rate (TR) in Megahertz is defined by the following equation:

$$\text{Toggle rate (MHz)} = 1/2 * f_{\text{MAX}} * \text{AF}\%$$

Other environmental factors, such as board size, heatsink, and airflow, are factored into calculations for dynamic and static power consumption.

MANAGING POWER CONSUMPTION

One of today's most critical design factors is the need to reduce system power consumption—especially for modern handheld devices and electronics. Designers can use several FPGA design techniques to significantly reduce overall system power consumption including:

1. Reducing operating voltage
2. Operating within the specified package temperature limitations
3. Using optimum clock frequency, as the dynamic power is directly proportional to the frequency of operation. Designers must determine if a portion of their designs can be clocked at a lower rate that will reduce power consumption.
4. Reducing the span of the design across the device. A more closely placed design utilizes fewer routing resources for less power consumption.
5. Reducing, where possible, the voltage swing of the I/Os
6. Using optimum encoding where possible. On average, for example, a 16-bit binary counter has only a 12% activity factor and a 7-bit binary counter has a 28% activity factor. On the other hand, a 7-bit linear feedback shift register could toggle as much as a 50% activity factor, which will cause higher power consumption. A gray code counter, where only 1 bit changes at each clock edge, will use the least amount of power. After all, the activity factor would be less than 10%.

7. Minimize the operating temperature:
 - a. Use packages that can better dissipate heat, such as packages with lower thermal impedance.
 - b. Place heatsinks and thermal planes around the device on the printed-circuit board (PCB).
 - c. Adopt better airflow techniques using mechanical airflow guides and fans (both system and device-mounted fans).

TYPICAL POWER-ANALYSIS SCENARIOS

FPGA power-analysis tools can be used to estimate power consumption at any stage in the FPGA design flow. For example, the tools can be used to estimate power before completing the actual design. They also can be used after place and route, importing the resulting design database. The accuracy of the power-analysis tool increases when provided with post-mapped, post-placed, or post-routed results. An FPGA design flow that incorporates power analysis typically provides milestones: estimate-driven, post-place and route, and post-simulation. Figure 2 illustrates the flow and typical milestones in a power-aware FPGA design flow.

1. Estimate-driven: Utilized resources and toggle activity are entered manually.
2. Post-place and route: Post-place-and-route resources are imported for a more accurate utilization model.
3. Post-simulation: Toggle activity produced by an HDL simulator is imported for a more accurate activity factor and toggle rate model.

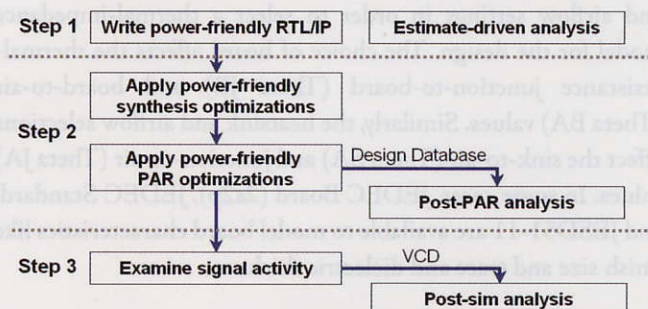


Figure 2: Here is the design flow for FPGA power analysis.

To accommodate the differing amounts of model details available to the analysis tool, power-estimation tools may be modal in operation. In an “estimate-driven” mode, the analysis engine calculates consumption based on device resources or a template provided by the user. This mode is most useful during early device-review and “what-if” analysis scenarios. In this mode, the designer supplies frequency, activity factor, voltage parameters, and device utilization. The designer also needs to provide the

conditions of operation, such as ambient temperature. With some advanced power tools, the designer also can select thermal profiles like the size of the board, heatsinks, and airflows.

In a more accurate calculation mode, which occurs during post-place-and-route analysis, the tool calculates power consumption on the basis of device resources extracted from a placement-and-routing device database. The database includes block usage and routing information. Detailed block utilization of the FPGA can be extracted from the database. FPGAs commonly include blocks representing logic of the generic programmable fabric, I/Os, clocks, embedded block RAM, embedded DSPs, PLLs/DLLs, and SERDES I/O. Once again, the environment plays a critical role in determining the operational temperature. The junction temperature and power are interdependent. As a result, an increase in one causes an increase in the other. Eventually, this aspect leads to higher cooling costs and the need to design larger battery capacities.

At the most accurate stage—post simulation—an optional value-change-dump (VCD) file, IEEE 1364 standard, contains activity and clock frequency information. The VCD file preserves waveform information that can be displayed in third-party simulation tools.

ENVIRONMENT MODELING

The power-analysis environment provides the means to model the environment of the FPGA device including PC-board layer stack-up, heatsinks, airflow, and ambient temperature. The designer may experiment with various board sizes, heatsinks, and airflow settings in order to select a thermal-impedance model for the design. The choice of board affects the thermal-resistance junction-to-board (Θ_{JB}) and board-to-air (Θ_{BA}) values. Similarly, the heatsink and airflow selections affect the sink-to-air (Θ_{SA}) and junction-to-air (Θ_{JA}) values. In some cases, JEDEC Board (2s2p), JEDEC Standard, and JESD51-11 are available to model board characteristics like finish size and trace and dielectric thickness.

Generally, regular θ_{JA} is based on the 4-x-4-in., four-layer JEDEC Standard board. A more realistic and complex PC board could be as large as 8 x 8 in. with eight to ten layers that act to dissipate heat. The board design is critical because part of the heat is absorbed and dissipated by the board. Placing high-power parts near one another makes them compete for the “thermal real estate” on the board, which may cause unexpected and unwanted results. Adding thermal vias to the board also helps to spread the heat to different layers and—possibly—out of the board entirely.

Because heatsink characteristics influence power calculations, the analysis tool may allow a variety of profiles. Heatsinks are used in cases where the thermal impedance of the board-device combination isn't small enough (i.e., when the system cannot dissipate heat fast enough). The overall effect of adding the heatsink is to reduce thermal impedance. Some of the newer advanced-device thermal-modeling and simulation tools can be used in advance to check if there are any thermal pitfalls.

Adding airflow features to a case design enables better heat dissipation through convection. This again contributes to reducing the overall thermal impedance of the system. Environment airflow, which is expressed in linear-feet-per-minute (LFM) units, is another factor commonly used by power-analysis tools. The ambient temperature is the expected operating temperature—in degrees Celsius—of the medium surrounding a device in a package. The position of the FPGA relative to other heat-emitting devices should be accounted for because another hot device in the airflow path may cause heat transfer.

Today, one of the most critical factors in design is reducing system power consumption. This aspect is especially important for handheld devices and other modern electronic products. FPGA power analysis is a parallel verification track similar to other simulation solutions. When detailed device and signal-activity information are available, analysis tools support an estimate mode for what-if scenarios or a calculator mode.

Most analysis tools feature environment model options to characterize the PC board, assembly mechanics, and airflow. Power calculators can report both the AC and DC components of power. Advances in modeling methods, such as DELPHI compact models, will improve the performance of FPGA thermal-analysis tools in the future. ♦

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