FPGAs extend use of automotive graphics

Kerry Howell examines how using FPGA devices to build video and graphics controllers is extending the applications base

LCDs truly are ubiquitous. They are encountered in the home, at work, the supermarket, at the gym and in cars. Not surprisingly, automotive is one of the fastest growing markets for LCD systems.

This growth is fuelled by several factors: declining display prices, rising user expectations, additional product features, product functionality and the convergence of consumer products in automotive applications.

A typical graphics system is built using a normal application specific standard processor (ASSP) or a custom asic as the controller. When automotive graphics designers use these devices they encounter a few speed bumps on the road to system implementation. These include short product life cycles, PC-based system bus interfaces and the inability to adapt to new standards and display types.

All these limit the design for reuse in other applications.

Fig. 1 is an example of a typical automotive graphics and video system. On the left side of the diagram are some of the different input signals that can drive a graphics system. This example shows a Media LB interface, two-wire Pixel Link transceiver for video, generic system interface bus and NTSC-Pal video encoder. Once video and graphics information are in the system, processing is performed by a general-purpose CPU or, depending on the system architecture, sent directly to the graphics processor. Additionally, most designs include flash memory for programme storage and sdram for storing page and video information.

The graphics processor may be an ASSP, custom asic or FPGA device. Depending on the implementation, there may be multiple displays in the system (as shown), which requires additional logic to manage the signals to support each display.

As previously mentioned, developers encounter several barriers when attempting to use an ASSP graphics controller in their automotive design. These barriers include:

- PC and consumer products typically have a very short life cycle; in contrast, the automotive market has a very long production and support requirements that cannot tolerate changes forced by end-of-life situations.
- Support for new or derivative video and imager standards in legacy systems cannot be supported in hardwired ASSP or asic devices.
- Hardwired systems also have difficulty in adapting to different display types. This can be in the area of resolution, aspect ratio or the display signal interface.

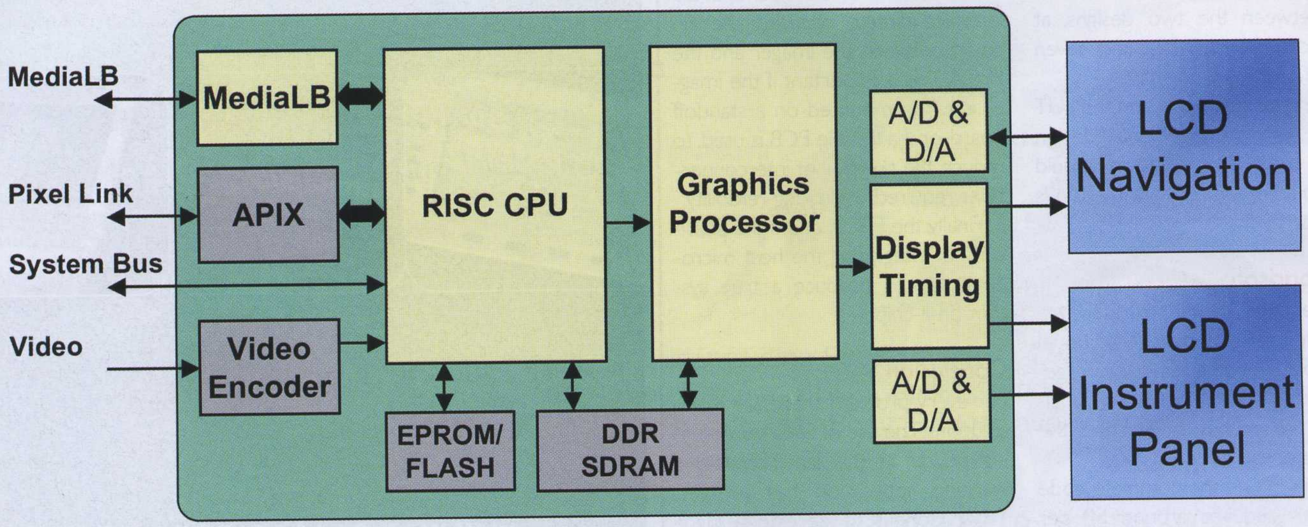

Fig. 1: Typical graphics and video system architecture

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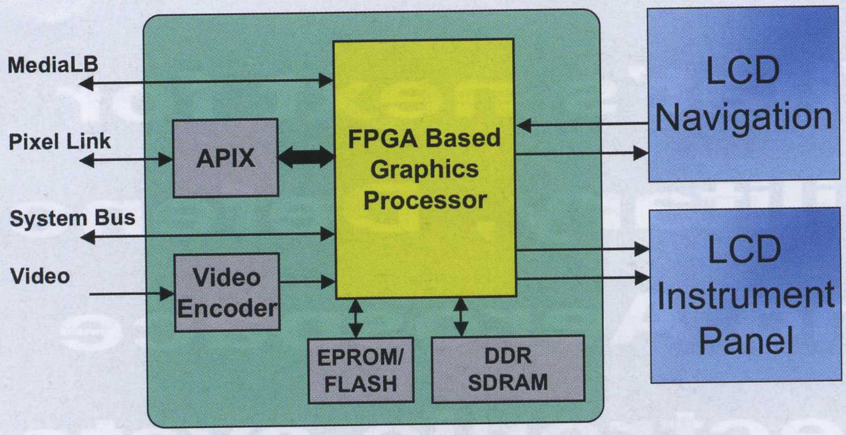

Fig. 2: Integrated vehicle graphics

- Most of the ASSP devices have standard PC bus interfaces such as AGP, PCI and PCI Express. Automotive designers incur additional cost and complexity when they build a custom interface between the internal system bus and the ASSP graphics device.

While asics have an attractively low per piece price, they are very expensive to develop. The mask charges for an asic can run in the millions of dollars and, if the design is changed to support a new standard or function, the mask charges are incurred again and again.

The versatile nature of FPGA devices, plus commercially available IP, allows for the integration of almost all the graphics system functions: video controller, risc processor, display interfaces, bus standards and different video input standards can be included in one device.

Fig. 2 is an example of the high levels of integration possible using FPGA devices. Instead of having an external Media LB device, the Media LB protocol is now processed within the internal FPGA logic. The risc processor is incorporated in the form of an IP-based soft 32bit processor. IP for the modular graphics and video core completes the design, including support for touch panel inputs, LCD backlight control, memory controller and multiple displays. This design greatly reduces the number of parts in the design by integrating all the major system functions into the FPGA. By using an FPGA with a built-in non-volatile boot flash, yet another device may be eliminated from the design.

The hardware implementation of the graphics system is part of the overall project. The designer must look at the functions of the graphics controller to find the best for the application. For instance, a customer information display (CID) may only need to display text messages and rudimentary graphics, whereas a glass instrument cluster needs high-resolution anti-aliased graphic images that realistically represent the physical gauges and instruments the CID replaces. Some instrument clusters and navigation systems also have real-time video displays for rear-view camera video that require a graphics controller that supports picture-in-picture and real-time video, without degradation of the other graphic images. Flexibility for handling multiple video streams and inputs is typically a requirement.

There are many issues to be resolved before a graphics system is implemented, because each one can affect the final hardware and IP core implementation. Some of these issues are:

- Will the source of the data be a video stream, a graphically rendered output or a combination or the two? If it is a video stream, then how many streams and at what resolutions?
- Will the final images be 2D or 3D representations?
- What type of display technology will be used? LCD? Plasma? Video? How many displays will there be, and at what resolutions?
- What is the application software interface, and how easy is it to use?
- Does this application require a scalable architecture for future growth or for a tiered set of products?
- Are multiple video pages required, and if so how many?
- Will there be scaling performed on the images and at what multipliers? If the image will be scaled, then cropping ability is also required.
- Are bitblit capabilities required for fast graphics performance? Does the application require horizontal and vertical bitblit options?
- What memory and bus interfaces are required for the system?
- Finally, will there be the need for future system expansion?

Fig. 3 shows an example of a modular 2D graphics and video IP core. This IP is representative of the features and functions that are found in current FPGA-based graphics IP cores. This fast graphics core was developed for embedding within FPGA-based systems. The memory controller can interface with sdram or ddram, depending on the application performance and cost budgets. With optional video input and bitblit modules, this IP core can be configured with the specific performance and functionality required for the design. The display controller is designed to con-

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trol single or dual displays of any display technology. This core features an internal general-purpose 32bit Amba bus that can easily interface with other internal IP cores, or external logic through the FPGA's IOs.

A complete FPGA-based graphics and video module is shown in Fig. 4. It demonstrates the small physical size and low part count possible with FPGA based graphics. This module measures just 70 x 50mm and operates on a single 3.3V supply.

An automotive graphics design with an FPGA device mitigates the issues found with ASSP and asic devices. FPGAs make it easy to develop a modular design that offers the flexibility to integrate different IP blocks, depending on the cost and feature requirements of the system. FPGAs enable design integration that typically results in a reduction of board space and parts inventory count. The long life commitments for FPGA devices ensure they will be available for the operational life of the product. Most FPGAs are field upgradeable (some devices even while they are operating), which allows for easy upgrades to support new standards and options.

Standard video and graphics IP for FPGAs offer tested and verified designs that are easy to integrate into a graphics product. Using packaged IP also speeds system development, allowing engineers to concentrate their efforts on the application rather then on low-level interfaces and graphics engines. Modular graphics IP cores allow the development and inclusion of custom graphics accelerators within the video controller. In this way, the graphics performance can be specifically scaled and optimised for the target system.

FPGAs offer the versatility to include the optimal bus and interface standards. This allows the system architect to design with the best interfaces for the entire system, rather than having to design around a specific graphics processor interface or bus. Designs using FPGAs allow the system designer complete control over the system interface: the entire design can be optimised to support real-time control and display systems that process video streams without any performance degradation.

In addition, FPGA manufacturers support density migration within the same size package. This allows more logic to be added for

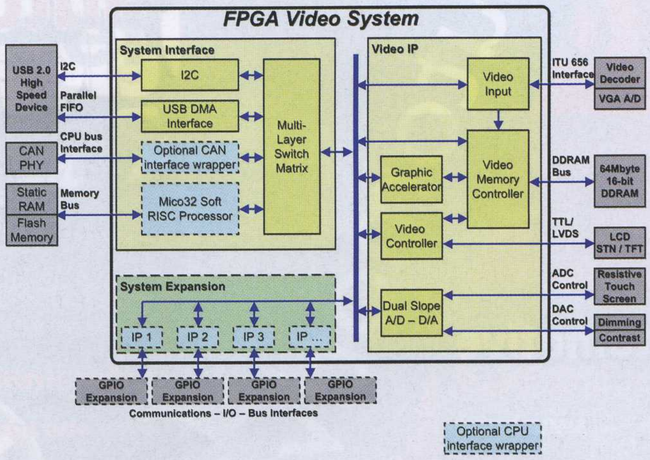

Fig. 3: Video and graphics IP contents

enhanced features, or less logic capacity for reduced functionality, without affecting the PCB layout. Density migration results in cost savings for development, production, servicing and logistics.

AEC-Q100 Grade-2 qualified FPGAs are available now, and several more with additional features and lower cost will be available in early 2008. The latest have true DSP blocks as well as single-die, non-volatile flash on board that can even be used to store the contents of internal memory blocks during power down. In the past, a concern of designers was the prices of FPGAs were too high for automotive systems. However, FPGAs now are designed for low-cost with features that make the piece price of FPGAs very competitive.

The use of FPGA devices to build video and graphics controllers is enabling automotive designers to add graphics display technology in additional applications. By using AEC-Q100 qualified FPGA devices instead of PC-related graphics controllers, the automotive market can rely on an extended product life well beyond the typical two to three year period expected with current ASSPs. ■

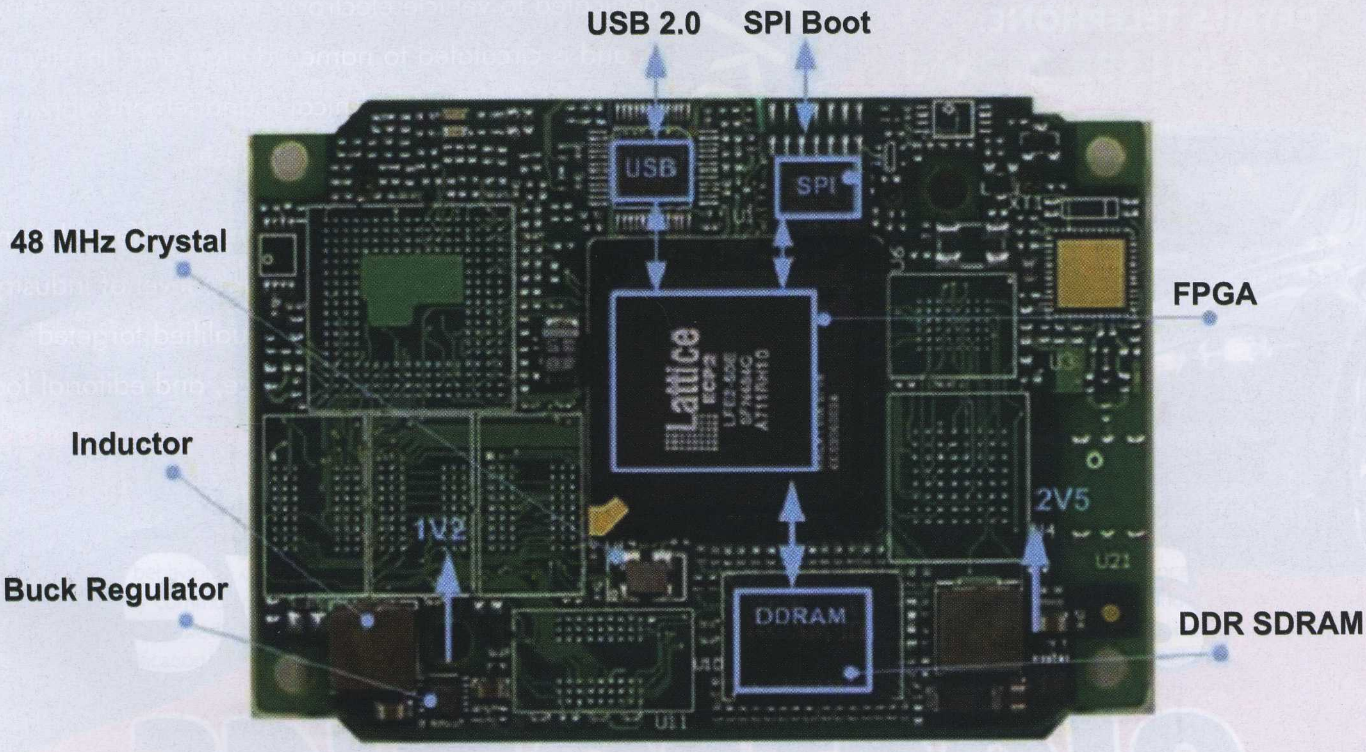

Fig. 4: Graphic and video controller module

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