FPGA FABRIC ADAPTS FOR COMMS PROTOCOLS

Many of today's electronic designs require high-speed serial I/O techniques to achieve the specified system performance criteria. As such they will continue to need a high-performance FPGA fabric

The broader FPGA marketplace however, additionally requires low-cost solutions to address newly emerging opportunities. Across diverse application spaces, communications protocols such as PCI Express and Serial Ethernet-based designs are replacing legacy PCI and Fast Ethernet interfaces.

Traditionally, Serialiser/Deserialiser- (SerDes) based FPGAs have been offered only as part of a vendor's flagship FPGA portfolio. To address serial multi-protocol transmission, the choice is to either pay the premium for an integrated, high performance FPGA family, or revert to a discrete PHY and a low-cost FPGA.

Comms processing

There are many applications in which neither of these choices is palatable. These include lower bandwidth, high volume; small form factor applications where both cost and board real estate are tightly budgeted. Applications such as wireless base-stations, low-cost industrial, audio/video, automotive, and medical applications all require both high-speed signal processing and serial transmission integrated into a low cost programmable platform. The emergence of ATCA (Advanced Telecom Computing Architecture) and microTCA standard form factors in these application areas will also drive the need to provide more hardware integration at lower cost points. In the past, the only solution available is to incur a large NRE (non-recurring expense) from Structured ASIC vendors. However, the Structured ASIC is a non-programmable solution that is more costly, inflexible and extends the time to market.

The Lattice ECP2M FPGA offers a solution that couples a low-cost FPGA fabric with a high performance MAC (Multiply Accumulate) engine, together with the industry's first integrated, low-cost SerDes on a single chip. The combination of SerDes, high performance DSP and a low cost FPGA extends system vendors' market base into areas where previously the engineering costs would have prohibited the inclusion of these serial protocols into applications.

An effective low-cost SerDes solution has to meet the specifications necessary to achieve reliable transmission and reception of key serial protocols over nominal PCB (FR-4 based) distances. Specifications include reliable transmission and recovery of serial signals for chip to chip and small form factor back planes (<40in of FR-4). There must also be embedded digital logic to support popular serial protocols, focusing on Ethernet and PCI Express, as well as other packet-based derivatives, such as Serial RapidIO and Fibre Channel. Other requirements are support for video serial standards such as SMPTE259M/292M and complete protocol stack support by developing key pieces of IP.

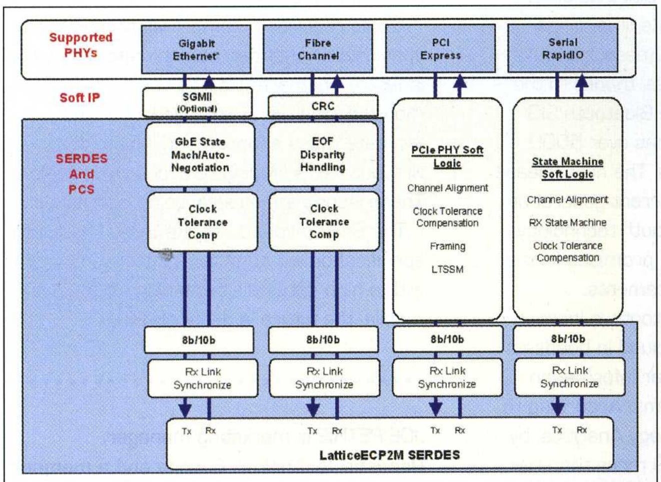

Figure 1: Lattice ECP2M Supported Packet Protocols

Protocol parity

Although each protocol is unique, they all have a layered protocol stack. However, protocol stack implementation can vary greatly from one layer to the next. Typically, the physical layer consists of fixed functionality that is common to multiple packet-based protocols, while the upper layers tend to be more customisable. The dynamic of upper layer functionality is necessitated both by the natural evolution that takes place when dealing with an emerging standard, and the desire of system vendors to create their own added value via proprietary functionality.

It follows that using programmability for implementation of these upper layer serial standards means a SerDes-based FPGA solution will remain a necessity for the foreseeable future.

Many elements of the PHY (Physical Layer) are common across many of the packet-based protocols. The functionality is partitioned into the electrical sub-block and the digital logic sub-block. These blocks are the foundation for implementing a multitude of existing and emerging serial packet-based protocols.

Building by blocks

System-level designers can face moving large blocks of data from one location to another over moderate distances and at high speed. Historically, this was accomplished by a source synchronous parallel interface, which required large banks of parallel line drivers and receivers. It has become more and more difficult to ensure the data integrity of these types of interfaces from board to board at the gigabit plus data rates that are required in systems today.

With the inception and growing acceptance of SerDes devices, designers can alleviate the concerns inherent in the implementation of a parallel interface. SerDes technology permits smaller, less expensive cables and connectors, while providing more robust signal integrity when

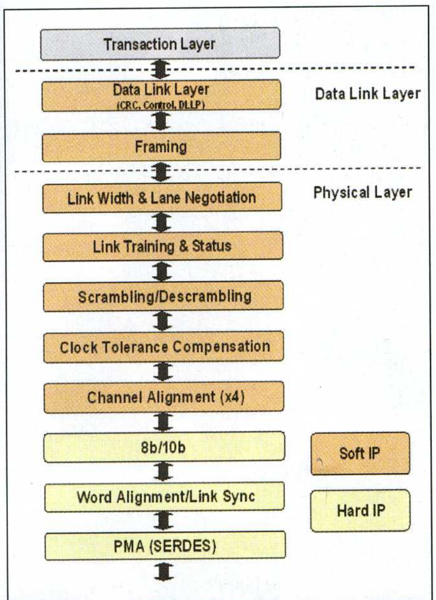

Figure 2: Lattice ECP2M PCI Express Protocol Stack

moving large blocks of data at rates of 3.125Gbit/sec and beyond.

The Lattice ECP2M delivers integrated SerDes and FPGA performance with a drive length across the passive channel of 40in of FR-4 Backplane @ 3.125Gbit/sec (aided by built-in Tx pre-emphasis and Rx equalisation).

Its Tx/Rx jitter values (0.25UI at for Tx, 0.65UI tolerance for Rx, typical at 2.5Gbit/sec) meets PCI Express, GbitEthernet and jitter specifications. The power performance is 100 mW/channel (typical) @ 3.125Gbit/sec, including I/O buffers and Rx equalisation. The 270Mbit/sec to 3.125Gbit/sec serial data rates (full and half rate data rates selectable per channel), with emphasis on PCI Express and Gigabit Ethernet-based applications, provide flexibility.

Wireline networks

PCI Express, Serial RapidIO, Ethernet and Fibre Channel are four of the most popular serial protocols used in wireline applications.

Designers have implemented newer versions of conventional PCI, such as PCI-x and PCI-x 2.0, allowing them to maintain the existing software base while achieving greater throughput. Even with these enhancements, processor throughput still outpaces I/O throughput.

PCI Express was conceived in order to address these ever-increasing bandwidth requirements by providing a scalable, point-to-point serial connection between chips, over cable or via connector slots for expansion cards, while maintaining compatibility with conventional PCI at the software layer.

A single PCI Express serial link is a dual-simplex connection, specified to speeds of up to 2.5Gbit/sec/link that can be scaled in one, two, four, eight, 12, 16 and 32 lane widths to achieve greater bandwidth. A serial implementation is cheaper, can be driven further distances and alleviates common mode noise and skew concerns inherent in existing source synchronous parallel interfaces (such as conventional PCI), as well as reducing the overall number of connections required. Figure 2 illustrates the PCI Express protocol stack and the cost of soft IP implementation.

Serial RapidIO

Another emerging serial standard is Serial RapidIO. This also has its roots in the source synchronous world. When combined with the existing RapidIO parallel specification, Serial RapidIO allows designers to standardise on a single interconnect technology for networking, telecommunications and other embedded applications.

Serial RapidIO is a scalable, point-to-point, low pin count interconnect designed to address increasing system bandwidth needs. It leverages industry-standard signalling technology found in Fibre Channel, 10G Ethernet XAUI interfaces and Infiniband, and operates at 1.25, 2.5 and 3.125 Gigabaud per link.

Ethernet, based on the volume of installed ports, is the most dominant networking protocol. Gigabit Ethernet (GbE) increases the speed tenfold over Fast Ethernet from 100Mbit/sec to 1,000Mbit/sec, or 1Gbit/sec. By leveraging the Fast Ethernet protocol stack, GbE allows engineers to migrate Fast Ethernet solutions while maintaining software compatibility with existing products.

The Lattice ECP2M family offers a compliant 802.3z implementation of a GbE PHY in the PCS portion of the SerDes. This embedded block provides functionality such as 8b/10 encode/decode, link state machine, auto-negotiation and clock tolerance compensation. When combined with available MAC layer IP and proprietary upper layer functionality, the device allows the user to design a fully integrated GbE solution.

Fibre Channel is a high performance serial link supporting its own and other higher-level protocols, such as the FDDI, SCSI, HIPPI and IPI. The FC standard addresses the need for very fast, reliable transfers of large amounts of information.

The bulk of current implementations operate at 1Gbit/sec on a single serial channel; however, specifications exist for single channel data rates of 2G, 4G and 10Gbit/sec.

Other emerging, packet-based protocol standards such as the CPRI and OBSAI are gaining momentum in the wireless infrastructure. These standards also receive PHY layer support in the Lattice ECP2M by virtue of the SerDes and the embedded 8b/10b encode/decode block.

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