Embedded technology meets connectivity challenges using FPGAs

by Van Macomb, Lattice Semiconductor

Lattice introduced the new silicon technology MACO that adds a 90nm structured ASIC capability to an advanced FPGA + SERDES platform. MACO is targeted for industry-standard IP such as memory controllers, SPI4.2, and MACs.

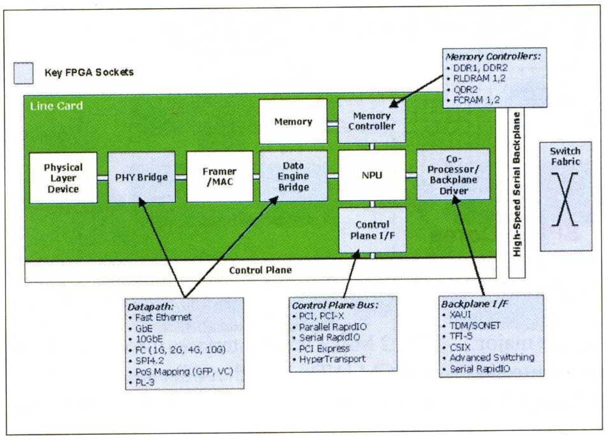

Figure 1. FPGAs in a typical communications line card

In the communications and networking markets, designers face a number of competitive pressures: time-to-market, increasing demand for bandwidth, compliance with evolving protocols, cost reduction, etc. At the same time, designers have a growing number of devices from which to choose as ASSP vendors broaden their product portfolios. For the past 20 years, one constant in this sea of change has been the reliance on FPGAs as the device of choice for meeting connectivity challenges.

In the early days, FPGAs were called upon to implement simple I/O bridging and decoding logic with a few hundred logic gates and a handful of I/O pins. Today's multi-million gate FPGAs with nearly 1000 I/O pins are relied upon to implement complex communications protocols in chip-to-chip as well as backplane applications. And increasingly, FPGAs are being relied upon to implement higher layers of the protocol stack associated with the numerous packet- and cell-based protocols in use today. Recognizing significant bandwidth, time-to-market, and protocol pressures in the communications market, Lattice Semiconductor has introduced a new silicon technology to meet the challenges for next-generation systems: the LatticeSCM.

Figure 1 summarizes the broad range of roles performed by FPGAs on a typical communications line card. At a high level, these basic functions are common across the major industries served by FPGAs, which include telecom, datacom and storage. Thus in each of these industries, FPGAs are called upon to connect ASSPs via industry-standard interfaces in the data path as well as on the control plane, connect to memory devices, and drive backplanes. The LatticeSC FPGA with MACO is designed to meet the connectivity challenge present in today's telecom, datacom and storage markets.

The LatticeSCM family of FPGAs is fabricated on a state-of-the-art 90nm technology to provide one of the highest performing FPGAs in the industry. This feature-rich device includes: a high-performance FPGA fabric; 3.4 Gbit/s SERDES (up to 32 on a single device); advanced physical coding sub-layer with dedicated logic (link layer) to support PCI Express, SRIO, SPI-4.2, SFI-4, Ethernet and fibre channel; high-performance single-ended and differential I/Os; up to 7.8 Mbit of embedded memory as well as embedded MACO blocks that are pre-engineered interfaces (discussed below).

The layout of the LatticeSCM FPGA is a regular and homogeneous array of programmable logic cells (PICs). Included in the device are embedded SERDES channels that connect to embedded multi-purpose physical coding sub-layer (PCS) blocks for managing high-speed serial data transfers. Rows of embedded block RAM (EBR) are "striped" across the array for efficient connectivity to the PFUs. At the end of each EBR row is an area of silicon that Lattice has made available for a "structured ASIC" block, allowing designers the ability to commit logic to high-performance, high-density 90nm arrays. These are termed "MACO" blocks (masked array for cost-optimization). These logic blocks because they are "hard-wired" have been fully characterized and pre-engineered in order to meet the high-speed requirements of today's communications systems. This frees the design engineer and allows him to concentrate on a systems approach to his problem. A simplified diagram is shown in figure 2.

For a comprehensive view of the LatticeSCM architecture, please refer to the LatticeSCM data sheet, which can be found on the Lattice Semiconductor web site at www.latticesemi.com. The initial LatticeSCM devices will offer pre-designed hardware IP-based industry-standard interfaces. The first MACO blocks include memory controllers, SPI4.2 interfaces, and flexible MAC blocks supporting GbE, 10GbE and PCI Express protocols.

The following are brief descriptions of the "structured ASIC" MACO blocks that are shown in figure 2. The LatticeSCM devices provide dedicated high-speed memory controllers

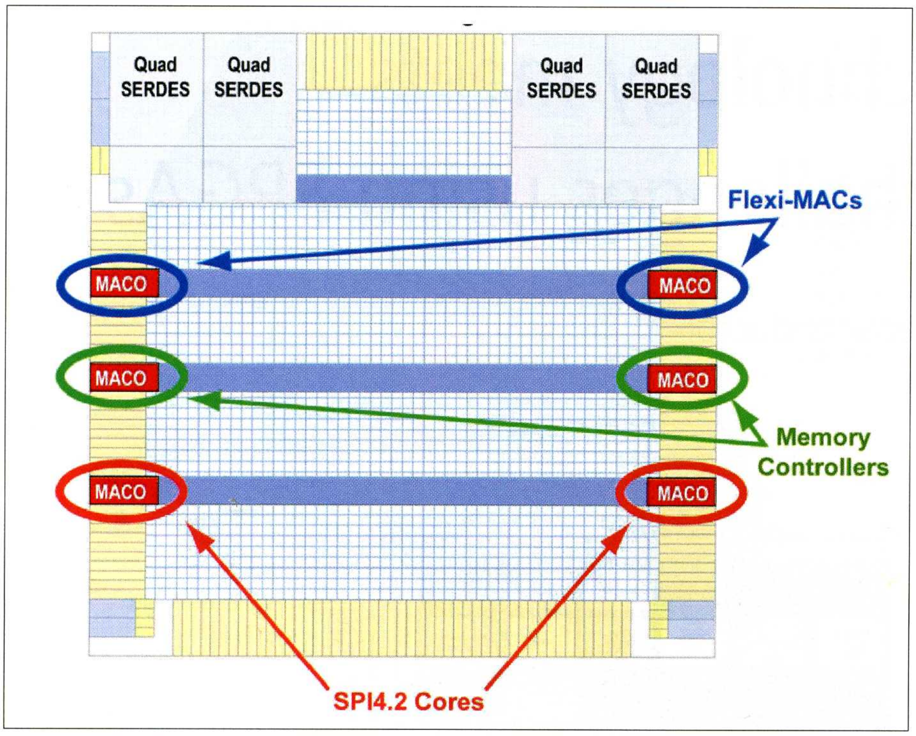

Figure 2. LFSC25 FPGA with predesigned MACO blocks

with MACO technology supporting the major high-speed memory standards implemented in many communications systems today, DDR fi SDRAM, QDR fi SRAM, and RLDRAM fi. These functions would require significant resources and critical timing control if they were implemented in a typical look-up table architecture.

Initial LatticeSCM FPGAs will incorporate one or two SPI4.2 cores implemented in MACO. Each is fully compliant with the OIF-SPI4-02.0 specification, offering up to 256 logical ports, with transmit/receive data paths that are 16-bit wide with in-band port address, SOP, EOP indication and error control. Each SPI4.2 MACO core interfaces directly with LatticeSCM LVDS I/Os that offer source synchronous double edge clocking at 311 MHz minimum and in static or dynamic alignment modes. The core supports up to 1 Gbit/s with dynamic phase alignment and up to 700 Mbit/s in static alignment mode. The SPI4.2 MACO core interfaces with the FPGA via a 128-bit user-accessible data path. Only 1500 FPGA LUTs and 10 EBR are used, primarily for buffering FIFOs and status path management.

FlexiMAC is a flexible packet framer and parser that can implement Layer 2 (data link layer or MAC) functionality for various standards. Implemented in MACO technology, the flexi-MAC functionality complements the LatticeSCM SERDES and the Layer 1 (physical layer) multi-protocol functionality of the physical coding sub-layer (PCS). This results in a complete Layer 1/Layer 2 solution for 1G/10G Ethernet standards and provides customers with integrated 1GE/10GE solutions without using up valuable FPGA gates.

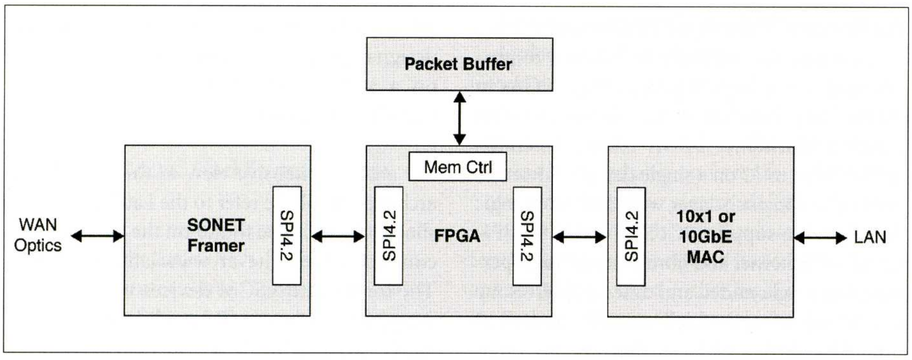

Figure 3. FPGA as a SONET-to-Ethernet bridge employing SPI4.2

MACO provides multiple advantages: speed, density and lower power dissipation. Because MACO is implemented in 90nm ASIC gates, the performance increase over SRAM-based look-up-table architecture can exceed 100%. This advantage was demonstrated in a simple test where a 32-bit CRC (cyclic redundancy check) design was targeted toward both the SC FPGA fabric and the SC MACO technology.

A sample application using an FPGA with a SPI4.2 interface in an Ethernet-to-SONET bridge design was used to demonstrate the area efficiency of MACO. A block diagram of this application is shown in figure 3. The FPGA is used to manage the bridge, including flow control and packet buffering, which usually requires a memory controller and external buffer. If the SPI4.2 interfaces in this example were to be implemented in soft IP using FPGA gates, the design becomes considerably more difficult and may require a larger device. Lattice studies have found that each MACO core is equivalent to at least 5000 LUTs, while occupying only 10% of the area of an equivalent FPGA implementation. With multiple MACO blocks per device, this results in substantial cost savings by lowering the development cost and saving significant silicon area.

For a comparison of power dissipation, we will again use a SPI4.2 core as an example. The Lattice SPI4.2 solution using the LatticeSCM FPGA utilizes MACO technology for the majority of a SPI4.2 core. Only 1500 LUTs and 10 EBRs are used in the LFSC FPGA fabric, primarily for FIFOs and the SPI4.2 status path. Considerably less than competitive FPGA SPI4.2 solutions that use only FPGA gates to implement entire SPI4.2 cores. In contrast, the LatticeSCM solution benefits from the low power dissipation of the MACO technology. In fact, a LatticeSC FPGA could implement four SPI4.2 cores for the same power budget that certain competing FPGAs would dissipate in implementing a single core, an important consideration when packing density is a key issue. ■