



# Lattice ispLeverCORE IP Tutorial

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## Type Conventions Used in This Document

Convention	Meaning or Use
<b>Bold</b>	Items in the user interface that you select or click. Text that you type into the user interface.
<i>&lt;Italic&gt;</i>	Variables in commands, code syntax, and path names.
<b>Ctrl+L</b>	Press the two keys at the same time.
<i>Courier</i>	Code examples. Messages, reports, and prompts from the software.
...	Omitted material in a line of code.
. . .	Omitted lines in code and report examples.
[ ]	Optional items in syntax descriptions. In bus specifications, the brackets are required.
( )	Grouped items in syntax descriptions.
{ }	Repeatable items in syntax descriptions.
	A choice between items in syntax descriptions.

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# Lattice ispLeverCORE IP Tutorial

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## Introduction

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Lattice's ispLeverCORE™ IP modules are large, modular design blocks that can be reused and easily placed within your programmable logic design.

This tutorial is designed to help you evaluate the IP module package you have chosen as quickly as possible. Admittedly, it is brief and intended for users that are familiar with all the required tools and processes.

### Supported Technologies

Lattice ispLeverCORE IP modules are available for LatticeECP-DSP, LatticeECP2, LatticeEC, LatticeXP, LatticeSC/SCM, and MachXO technologies. This tutorial is written to support all device technologies.

### Learning Objectives

When you have completed this tutorial, you should be able to do the following:

- ◆ Download an ispLeverCORE IP using IPexpress software.
- ◆ Customize and Generate Output Files.
- ◆ Run Functional Simulation Using ModelSim.
- ◆ View Resource Utilization and Performance.

## Time to Complete This Tutorial

The time to complete this tutorial is about 60 minutes.

## System Requirements

The following software is required to complete this tutorial:

- ◆ ispLEVER Software version 5.1 or higher

## Directory Path Description

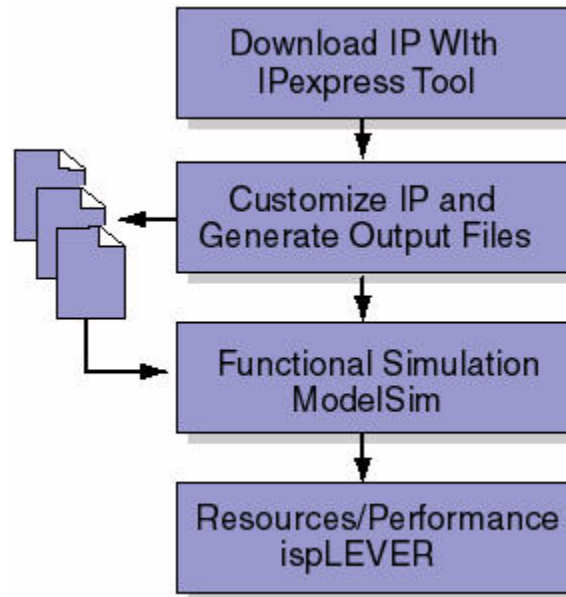
To accommodate all ispLeverCORE IP module download packages, the directory paths are described as *<variables>*.

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## Evaluation Tutorial Flow

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You must run this tutorial in its organized sequence.



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## Downloading the ispLeverCORE Using IPexpress

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You must download and install your ispLeverCORE using IPexpress software. When you start IPexpress, the main window allows you browse ispLeverCORE IP modules available on your local computer and on the Lattice IP Server. The ispLeverCORE IP Modules are available in User-Configurable and Factory-Configured versions.

### Note


Some legacy ispLeverCORE IP modules require factory assistance to configure the core parameters and options. There is a tutorial available for Factory-Configured versions of ispLeverCORE IP Modules at:

[http://www.latticesemi.com/lit/docs/ip/ip\\_tutorial.pdf](http://www.latticesemi.com/lit/docs/ip/ip_tutorial.pdf).

For this tutorial, you will be working with User-Configurable versions.

*To view ispLeverCORE IP Modules available from the Lattice web site*

1. Start the IPexpress software in one of three ways:
  - ◆ From your PC's Start menu, choose **Programs > Lattice Semiconductor > Accessories > IPexpress**;
  - or,
  - ◆ From the ispLEVER Main Window, choose **Tools > IPexpress**;
  - or,

- ◆ Click the  button on the ispLEVER Tools tool bar.
2. In the IPexpress Main Window, click the **Display IPs in the Lattice IP Server** tab, located in the lower left corner of the Main Window. IPexpress automatically connects to the internet.
3. Expand the Lattice IPs Server folder in the left panel.
4. Expand remaining folders to view to the available ispLeverCORE IP Modules

## Installing or Downloading ispLeverCORE IP Modules

You can download and install ispLeverCORE IP modules on your computer, or you can simply download them and then install them at a later time.

*To install an IP in IPexpress:*

1. Highlight the desired IP in the IP list, then click the **Install** button on the Main Window tool bar, or you can right-click on the desired IP and choose **Install** from the drop-down menu.
2. Follow the on-screen instructions.

*To download an IP for installation at a later time:*

1. Highlight the desired IP in the IP list, then click the **Download** button on the Main Window tool bar or you can right-click on the desired IP and choose **Download** from the drop-down menu.
2. Specify a location in which to save the IP in the dialog box, and click **Save**.
3. When you are ready to install the IP, double click on the `<ip_name>.exe` file that you had previously saved, and follow the on-screen instructions. Once completed, the installed IPs will appear in the Installed IPs/Modules tab of the Main Window.

### Note

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For a more complete description on running IPexpress and installing/downloading ispLeverCORE modules, refer to the *IPexpress Quick Start Guide*.

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## Customizing and Generating the IP



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Once you have downloaded and installed an ispLeverCORE IP module, you can customize it with the IPexpress software.

*To customize an ispLeverCORE IP module in IPexpress:*

1. Click the **Installed IPs/Modules** tab.
2. Select the desired IP in the list.

### Note

User-Configurable IPs are indicated in the list with a  icon. Factory-configurable IPs are indicated in the list with a  icon.

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3. Enter the following information in the right pane of the Main Window:
  - ◆ **Project Path** - Browse to your project directory (for example: c:/<project\_dir>).
  - ◆ **File Name** - An entry box for file name.
  - ◆ **Design Entry** - Select a design entry format from the drop-down list.
  - ◆ **Device Family** - Select the name of the device family for the module or core you've selected.
  - ◆ **Part Name** - Select a part name from the drop-down list.
4. Click the **Customize** button in the Main Window tool bar, or click the **Customize** button in the lower right corner of the Main Window. This displays the Configuration dialog box for your IP.

*To generate IP output files:*

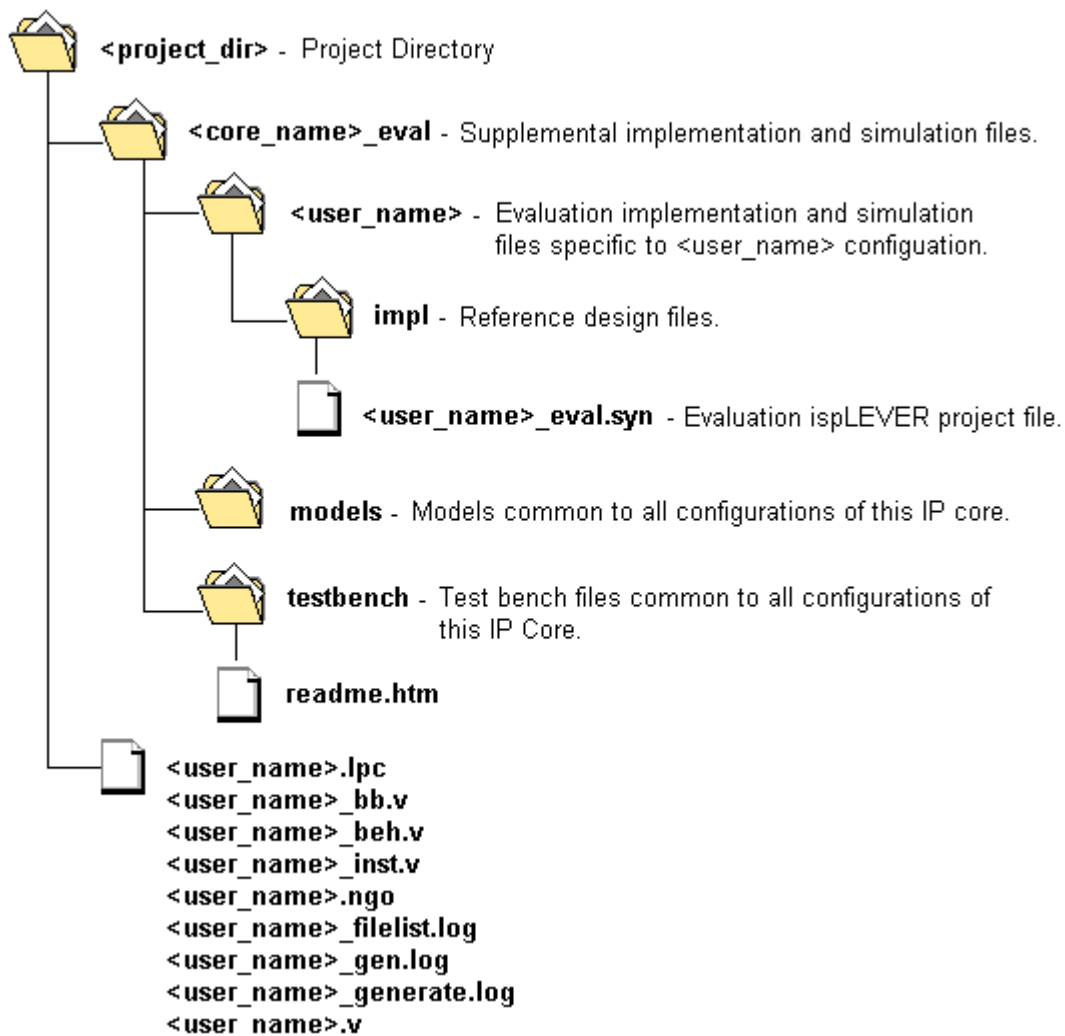
1. Set desired IP parameters, if available, in the Customization dialog box.
2. Click **Generate**. The output directories and files are generated in the location you specified in the Configuration dialog box.

## Generated IP Directory Structure

When you customize and generate your core using IPexpress, the following files and folders are created.

### Note

The directory structures/file names described in this tutorial are typical, but can vary in some cases. Refer to your ispLeverCORE *User Guide* for information specific to your ispLeverCORE module.



## File Definitions:

`<user_name>.v` - IP Core Wrapper file (optional).

`<user_name>.lpc` - Lattice Parameter Configuration file. This file contains the configuration parameters that have been selected using the IPexpress user interface.

`<user_name>_bb.v` - Black box module wrapper for synthesis.

`<user_name>_beh.v` - Behavioral simulation model for IP core configuration user name.

`<user_name>_inst.v` - Example of instantiation template to be included in the user's design.

`<user_name>.ngo` - Synthesized and mapped IP core.

`<user_name>_generate.tcl` - Created when IPexpress graphical user interface "Generate" button is pushed. Invokes core generation. May be run from command line.

`<user_name>_filelist.log` - List of files and folders created when IP core is generated.

`<user_name>_gen.log` - IPexpress IP generation log file.

`<user_name>_generate.log` - ispLEVER synthesis and map log file.

`<user_name>.v` - IP core wrapper (optional).

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## Running Functional Simulation Using ModelSim

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A simulation script file is provided in the `eval` directory for functional RTL simulation. The script file `<core_name>_eval.do` uses simulation models provided with this package. The simulation models are located in the directory `<project_dir>\<core_name>_eval\<user_name>\src\beh_rtl\<family_name>`.

*To run functional simulation using ModelSim:*

1. Open ModelSim.
2. Choose **File > Change Directory** and go to the `<project_dir>\<user_name>_eval\sim\modelsim` directory.
3. Run the ModelSim DO (macro) file, choose **Tools > Execute Macro** and select the file: `scripts\<modelsim_macro_name>.do`.
4. The ModelSim macro executes an evaluation test bench designed to show some example transactions or functions associated with the core. You can create your own test benches and use the simulation models.

5. View the waveform results in the Wave window.

### Note

The behavioral simulation model (<user\_name>\_beh.v) generated by IPexpress is compatible with Third-party EDA simulators that support Verilog HDL.

For more information on using 3rd party simulators with ispLEVER see the *Simulating Designs for Lattice FPGA Devices* topic in the ispLEVER software online Help.

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## Viewing Resource Utilization and Performance

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This procedure shows you how to view resource utilization and performance of the ispLeverCORE module using the ispLEVER software.

*To open the ispLeverCORE module in ispLEVER and generate the timing report:*

1. In ispLEVER Project Navigator, choose **File > Open Project**.
2. Browse to \<project\_dir>\<core\_name\_eval>\<username>\impl in the Open Project dialog box..

### Note

The directory structures/file names described in this tutorial are typical, but can vary in some cases. Refer to your ispLeverCORE *User Guide* for information specific to your ispLeverCORE module.

3. Select and open <username>\_eval.syn. All of the files needed to support top-level synthesis and implementation will be imported to the project.
4. In ispLEVER Project Navigator, choose **Source > Import Constraint/Preference File** and import the preference file corresponding to the synthesis tool being used.

## Enable Hardware Evaluation (Optional)

Lattice's IP hardware evaluation capability makes it possible to create versions of IP cores that operate in hardware for a limited period of time (approximately one hour) without requiring the purchase on an IP license. The hardware evaluation capability is enabled by including a specific attribute string in the top level of the design that contains the IP. The attribute string is included in the top-level module declaration as follows:

```
module <top_design> (  
  signal_1,  
  signal_2,  
  .  
  .  
  signal_n  
)  
/* <attribute string> */  
;
```

The specific attribute string to be inserted is a function of the Lattice IP core being used, the Lattice FPGA device family being targeted, and the synthesis tool being used.

Please refer to the user's guide of your specific IP core to obtain the specific string. The same string may be included in your top-level designs to enable hardware evaluation of the IP core in the context of your application.

When the attribute string is included in the top level of the design, it is possible to generate a programming file that may be downloaded into the device. After initialization, the IP core will be operational for approximately one hour.

After one hour, the IP core will stop working and it will be necessary to reprogram the device to re-enable operation. This hardware evaluation capability is only if the core has not been licensed.

During implementation, a license check is performed. If a license is not detected, a pop-up window will be displayed indicating a license failure. Click "OK" in the window and generation will proceed to completion with hardware evaluation enabled.

If a license is detected, no pop-up window is displayed and core generation is completed with no restrictions.

## Viewing Resource Utilization

The ispLEVER design mapper (map) converts the logical design of the IP module to physical resources of the target device and reports resource utilization. The map report provides a design summary including Register, LUT4, block RAM, and DSP components.

*To view resource utilization:*

1. In the ispLEVER Project Navigator Sources in Project window, select the device top-level entry.
2. In the Processes window, double-click the **Map Report** process to run the design mapper and open the Map Report (<project>.mrp) in the Output panel.

## Viewing Place and Route Results

The ispLEVER place and route program (PAR) produces a placed and routed native circuit description (.ncd) file of the design, and a report of the results.

The place and route report provides implementation details such as clock and set/reset signals, IOLOGIC, PFU Slices, DSP block elements, and EBRs. The report's timing score reflects a composite of the PAR program's ability to meet all timing preferences. The lower the score, the more preferences were met. For each routing iteration, the router will attempt to reduce this number until the number of routing iterations is completed or the value is 0, meaning the design has fully met the timing constraints.

*To view place and route results:*

1. In the ispLEVER Project Navigator Sources in Project window, select the device top-level entry.
2. In the Processes window, double-click the **Place & Route Report** process to run place and route and to open the Place & Route Report (<project>.par) in the Output panel.

## Viewing Performance Results

Performance results of the ispLeverCORE IP module can be produced by the ispLEVER static timing analysis (STA) program TRACE (Timing Reporter and Circuit Evaluator).

TRACE enumerates each timing constraint specified versus the actual result. The critical paths related to each preference is reported in terms of both logical (netlist) and physical path details. Choose **Tools > TRACE Options...** for additional analysis options.

*To view performance results:*

- ◆ In the ispLEVER Project Navigator Processes window, right-click on **Place & Route TRACE Report** and choose **View** to run STA and to open the TRACE report (<project>.par) in the Output panel.

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## Summary

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You have completed the “Lattice ispLeverCORE IP Tutorial.” In this tutorial, you have learned how to do the following:

- ◆ Download an ispLeverCORE IP using IPexpress software.
- ◆ Customize and Generate Output Files.
- ◆ Run Functional Simulation Using ModelSim.
- ◆ View Resource Utilization and Performance.

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## Glossary

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Following are the terms and concepts that you should understand to use this tutorial effectively.

**Factory-Configurable IP** - Allows you to configure the IP and generate a Lattice Parameter Configuration (.lpc) file. The .lpc file must then be submitted to Lattice for generation of a custom IP configuration that matches your .lpc file parameters. Many Factory-Configurable ispLeverCORE modules come pre-installed in IPexpress. Contact your local Lattice Sales/Applications representative for more details.

**IPexpress** - IPexpress is an ispLEVER application that enables you to generate parameterized modules and IP cores from templates supplied by Lattice Semiconductor and third-party vendors. It is similar to the Module IP Manager but is used only to generate IP cores and parameterized modules for Lattice FPGA devices.

**ispLEVER Software** ispLEVER software Development System is the Lattice software used to design, simulate, implement, and verify your Lattice programmable logic design.

**ispLeverCORE IP module** An ispLeverCORE IP module is a Lattice large modular design block that implements popular industry-standard functions. It can be reused and easily placed within a programmable logic design. Lattice ispLeverCORE IP modules are optimized for use with the Lattice device families.

**ispVM System** ispVM System is Lattice Semiconductor's second-generation device download technology, which is used to program, or configure, JTAG programmable devices. It is based on the concept of a portable virtual machine which provides multi-vendor programming support, improved performance, and increased functionality.

**.par file** A .par file is an FPGA report file summarizing the information from all placement and routing iterations. The report also shows the steps taken as the program converges on a placement and routing solution. Running the Place & Route Report process in the Project Navigator generates this file.

**.prf file.** A .prf file is an ASCII text file containing preferences (placement, routing, timing constraints, or all three) specified during design entry and preferences that you added. The .prf file is an optional input to MAP, PAR, EPIC, and TRACE.

**User-Configurable IP** - Allows you to configure the IP and generate a netlist and simulation file for use in your design. Please note that you may be prevented from generating a bitstream or the bitstream may have time logic present unless you purchase a license for the IP.

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## Recommended Reference Materials

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The following reference materials are recommended to supplement this tutorial:

- ◆ *IPexpress Quick Start Guide*
- ◆ *Lattice ispLEVER online Help for IPexpress*
- ◆ *Mentor Graphics ModelSim online Help for ModelSim*

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## Getting Technical Assistance

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Customers can receive direct technical support for all Lattice products by calling Lattice Applications during the hours of 8 a.m. to 5 p.m. Pacific Time.

### Telephone Support Hotline

For USA & Canada: 1-800-LATTICE (528-8423)

For other locations: 503-268-8001

### E-mail Support

[techsupport@latticesemi.com](mailto:techsupport@latticesemi.com)

### Internet

<http://www.latticesemi.com>